Fast-Locking, High Sensitivity Tuned-IF Radio Receiver Achieved with a 7-GHz Synthesizer

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INTRODUCTION

To improve sensitivity and selectivity in modern radios, there is a need to minimize phase noise and reference spurs, and to reduce the lock time. The circuit outlined in this article improves local oscillator (LO) performance with respect to each of these.

Phase noise is a measure of the purity of the LO signal. It is ascertained by taking the ratio of the output fundamental power to the noise power in a 1-Hz bandwidth at a given offset from the carrier. The result is expressed in dBc/Hz.

Spurious frequency elements (*spurs*) can occur in the output due to internal switching in the synthesizer. In an integer-*N* synthesizer, they are generally due to the phase-frequency detector (PFD) frequency; in a fractional-*N* device, they can be a result of the nature of the synthesizer architecture. In an integer-*N* phase-locked loop (PLL), they are called *reference spurs.*

Lock time refers to the time it takes to switch the output from one frequency to another—an important specification in many systems. In general, we say that the output is switched—or has locked—to the new frequency when it has settled to within a certain percentage, or parts per million (ppm), of the final desired frequency—or has locked to within a specified number of degrees of the final phase.

Traditional Receiver Implementation

Figure 1 shows the general block diagram for the most popular receiver architecture (*superheterodyne* receiver). The system shown here is typical for receivers designed to meet the DCS1800 standard for mobile phones. For this standard, the Receive (Rx) band is 1805 MHz to 1880 MHz.

In Figure 1, the RF input is applied to an RF filter, followed by a low-noise amplifier (LNA). The signal is then mixed down to the intermediate frequency (IF) by a mixer with a tuned LO input. Additional filtering follows, and a final mixer, using a single-frequency LO, takes the fixed IF down to baseband.

The tuned-RF LO starts with a clean and stable reference frequency, followed by an ADF4106 PLL synthesizer and a voltage-controlled oscillator (VCO). The reference is provided by a temperature-controlled (TCXO), voltage-controlled (VCXO), or oven-controlled (OCXO) crystal oscillator. The PLL synthesizer's R-divider conditions this reference to a value equal to the channel spacing in integer-*N* systems—or a multiple of the channel spacing in fractional-*N* systems. The PFD compares the loop output, F_{VCO}, divided by N, with the output of the R-divider, and the loop drives the PFD output toward zero by driving the VCO to make $F_{VCO} = F_{PFD} \times N$. *N* is varied to vary the LO output frequency, thus tuning the radio.

Phase noise of the LO depends on a number of factors: reference noise; noise in the synthesizer (R-divider, N-divider, PFD, and charge pump); the value of *N*; and the frequency at which the synthesizer PFD is operated.

The phase noise of the LO (dB) can be described by the general equation:

$$PN = PN_{SYNTH} + 20 \log N + 10 \log F_{PFD}$$

where:

PN_{SYNTH} is the phase noise contribution of the synthesizer (given in the appropriate data sheet, in dB)

20 log *N* is the additional noise due to the *N* value in the synthesizer

10 log F_{PFD} is the noise contribution due to the synthesizer PFD frequency.*

*For a more detailed explanation, please see "Design a Direct 6-GHz Local Oscillator with a New, Wideband, Integer-*N*, PLL Synthesizer" in *Analog Dialogue*, Volume 35 (print edition) or http://www.analog.com/library/analogDialogue/archives/35-06/ADF4106/index.html.

The level of reference spurs depends on: the PFD design, leakage in the charge pump section of the PFD, the PLL loop bandwidth, and VCO sensitivity. The lock time depends on: the PFD frequency and the PLL loop bandwidth.

In the receiver, with the IF chosen as 230 MHz, the tuned RF has to go from 2035 MHz to 2110 MHz (using high-side injection), in 200-kHz steps. Using an integer-*N* architecture to do this, a PFD frequency of 200 kHz is needed and the *N* value would vary from 10175 (2035 MHz) to 10550 (2110 MHz).

Using the best commercially available components (ADF4106 PLL synthesizer), the expected in-band phase noise in this system would be –85.6 dBc/Hz. Typical reference spurs in such a system would be –88 dBc at 200 kHz and –90 dBc at 400 kHz.

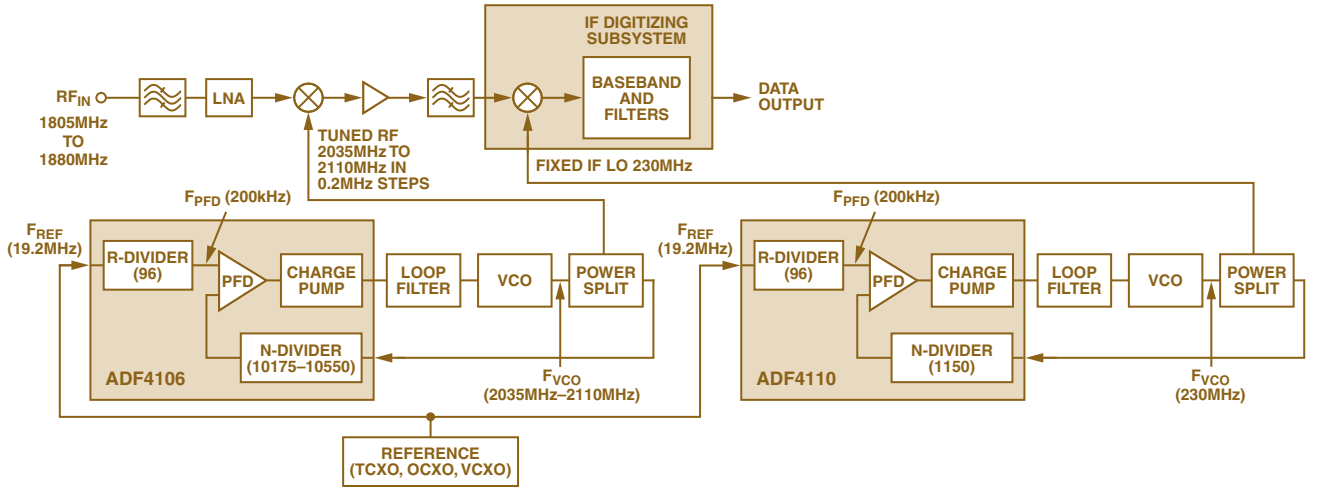

Figure 1. Block diagram of a traditional superheterodyne receiver.

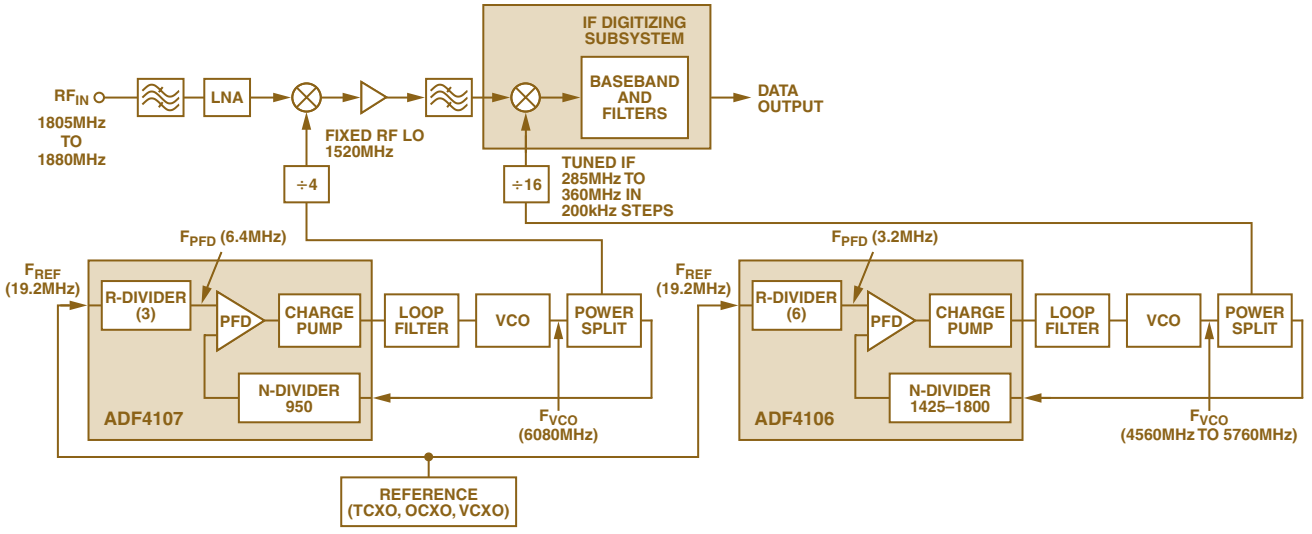

Figure 2. Alternative receiver block diagram

Using a loop bandwidth of 20 kHz, typical lock time to 10 degrees of phase error would be 250 µs.

Alternative Receiver Implementation

A new high-bandwidth PLL synthesizer, the ADF4107, is now available from ADI. Its RF stage is capable of operating at frequencies up to 7.0 GHz, while the PFD frequency is capable of operating at up to 104 MHz. This high-bandwidth capability can be used to implement novel receiver architectures, such as that shown in Figure 2. Here, the LO for each stage is derived from a higher frequency that is an integer multiple of the required frequency. In addition, the tuning is done in the IF section. This allows a very high multiple to be used, for an improvement in overall phase noise and lock time.

Fixed RF

In Figure 2, a fixed-frequency RF LO converts the signal down to the IF-band, and the channel is tuned in the IF-band. Again using the DCS1800 example, we can choose a fixed RF LO of 1520 MHz. This can be derived from a 6080-MHz signal by dividing by 4, as shown in Figure 2.

The phase noise of the RF LO will be:

$$\begin{aligned} &-219 + 20 \log 950 + 10 \log (6.4 \times 10^6) - 20 \log 4 \\ &= -219 + 59.5 + 68 - 12 \\ &= -103.5 \text{ dBc/Hz} \end{aligned}$$

The reference spurs will occur at 6.4 MHz offset from the carrier and will be very small (< –90 dBc), because (a) there will be 12 dB of attenuation due to the divide-by-4 circuit, and (b)—since this is a fixed-frequency LO—the loop bandwidth can be made low (say 20 kHz). A simple 20-dB/decade attenuation will give even further attenuation of the spurs.

There will be no spurs at 200 kHz, 400 kHz, 600 kHz, and 800 kHz; and lock time is not an issue, since no tuning occurs in the fixed-RF section.

Tuned IF

Continuing with the DCS1800 example, Figure 2 shows a tuned IF going from 285 MHz to 360 MHz in 200-kHz steps. To implement this, a PFD frequency of 3.2 MHz is used, producing an initial LO that goes from 4560 MHz to 5760 MHz, in 3.2-MHz steps. Dividing these frequencies by 16 gives the desired 285 MHz to 360 MHz in 200-kHz steps.

The worst-case phase noise of the tuned IF will be:

$$\begin{aligned} &-219 + 20 \log 1800 + 10 \log (3.2 \times 10^6) - 20 \log 16 \\ &= -219 + 65 + 65 - 24 \\ &= -113 \text{ dBc/Hz} \end{aligned}$$

Reference spurs will occur at a 3.2-MHz offset from the carrier. By choosing a loop bandwidth of 500 kHz, the spurs at 3.2 MHz will be below –90 dBc. In a DCS system, the important frequencies for spur reduction are 200 kHz, 400 kHz, 600 kHz, and 800 kHz. However, spurs will not exist at these frequencies in the proposed configuration, since we are operating at the high PFD frequency of 3.2 MHz.

With the loop bandwidth set at 500 kHz and the PFD frequency at 3.2 MHz, phase lock to within 10 degrees will occur in less than 10 µs. The frequency lock response is shown in Figure 3.

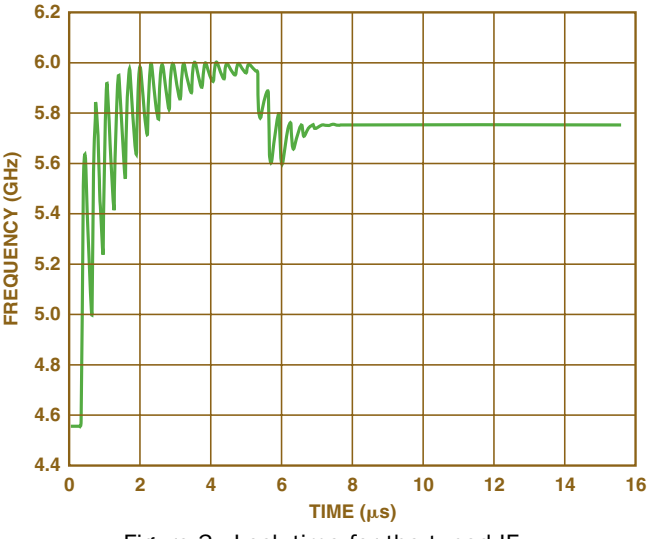

Figure 3. Lock time for the tuned IF.

Filtering Considerations

Both of the architectures considered are essentially superheterodyne, with two stages of downconversion. Filtering is critical in each of the stages.

In Figure 1, the RF filter that precedes the LNA rejects the very strong out-of-band interferers. The IF filter can be narrow-band (200 kHz in GSM) to reject the in-band interferers.

In Figure 2, the RF filter is the same as in Figure 1. However, the IF filter of Figure 2 cannot be narrow-band. It must pass the full band, since tuning has yet to occur. This means that the in-band interferers will have to be filtered later in the chain, as part of the baseband processing. Several IF-to-baseband receivers are available from ADI. These include the AD6650, AD6652, AD9870, and AD9874. They should be carefully considered when analyzing the architecture of Figure 2.

CONCLUSION

Operating the core of a PLL at a higher PFD frequency (an integer multiple of the final LO frequency) provides improved phase noise, output reference spurs, and lock time. Furthermore, a tuned-IF architecture provides even higher performance, as the integer multiple can be higher. However, filtering requirements need to be carefully considered.

The example used in this proposal is for an integer-*N* PLL, the ADF4107, but the configuration is not limited to this. It is also quite feasible to realize similar gains using this configuration with a fractional-*N* architecture.

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Phase-Locked-Loop (PLL) RF Frequency Synthesizers—Single

ADI Model	2nd Source?	Maximum RF Input Frequency F_{IN} (MHz)	Phase Noise @ 1 kHz ΦN dBc/Hz, 200 kHz Channel Spacing	Phase Noise Frequency (MHz)	Maximum REFIN Frequency (MHz)	RF Prescalers	Power Consumption (mA)	Package
ADF4001BRU	Proprietary	200	–99	200	100		4.5	TSSOP-16
ADF4001BCP	Proprietary	200	–99	200	100		4.5	CSP-20
ADF4110BRU	Proprietary	550	–91	540	100	8/9 16/17 32/33 64/65	4.5	TSSOP-16
ADF4110BCP	Proprietary	550	–91	540	100	8/9 16/17 32/33 64/65	4.5	CSP-20
ADF4111BRU	Proprietary	1200	–87	900	100	8/9 16/17 32/33 64/65	4.5	TSSOP-16
ADF4111BCP	Proprietary	1200	–87	900	100	8/9 16/17 32/33 64/65	4.5	CSP-20
ADF4112BRU	Proprietary	3000	–90	900	100	8/9 16/17 32/33 64/65	6.5	TSSOP-16
ADF4112BCP	Proprietary	3000	–90	900	100	8/9 16/17 32/33 64/65	6.5	CSP-20
ADF4113BRU	Proprietary	4000	–91	900	100	8/9 16/17 32/33 64/65	8.5	TSSOP-16
ADF4113BCP	Proprietary	4000	–91	900	100	8/9 16/17 32/33 64/65	8.5	CSP-20
ADF4106BRU	Proprietary	6000	–93	900	250	8/9 16/17 32/33 64/65	13	TSSOP-16
ADF4106BCP	Proprietary	6000	–93	900	250	8/9 16/17 32/33 64/65	13	CSP-20
ADF4107BCP	Proprietary	7000	–93	900	250	8/9 16/17 32/33 64/65	14	CSP-20
ADF4107BRU	Proprietary	7000	–93	900		8/9 16/17 32/33 64/65	14	CSP-20
ADF4116BRU	LMX2306TM	550	–89	540	100	8/9	4.5	TSSOP-16
ADF4117BRU	LMX2316TM	1200	–87	900	100	32/33	4.5	TSSOP-16
ADF4118BRU	LMX2326TM	3000	–90	900	100	32/33	6.5	TSSOP-16
ADF4153BRU	Proprietary	4000	–103	1740	150	4/5 8/9	12	TSSOP-16
ADF4153BCP	Proprietary	4000	–103	1740	150	4/5 8/9	12	CSP-20

For additional synthesizer types or an updated chart, see http://www.analog.com/analog_root/static/pdf/RFComms/SelectionGuides/phase.pdf