Encoder's Spare Channel Embeds Whole-House Stereo Audio in Satellite Set-Top-Box Designs Stably and Cost-Effectively

By Jeritt Kent [jeritt.kent@analog.com] and
Victor Chang

INTRODUCTION

Satellite set-top boxes (STBs) and television receivers contain a number of chips that require high-speed clocks. If the video decoder chip does not have an external clock drive—and many newer devices do not—a clock must be indirectly generated for any audio components that require it. This article shows how a *phase-locked loop* (PLL) can be used to derive a stable high-speed clock for a *Broadcast-Television-Systems-Committee* (BTSC) stereo-enabled system, employing a dual-channel BTSC encoder, such as the AD71028.[1]

One channel of the encoder handles the actual BTSC stereo-encoded output, and the second channel serves to derive both the primary channel's master clock and its own subsidiary clock—using the vestigial pilot signal in the BTSC composite audio spectrum plus negative-feedback error correction. With the AD71028 used in this way, stereo capability can be added inexpensively when designing a satellite STB. For the consumer, this means that in homes where TVs and *audio/video* (A/V) receivers are in multiple rooms, BTSC stereo can be fed throughout the house via coaxial cables, avoiding the high cost and low noise immunity of RCA audio/video cables.

This article describes the clock-generation problem in the set-top-box environment—and then shows a compact, low-cost solution that both generates a stable system master clock and derives a clock for the stereo audio distribution system.

Multi-channel television sound (MTS), better known as BTSC encoding—developed by Zenith—was adopted by the U.S. *Federal Communications Commission* (FCC) in 1984 as the method for encoding three additional audio channels onto *National Television Systems Committee* (NTSC) format video signals. Early NTSC video already included a monophonic audio signal (equivalent to L + R, stereo-sum), so BTSC added the stereo difference signal (L – R), which is combined with the sum signal to decode stereo audio. In addition, a second channel, known as *second audio program* (SAP), is available to provide a second language, an audio description service for the visually impaired, or radio service. A third—*professional* (PRO)—channel may be used by the broadcasting station for audio or data exchange.

Frequency plots of NTSC composite video and BTSC composite audio spectra are shown in Figures 1 and 2, respectively. Note that the BTSC spectrum incorporates a pilot signal at 15.734 kHz, which is the same frequency as the NTSC video horizontal sync, 1H = f_{Hsync}. This pilot signal is used by the receiver to recover the *double-sideband suppressed-carrier* (DSBSC) modulated stereo-difference (L – R) audio channel at 2H, and the SAP and PRO channels at 5H and 6.5H. It is important to note that DSBSC modulation requires *coherent* demodulation, so phase and frequency must be identical at both transmit and receive points to avoid severe distortion.

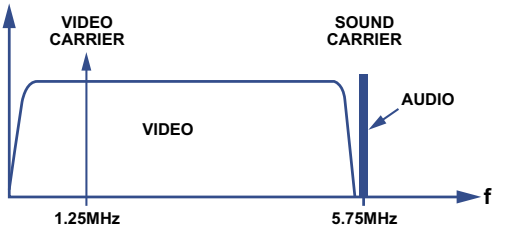

Figure 1. NTSC spectrum for a television channel.

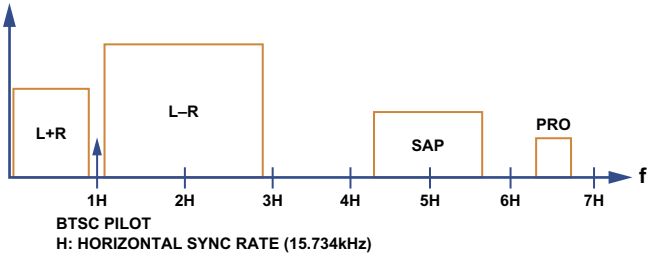

Figure 2. Audio spectrum defined by BTSC.

In receiver designs, a *phase-locked loop* (PLL) is used in the *local oscillator* (LO) to eliminate frequency- and phase offsets due to environmental effects—such as ambient temperature changes. Since these offsets cause errors in down-conversion and demodulation, standalone oscillators are inadequate because they track neither frequency nor phase. A typical PLL contains a low-drift reference oscillator and a *voltage-controlled oscillator* (VCO) that provides frequency tuning. Using negative feedback, a low drift output is generated from the reference input. Because f_{Hsync} can be used as a low-drift reference signal, a PLL can be used to generate the master clock for the BTSC encoder and *analog-to-digital converter* (ADC). The traditional method uses a PLL to produce a master clock, but the circuit presented here uses an unusual technique: it incorporates a device that *requires* a master clock into the PLL feedback loop that *generates* the master clock.

In its most basic form, the PLL consists of a phase detector, loop filter, and VCO, as shown in Figure 3. The phase detector compares the phase of the reference signal to the feedback signal, and produces a slowly varying output as a function of the difference. The phase detector's output is filtered to provide a clean control voltage for the VCO. The VCO output is fed back to the phase detector, and the negative feedback forces the VCO to generate a frequency equal to the reference frequency at equilibrium. Shifts in the frequency or phase (rate-of-change of frequency) of the reference signal will be tracked by the phase detector. The filtered output of the phase detector drives the VCO, causing it to follow the reference frequency. When the VCO output frequency and phase are equal to the reference signal, the PLL is said to be in a "locked" condition.

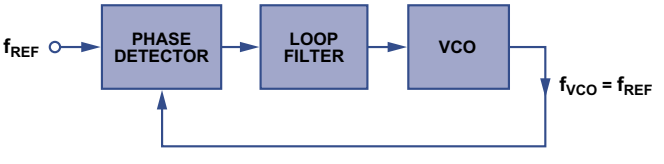

Figure 3. Basic PLL system.

With slight modifications, this basic PLL principle can be applied in many useful ways. For instance, by adding a frequency divider in the loop (for example, a modulo-N counter), as shown in Figure 4, the basic PLL becomes a stable and tunable frequency synthesizer, which generates a VCO output frequency that may be an integer- or fractional multiple of the input reference frequency, $f_{VCO} = N \times f_{REF}$.

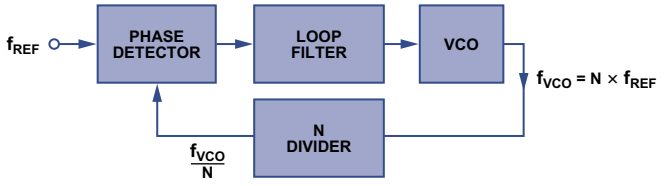

Figure 4. PLL frequency synthesizer. When the loop settles, $f_{VCO} = N \times f_{REF}$.

STBs and television receivers contain multiple chips that require high-speed clocks. *Moving-Picture-Experts-Group* (MPEG) based receivers, for example, use a 27-MHz master clock that must be routed to the supplemental audio components. The source of this clock is often the MPEG decoder chip, but if the MPEG decoder does not provide it externally, it must be generated elsewhere. The following application in a BTSC-enabled system employs PLL principles to use an AD71028 dual-channel BTSC encoder as the fractional divider that derives a stable, high-speed, frequency- and phase-locked clock. One channel of the encoder is used for the BTSC stereo-encoded output, while the second channel is used with negative feedback to derive the master clock for both the primary channel and for the encoder itself.

In this application, the AD71028 inexpensively adds stereo capability to satellite STBs without the need for a 27-MHz clock source. In homes where TVs and *audio/video receivers* (AVRs) are used in various rooms, this technique allows the BTSC stereo signal to be passed throughout the house via coaxial cable, avoiding the high cost, poor stereo separation, and low noise immunity of unbalanced RCA cables. This simplified approach can be used because the vestigial 15.734-kHz pilot signal in the BTSC composite audio spectrum provides an ideal reference signal to the phase detector of the PLL.

The RF outputs of *cable*-TV set-top boxes (modulated on Channel 3 or Channel 4) are already BTSC stereo encoded. However, the RCA outputs of inexpensive *satellite* TV set-top boxes are often limited to monophonic sound. To add stereo capability to a satellite STB, an AD71028 BTSC stereo encoder is added to the system. In homes with multiple TVs, an ADC is required in the primary satellite STB to convert the left- and right analog audio signals to digital before encoding. A master clock is required for the AD71028, the ADC, and other professional audio converters and components. These components have a quasi-standard sample rate of 48 kHz, but are typically oversampled at 12.288 MHz (48 kHz × 256). With a 12.288-MHz master clock and digitized L and R audio channels, the encoder will generate the main monaural channel (L + R), the BTSC stereo subchannel (L – R), and the 15.734-kHz pilot signal.

The master clock, which, in turn, generates a fractionally proportional pilot signal, can be generated in one of several ways. One option, the use of a crystal-based oscillator, will not ensure that the corresponding BTSC pilot signal is frequency- or phase-locked to f_{Hsync}, a requirement to accurately decode the double-sideband suppressed-carrier-encoded stereo audio. At the remote television, video signals can be as much as 10 dB higher than the audio, potentially causing phase alignment errors in the stereo matrix decoding. In addition, even the best available highly stable crystals are only specified to 0.01%, corresponding to a 1.6 Hz tolerance in the pilot signal. For example, if the PLL in the BTSC receiver were to lock on to a strong artifact of the NTSC f_{Hsync}, instead of the crystal-generated pilot, the signal differences will result in time-varying phase misalignment between L + R and L – R, causing a severe loss of separation between the left and right channels during decode. Also, depending on the architecture of the phase detector, the VCO may vacillate between the crystal-generated pilot and the f_{Hsync} artifact, again resulting in phase misalignment.

A more viable option is to derive a clock with a fractional-N PLL, actually using the f_{Hsync} as a reference input. Figure 5 shows a typical PLL with a fractional-N divider in its feedback path. If f_{Hsync} is used as the input reference, the value of the N divider is 780.9838... ($N = f_{MCLK}/f_{Hsync}$) requiring a very high resolution device. This approach also requires additional components, making it impractical in designs where board space is at a premium.

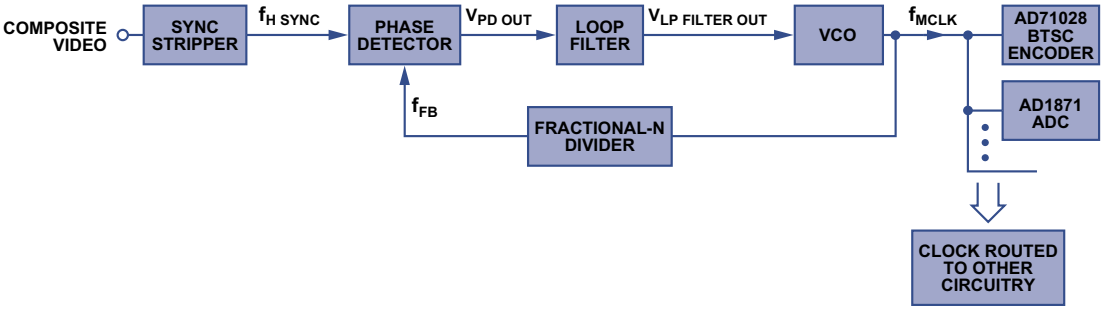

Figure 5. Typical MCLK derivation using a PLL. The fractional-N divider is set so that MCLK is 12.288 MHz.

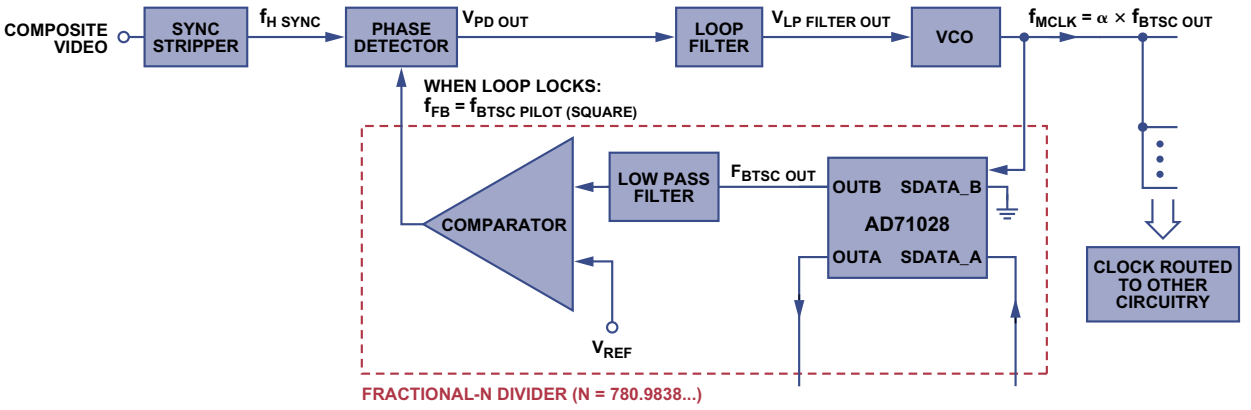

Figure 6. f_{MCLK} synthesis with H-sync and BTSC pilot. Observe how the AD71028 is incorporated in the feedback loop of the PLL

A third option is to include the secondary channel of the AD71028—which contains two stereo audio channels—in the feedback loop, using it to self-correct and self-sustain the master clock—as shown in Figure 6. The primary (A) channel of the AD71028 is used for encoding BTSC stereo audio. It receives its digital inputs from an audio ADC, such as the AD1871. If the audio inputs of the secondary (B) channel are grounded, only the vestigial pilot is seen at the output. If phase- and frequency-locked to f_{Hsync}, this signal can be used to generate the 12.288-MHz master clock, f_{MCLK}.

After the B-channel output of the encoder, a two-pole, low-pass filter and a biased comparator are needed to provide a clean square wave pilot signal to the phase detector. Any errors in the AD71028's master-clock frequency will be reflected immediately through the secondary channel to the phase detector's feedback input via the vestigial pilot, which is directly proportional to f_{MCLK}. Thus, this BTSC pilot feedback clock-synthesis method will provide a more accurate master clock than a conventional fractional-N PLL clock, since the master clock will be generated directly with the correct frequency feedback ratio. In this application, the PLL concept is successful because the AD71028 core is able to generate the pilot tone digitally at a fixed fractional ratio to the f_{MCLK}.

Thus, the master clock frequency must be precisely 12.288 MHz for the pilot tone to be 15.734 kHz. When the loop settles and locks, f_{MCLK} will be a fractional multiple of the instantaneous frequency of the BTSC encoder output, $f_{btsc\ out}$ (that is, $f_{MCLK} = \alpha \times f_{btsc\ out}$), and the pilot sent to the remote television is locked to the NTSC f_{Hsync}. Coupled artifacts of f_{Hsync} at the receiver are identical in phase and frequency to the pilot, so there is no erroneous demodulation.

When two TVs are connected to one satellite STB using a simple STB, the TV in a distant room must be connected via coaxial cable. The satellite dish is connected directly to the STB, via ANT IN, as shown in Figure 7. The audio signal is routed to the main TV via RCA cables, and the second TV receives its audio and video on channel 3 or 4 via coaxial cable. The second TV will receive only monophonic sound, though, because the stereo difference signal, L – R, is not present in the audio spectrum it receives (Figure 8).

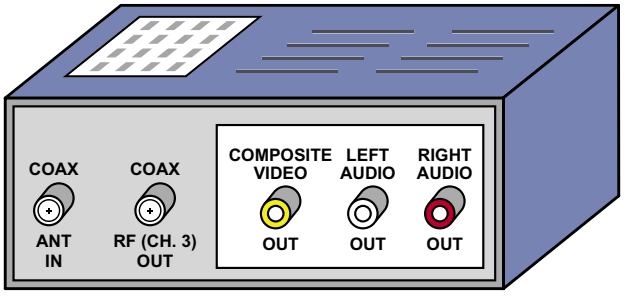

Figure 7. A/V inputs and outputs of a satellite STB.

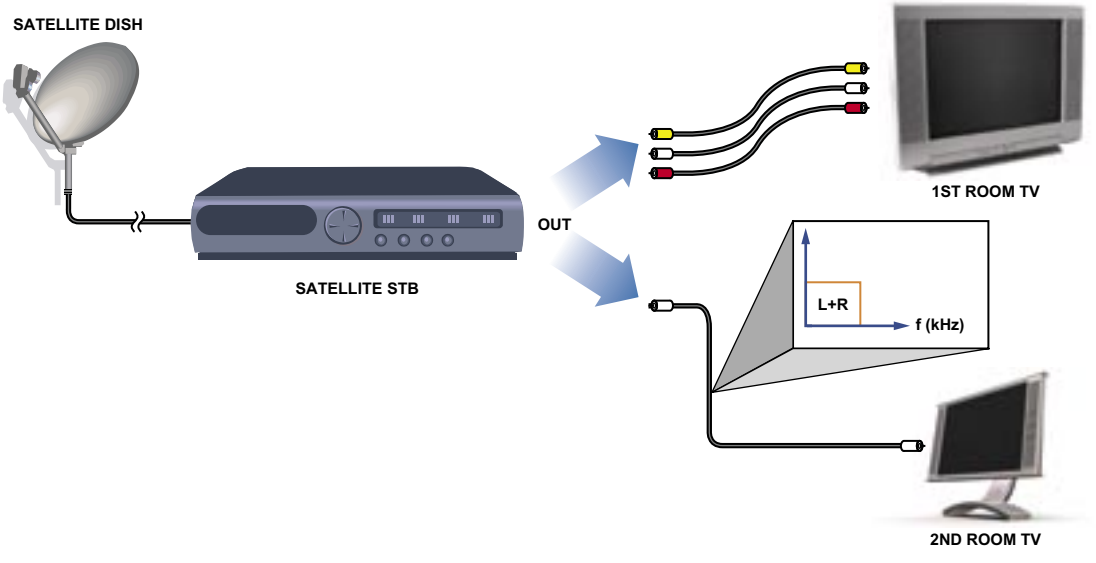

Figure 8. Audio spectrum of typical satellite TV setup where monaural audio is sent to 2nd room TV

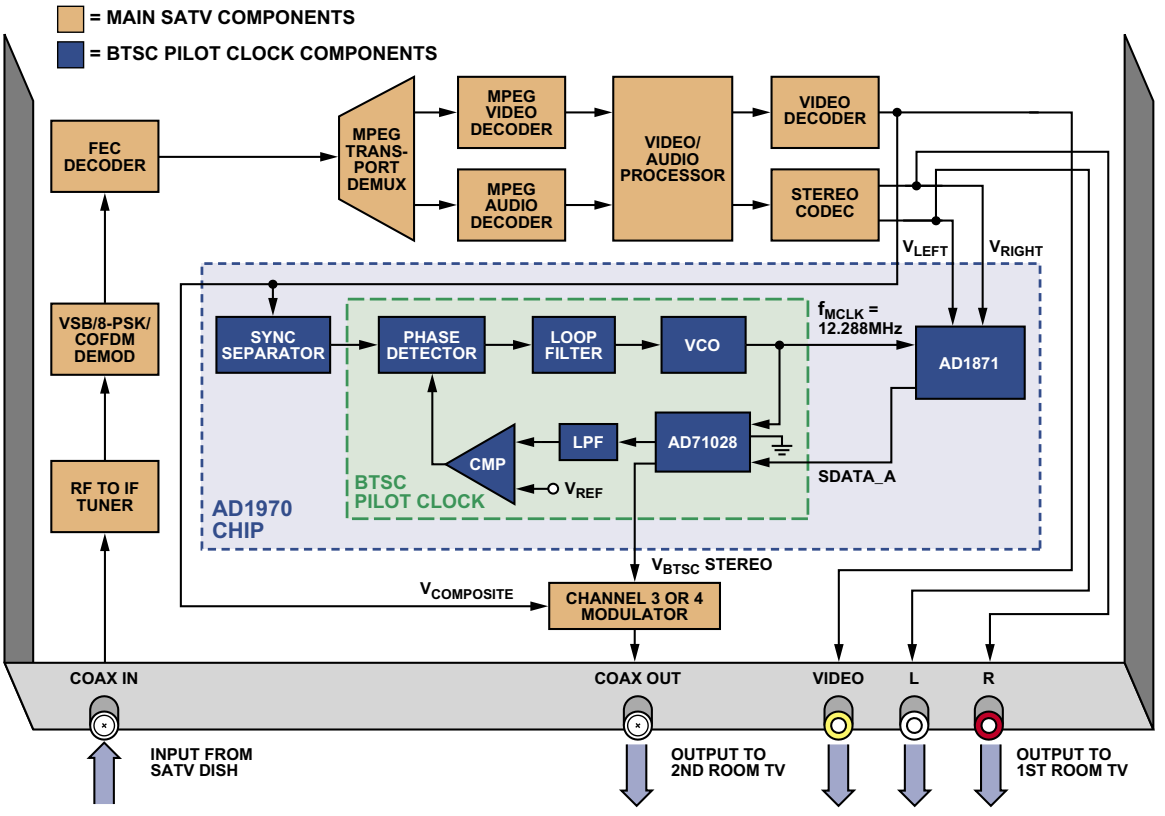

Figure 9. Block diagram of SATV receiver. MCLK is derived using a BTSC pilot. The AD71028's A channel output can be used to provide BTSC stereo to a second room TV or secondary A/V receivers.

The reason for this is that BTSC encoders have traditionally been expensive because designs require many analog components, a large board space, and complex calibration adjustments, making them impractical for low-cost satellite STBs. If one desires to preserve stereo sound in such a system, the decoded left and right analog audio signals must be passed to the second (remote) TV via extended unbalanced RCA cables, paralleled with the L and R cables shown in Figure 8, but this setup is highly susceptible to noise and signal degradation.

If, on the other hand, the AD71028, a dual-channel BTSC stereo encoder, is used as described above, its A channel can be used for passing encoded video and stereo audio to a second TV via a single coaxial cable. In homes where TVs and audio/video receivers may be in multiple rooms, the consumer can now pass BTSC stereo throughout the house via coaxial cable.

Figure 9 shows a block diagram of a *satellite-access-TV* (SATV) receiver. It has an RF output with BTSC stereo and a PLL-generated MCLK.

Digital BTSC Encoder Including ADC

The recently released AD1970[2] incorporates the AD71028[1] BTSC encoder and the AD1871[3] ADC. The required inputs to this device are the NTSC composite video signal and L and R audio channels.

Since the clock is self-generated with the concealed secondary channel in the core, no external clock is needed to drive this part. The AD1970 thus offers a fully integrated solution for BTSC-enabled satellite STB applications.

CONCLUSION

A novel application of a phase-locked loop provides an accurate, low-drift, self-correcting master clock for satellite set-top boxes. A BTSC pilot from the secondary channel of a dual BTSC encoder is continuously compared with the NTSC horizontal sync rate (15.734 kHz) to derive a self-sustaining stable master clock frequency of 12.288 MHz. This clock can be routed to other professional audio converters and components, and it can be used as a source for deriving further clock frequencies. In addition, the primary channel of the encoder provides a BTSC stereo-encoded output. This allows secondary TVs and A/V receivers to be interconnected via single standard coaxial cables. In TV and A/V setups where devices are far apart, this approach maintains the signal integrity of the system cost-effectively.

REFERENCES—VALID AS OF JULY 2005

[1] ADI website: www.analog.com (Search) AD71028 (Go)
[2] ADI website: www.analog.com (Search) AD1970 (Go)
[3] ADI website: www.analog.com (Search) AD1871 (Go)