19-5714; Rev 1; 3/11

备有评估板

6通道数字电平转换器

MAX14842

概述

MAX14842能够在两个参考地电位相差最高72V的电路之间进行数字信号转换。器件集成了六个传输通道：两个双向通道和四个单向通道。四个单向通道在每个方向分别提供两个通道。器件由两路电源供电，分别定义相对于各自地平面的逻辑电平。

MAX14842的四个单向通道可支持高达30Mbps的数据速率，两个双向通道支持2Mbps的数据速率。双向通道提供开漏输出，适用于I²C信号。双向通道支持I²C时钟扩展和热插拔。

欠压锁定确保在上电、断电及电源变化时，输出引脚具有确定动作。必须保证0V ≤ (V_{GNDB} – V_{GNDA}) ≤ 72V，使器件保持正常工作。注意，GNDB必须大于或等于GNDA。

MAX14842采用16引脚TQFN封装，工作在-40°C至+125°C汽车级温度范围。

定购信息

PART	TEMP RANGE	PIN-PACKAGE
MAX14842ATE+	-40°C to +125°C	16 TQFN-EP**

***EP = 裸焊盘。*

+表示无铅(Pb)/符合RoHS标准的封装。

特性

- 允许高达72V的地电位差
- 四路单向通道：两路输入/两路输出
- 两路双向通道
- I²C兼容
- 支持I²C时钟扩展
- 30Mbps单向通道数据速率
- 2Mbps双向通道数据速率
- +3.3V至+5V电平转换
- 欠压锁定
- 4mm x 4mm、16引脚TQFN封装
- -40°C至+125°C汽车级温度范围

应用

电信系统

电池管理

I²C、SMBus™、SPI™以及MICROWIRE™信号

医疗系统

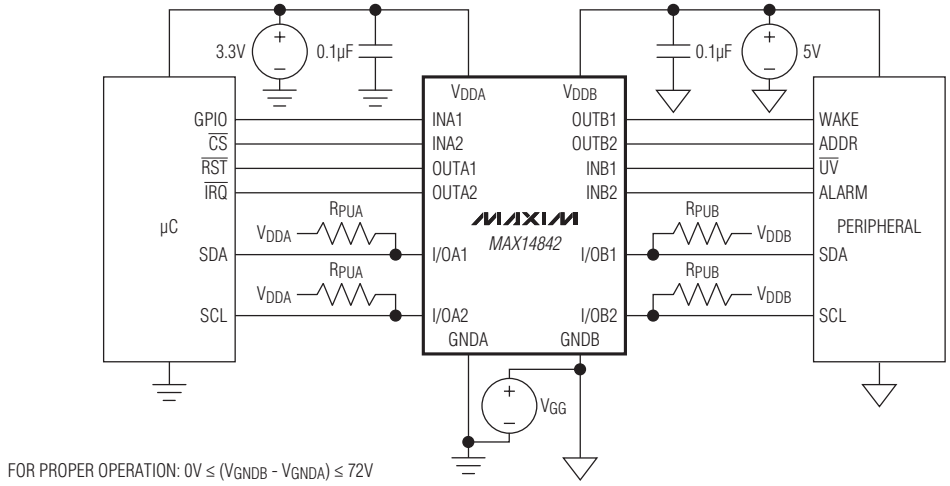
以太网供电

SMBus是Intel Corp.的商标。

SPI是Motorola, Inc.的商标。

MICROWIRE是National Semiconductor Corp.的商标。

典型工作电路



ABSOLUTE MAXIMUM RATINGS

V_{DDA} to GNDA .....-0.3V to +6V
V_{DDB} to GNDB .....-0.3V to +6V
GNDB to GNDA.....-0.3V to +80V
INA1, INA2 to GNDA..... -0.3V to (V_{DDA} + 0.3V)
INB1, INB2 to GNDB..... -0.3V to (V_{DDB} + 0.3V)
OUTA1, OUTA2 to GNDA ..... -0.3V to (V_{DDA} + 0.3V)
OUTB1, OUTB2 to GNDB ..... -0.3V to (V_{DDB} + 0.3V)
I/OA1, I/OA2 to GNDA .....-0.3V to +6V
I/OB1, I/OB2 to GNDB .....-0.3V to +6V
Common-Mode Transients (i.e., Transients Between GNDA and GNDB)..... 10V/µs
Short-Circuit Duration (OUTA1, OUTA2 to GNDA; OUTB1, OUTB2 to GNDB).....Continuous
Continuous Power Dissipation (T_A = +70°C)
TQFN (derate 25mW/°C above +70°C).....2000mW
Operating Temperature Range..... -40°C to +125°C
Junction Temperature .....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

PACKAGE THERMAL CHARACTERISTICS (Note 1)

TQFN
Junction-to-Ambient Thermal Characteristics (θ_{JA}) ....40°C/W
Junction-to-Case Thermal Characteristics (θ_{JC}) .....6°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **china.maxim-ic.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DDA} - V_{GNDA} = +3.0V to +5.5V, V_{DDB} - V_{GNDB} = +3.0V to +5.5V, V_{GNDB} - V_{GNDA} = 0 to +72V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = +3.3V, V_{DDB} - V_{GNDB} = +3.3V, V_{GNDB} - V_{GNDA} = +50V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
DC CHARACTERISTICS						
Supply Voltage	V_{DDA}	Relative to GNDA	3.0		5.5	V
	V_{DDB}	Relative to GNDB	3.0		5.5	
Supply Current	I_{DDA} I_{DDB}	V_{DDA} - V_{GNDA} = +5.5V; V_{DDB} - V_{GNDB} = +5.5V; V_{GNDB} - V_{GNDA} = +70V; all inputs at V_{GNDA}, V_{GNDB}, or +5.5V; no load			7.5	mA
Voltage Between GNDB and GNDA	V_{GG}	V_{GNDB} - V_{GNDA}	0		72	V
Side B Leakage Current	I_L				1	mA
Undervoltage-Lockout Threshold	V_{UVLO}	V_{DDA} - V_{GNDA}, V_{DDB} - V_{GNDB}		2		V
Undervoltage-Lockout Hysteresis	$V_{UVLOHYS}$	V_{DDA} - V_{GNDA}, V_{DDB} - V_{GNDB}		0.1		V
LOGIC INPUTS AND OUTPUTS						
Input Logic Threshold Voltage	V_{IT}	I/OA1, I/OA2, relative to GNDA	0.5		0.7	V
Input Logic-High Voltage	V_{IH}	INA1, INA2, relative to GNDA	0.7 x V_{DDA}			V
		INB1, INB2, relative to GNDB	0.7 x V_{DDB}			
		I/OA1, I/OA2, relative to GNDA	0.7			
		I/OB1, I/OB2, relative to GNDB	0.7 x V_{DDB}			

ELECTRICAL CHARACTERISTICS (continued)

(V_{DDA} - V_{GNDA} = +3.0V to +5.5V, V_{DDB} - V_{GNDB} = +3.0V to +5.5V, V_{GNDB} - V_{GNDA} = 0 to +72V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = +3.3V, V_{DDB} - V_{GNDB} = +3.3V, V_{GNDB} - V_{GNDA} = +50V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Input Logic-Low Voltage	V_{IL}	INA1, INA2, relative to GNDA			0.8	V
		INB1, INB2, relative to GNDB			0.8	
		I/OA1, I/OA2, relative to GNDA			0.5	
		I/OB1, I/OB2, relative to GNDB			0.3 x V_{DDB}	
Output Logic-High Voltage	V_{OH}	OUTA1, OUTA2, relative to GNDA, source current = 4mA	V_{DDA} - 0.4V			V
		OUTB1, OUTB2, relative to GNDB, source current = 4mA	V_{DDB} - 0.4V			
Output Logic-Low Voltage	V_{OL}	OUTA1, OUTA2, relative to GNDA, sink current = 4mA			0.8	V
		OUTB1, OUTB2, relative to GNDB, sink current = 4mA			0.8	
		I/OA1, I/OA2, relative to GNDA, sink current = 10mA	0.6		0.9	
		I/OA1, I/OA2, relative to GNDA, sink current = 0.5mA	0.6		0.85	
		I/OB1, I/OB2, relative to GNDB, sink current = 30mA			0.4	
Input/Output Logic-Low Threshold Difference	ΔV_{TOL}	I/OA1, I/OA2 (Note 3)	50			mV
Input Leakage Current	I_L	V_{INA1}, V_{INA2}, V_{DDA} = +3.6V, V_{INB1},V_{INB2}, V_{DDB} = +3.6V	-2		+2	µA
		$V_{I/OA1}$, $V_{I/OA2}$, V_{DDA} = +3.6V, $V_{I/OB1}$, $V_{I/OB2}$, V_{DDB} = +3.6V	-2		+2	
Input Capacitance	C_{IN}	INA1, INA2, INB1, INB2, f = 1MHz (Note 4)		4		pF
DYNAMIC SWITCHING CHARACTERISTICS						
Maximum Data Rate	DR_{MAX}	INA1 to OUTB1, INA2 to OUTB2, INB1 to OUTA1, INB2 to OUTA2	30			Mbps
		I/OA1 to I/OB1, I/OA2 to I/OB2, I/OB1 to I/OA1, I/OB2 to I/OA2	2			
Minimum Pulse Width	PW_{MIN}	INA1 to OUTB1, INA2 to OUTB2, INB1 to OUTA1, INB2 to OUTA2	30			ns
Propagation Delay	t_{DPLH} t_{DPHL}	INA1 to OUTB1, INA2 to OUTB2, INB1 to OUTA1, INB2 to OUTA2, V_{DDA} = V_{DDB} = +3.0V, R_L = 1MΩ, C_L = 15pF, Figure 1		20	30	ns
	t_{DPLH} t_{DPHL}	I/OA1 to I/OB1, I/OA2 to I/OB2, V_{DDA} = V_{DDB} = +3.0V, R_1 = 1.6kΩ, R_2 = 180Ω, C_{L1} = C_{L2} = 15pF, Figure 2		30	100	
	t_{DPLH} t_{DPHL}	I/OB1 to I/OA1, I/OB2 to I/OA2, V_{DDA} = V_{DDB} = +3.0V, R_1 = 1kΩ, R_2 = 120Ω, C_{L1} = C_{L2} = 15pF, Figure 2		60	100	

ELECTRICAL CHARACTERISTICS (continued)

(V_{DDA} - V_{GNDA} = +3.0V to +5.5V, V_{DDB} - V_{GNDB} = +3.0V to +5.5V, V_{GNDB} - V_{GNDA} = 0 to +72V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = +3.3V, V_{DDB} - V_{GNDB} = +3.3V, V_{GNDB} - V_{GNDA} = +50V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Propagation Delay Skew $\lvert t_{DPLH} - t_{DPHL} \rvert$	t_{DSKEW}	I/OA1 to I/OB1, I/OA2 to I/OB2, V_{DDA} = V_{DDB} = +3.0V, R_1 = 1.6kΩ, R_2 = 180Ω, C_{L1} = C_{L2} = 15pF, Figure 2		3	6	ns
		I/OB1 to I/OA1, I/OB2 to I/OA2, V_{DDA} = V_{DDB} = +3.0V, R_1 = 1kΩ, R_2 = 120Ω, C_{L1} = C_{L2} = 15pF, Figure 2		30	100	
Channel-to-Channel Skew	$t_{DSKEWCC}$	OUTB1 to OUTB2 output skew, Figure 1		3	6	ns
		OUTA1 to OUTA2 output skew, Figure 1		3	6	
		I/OB1 to I/OB2 output low skew, Figure 2		3	10	
		I/OA1 to I/OA2 output low skew, Figure 2		3	10	
Rise Time	t_R	OUTB1, OUTB2, OUTA1, OUTA2, 10% to 90%, Figure 1			5	ns
Fall Time	t_F	OUTB1, OUTB2, OUTA1, OUTA2, 90% to 10%, Figure 1			5	ns
		I/OA1, I/OA2, 90% to 10%, V_{DDA} = V_{DDB} = +3.0V, R_1 = 1.6kΩ, R_2 = 180Ω, C_{L1} = C_{L2} = 15pF, Figure 2		30	60	
		I/OB1, I/OB2, 90% to 10%, V_{DDA} = V_{DDB} = +3.0V, R_1 = 1kΩ, R_2 = 120Ω, C_{L1} = C_{L2} = 15pF, Figure 2		3	6	

Note 2: All units are production tested at T_A = +25°C. Specifications over temperature are guaranteed by design. All voltages of side A are referenced to GNDA; all voltages of side B are referenced to GNDB, unless otherwise noted.

Note 3: ΔV_{TOL} = V_{OL} - V_{IL}. This is the minimum difference between the output logic-low voltage and the input logic threshold for the same I/O pin. This ensures that the I/O channels are not latched low when any of the I/O inputs are driven low (see the *Bidirectional Channels* section).

Note 4: Guaranteed by design; not production tested.

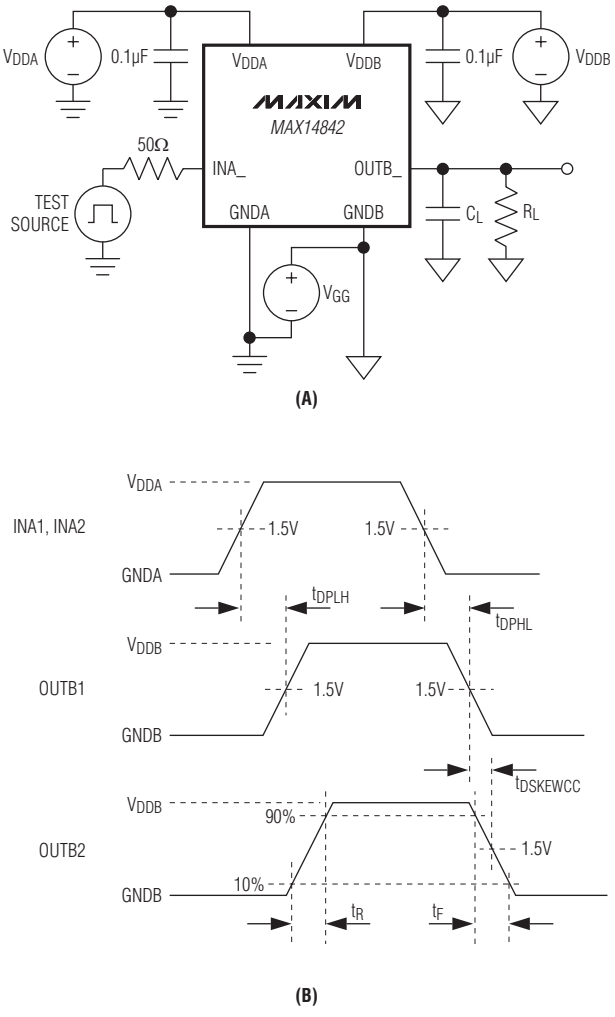


图1. 单向通道的测试电路(A)和时序图(B)

测试电路/时序图(续)

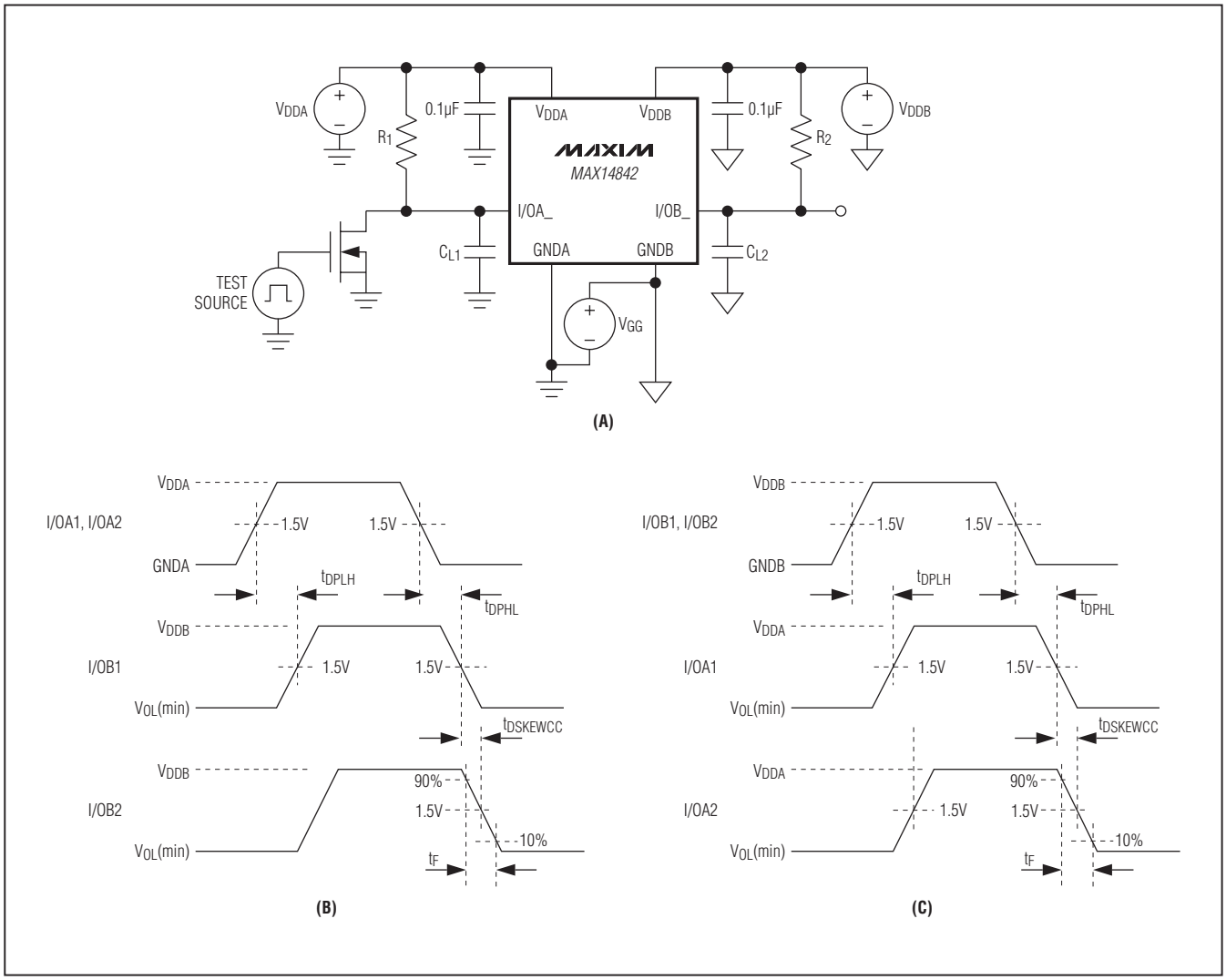
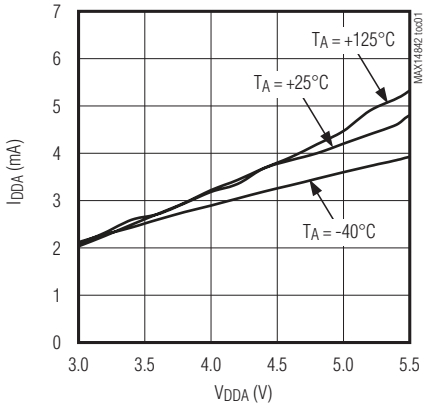


图2. 双向通道的测试电路(A)和时序图(B)及(C)

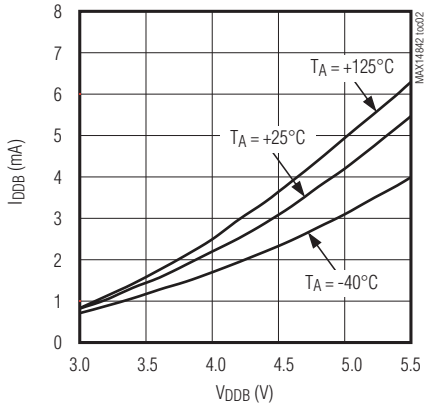
典型工作特性

(V_{DDA} - V_{GNDA} = +3.3V, V_{DDB} - V_{GNDB} = +3.3V, V_{GNDB} - V_{GNDA} = +50V, R_{PUA} = R_{PUB} = 2kΩ, C_L = 15pF, see the *Typical Operating Circuit*, T_A = +25°C, unless otherwise noted.)

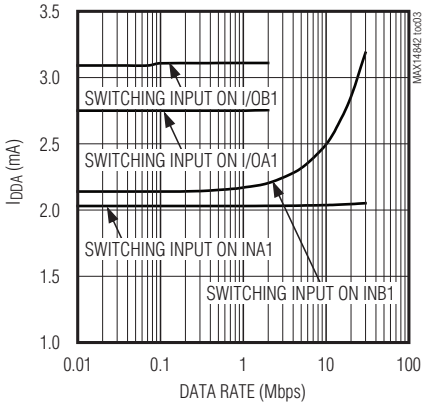
I_{DDA} vs. V_{DDA}



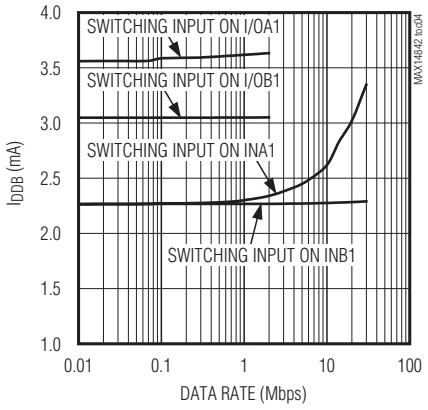
I_{DDB} vs. V_{DDB}



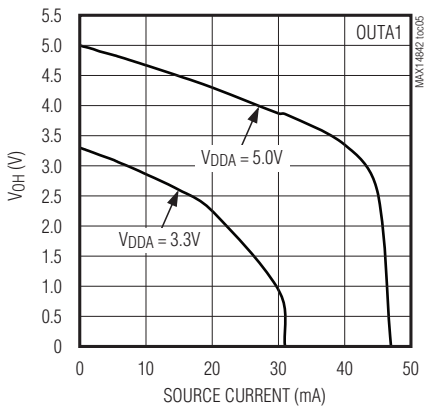
I_{DDA} vs. DATA RATE



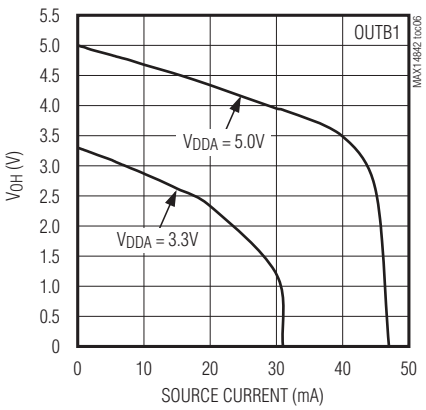
I_{DDB} vs. DATA RATE



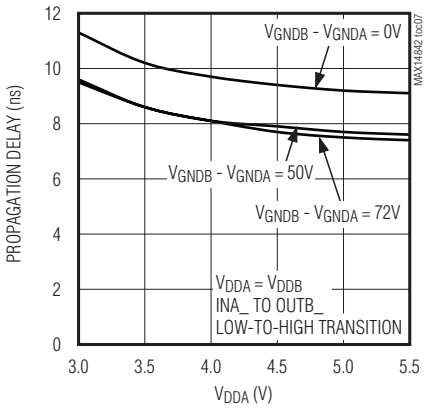
OUTPUT-VOLTAGE HIGH vs. SOURCE CURRENT



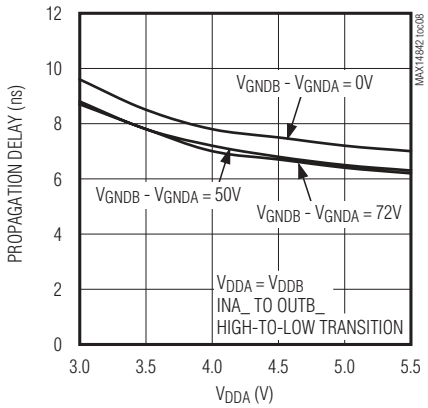
OUTPUT-VOLTAGE HIGH vs. SOURCE CURRENT



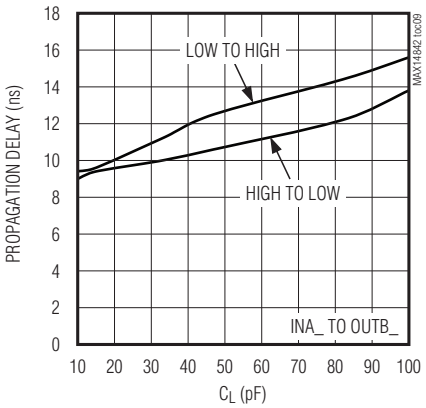
PROPAGATION DELAY vs. SUPPLY VOLTAGE



PROPAGATION DELAY vs. SUPPLY VOLTAGE



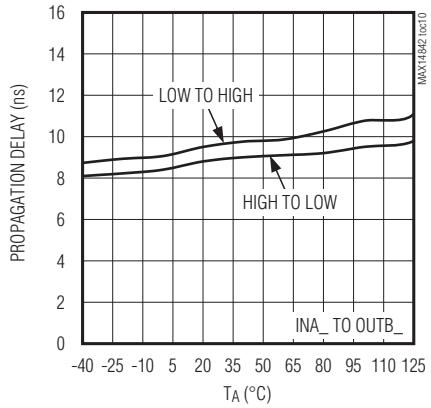
PROPAGATION DELAY vs. CAPACITIVE LOAD



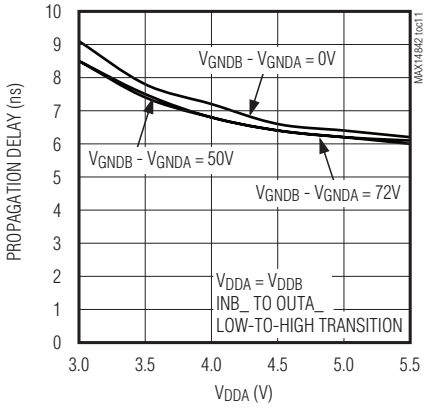
典型工作特性(续)

(V_{DDA} - V_{GNDA} = +3.3V, V_{DDB} - V_{GNDB} = +3.3V, V_{GNDB} - V_{GNDA} = +50V, R_{PUA} = R_{PUB} = 2kΩ, C_L = 15pF, see the *Typical Operating Circuit*, T_A = +25°C, unless otherwise noted.)

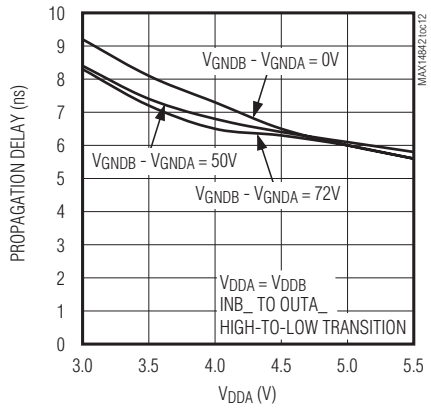
PROPAGATION DELAY vs. TEMPERATURE



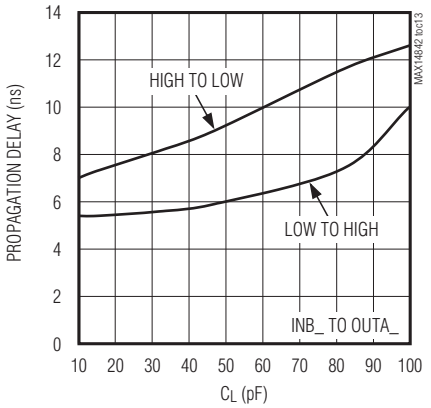
PROPAGATION DELAY vs. SUPPLY VOLTAGE



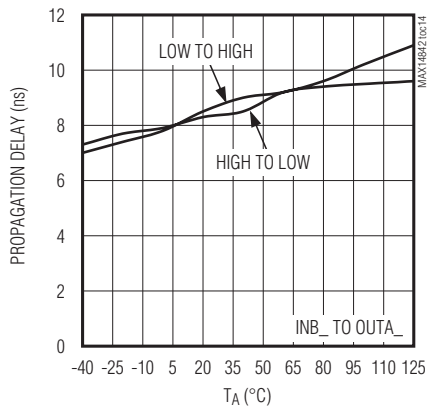
PROPAGATION DELAY vs. SUPPLY VOLTAGE



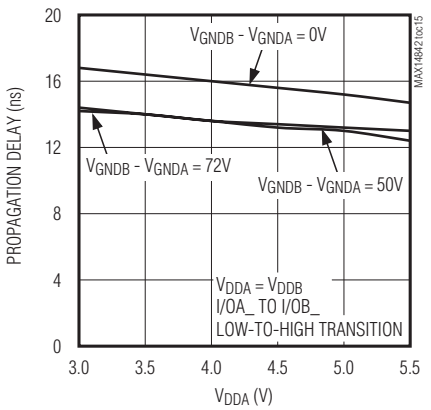
PROPAGATION DELAY vs. CAPACITIVE LOAD



PROPAGATION DELAY vs. TEMPERATURE



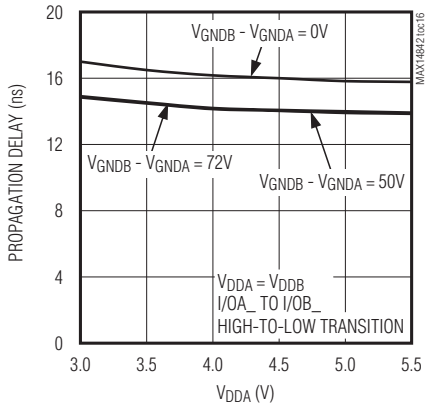
PROPAGATION DELAY vs. SUPPLY VOLTAGE



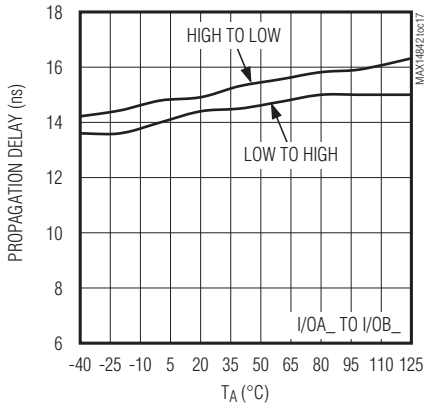
典型工作特性(续)

(V_{DDA} - V_{GNDA} = +3.3V, V_{DDB} - V_{GNDB} = +3.3V, V_{GNDB} - V_{GNDA} = +50V, R_{PUA} = R_{PUB} = 2kΩ, C_L = 15pF, see the *Typical Operating Circuit*, T_A = +25°C, unless otherwise noted.)

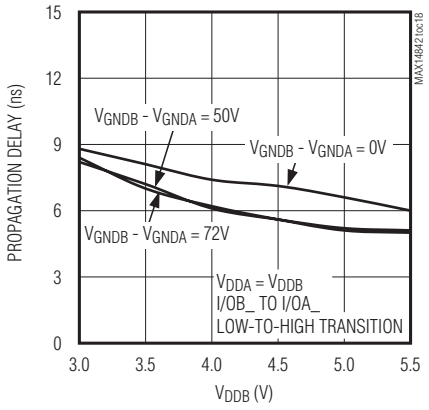
PROPAGATION DELAY vs. SUPPLY VOLTAGE



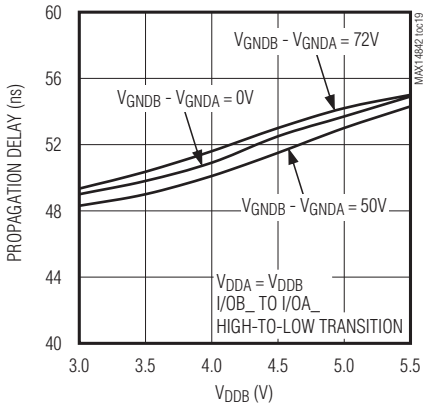
PROPAGATION DELAY vs. TEMPERATURE



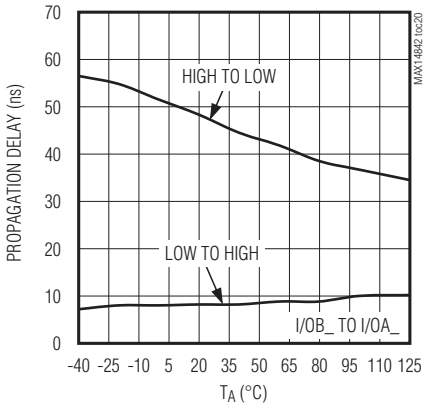
PROPAGATION DELAY vs. SUPPLY VOLTAGE



PROPAGATION DELAY vs. SUPPLY VOLTAGE

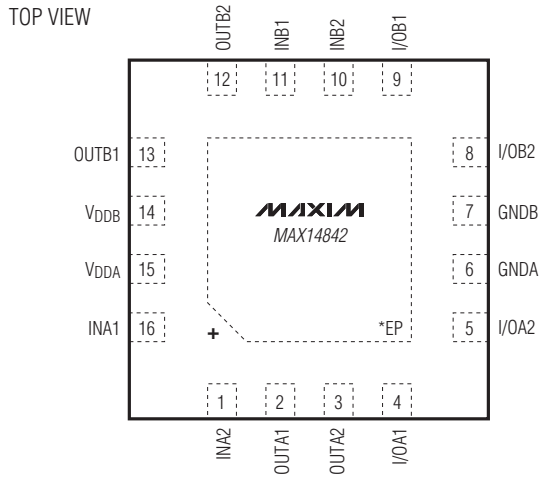


PROPAGATION DELAY vs. TEMPERATURE



6通道数字电平转换器

引脚配置



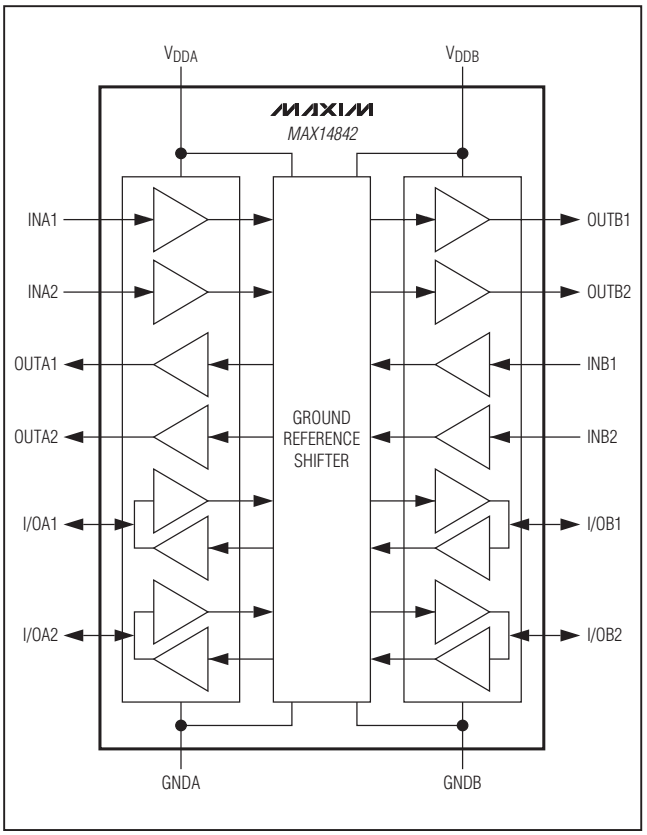
TQFN
(4mm × 4mm)

*CONNECT EXPOSED PAD TO GNDA.

引脚说明

引脚	名称	功能	电压基准
1	INA2	A侧逻辑输入2，INA2转换至OUTB2。	GNDA
2	OUTA1	A侧逻辑输出1，OUTA1为推挽式输出。	GNDA
3	OUTA2	A侧逻辑输出2，OUTA2为推挽式输出。	GNDA
4	I/OA1	A侧双向输入/输出1，I/OA1转换至I/OB1或反方向转换，为开漏输出。	GNDA
5	I/OA2	A侧双向输入/输出2，I/OA2转换至I/OB2或反方向转换，为开漏输出。	GNDA
6	GNDA	A侧接地参考端，V_{GNDA}必须小于或等于V_{GNDB}。	—
7	GNDB	B侧接地参考端，V_{GNDB}必须大于或等于V_{GNDA}。	—
8	I/OB2	B侧双向输入/输出2，I/OB2转换至I/OA2或反方向转换，为开漏输出。	GNDB
9	I/OB1	B侧双向输入/输出1，I/OB1转换至I/OA1或反方向转换，为开漏输出。	GNDB
10	INB2	B侧逻辑输入2，INB2转换至OUTA2。	GNDB
11	INB1	B侧逻辑输入1，INB1转换至OUTA1。	GNDB
12	OUTB2	B侧逻辑输出2，OUTB2为推挽式输出。	GNDB
13	OUTB1	B侧逻辑输出1，OUTB1为推挽式输出。	GNDB
14	V_{DDB}	B侧逻辑供电电压，利用0.1µF陶瓷电容将V_{DDB}旁路至GNDB。	GNDB
15	V_{DDA}	A侧逻辑供电电压，利用0.1µF陶瓷电容将V_{DDA}旁路至GNDA。	GNDA
16	INA1	A侧逻辑输入1，INA1转换至OUTB1。	GNDA
—	EP	裸焊盘，将EP连接至GNDA。	—

功能框图



详细说明

MAX14842能够在地电位相差高达72V的系统之间进行地电平和逻辑电平转换。器件由V_{DDA}和V_{DDB}两个电源供电，分别设置每侧的逻辑电平。V_{DDA}和V_{DDB}分别以GNDA和GNDB为参考。MAX14842的四路单向通道均支持高达30Mbps数据率，两个双向通道可支持2Mbps数据率。

地电位转换/电平转换

为保证正常工作，须确保0V ≤ (V_{GNDB} – V_{GNDA}) ≤ 72V。注意，GNDB必须大于或等于GNDA。

同时确保3.0V ≤ (V_{DDA} – V_{GNDA}) ≤ 5.5V及3.0V ≤ (V_{DDB} – V_{GNDB}) ≤ 5.5V。只要每路电压均在正常工作范围内，(V_{DDA} – V_{GNDA})可大于或小于(V_{DDB} – V_{GNDB})。

单向通道

器件具有四个单向通道，每个通道可独立工作在高达30Mbps的数据率。每个单向通道采用推挽式输出驱动器，无需上拉电阻。驱动器也能够驱动TTL和CMOS逻辑输入。

双向通道

器件具有两路双向转换通道，采用开漏输出，双向通道无需方向控制输入。一侧的逻辑低电平将拉低另一侧的相应引脚，同时避免了器件的数据锁存。为防止双向通道闭锁，I/OA1和I/OA2输入的逻辑低电平门限(V_{IT})比I/OA1和I/OA2输出的逻辑低电平(V_{OL})至少低50mV，这样可以防止A侧的输出逻辑低电平被作为输入低电平而转换到B侧，反之亦然。

I/OA1、I/OA2、I/OB1和I/OB2引脚具有开漏输出，需要上拉电阻拉至对应的电源，以提供逻辑高电平输出。在确保输出低电平的前提下，B侧吸电流可达30mA，A侧吸电流可达10mA (参见*Electrical Characteristics*表)。

器件的双向通道支持I^2C时钟扩展。

独立的地参考端

器件设计用于地电位隔离或地电位偏差较大的系统之间的逻辑信号转换。

启动和欠压锁定

器件内部监测V_{DDA}和V_{DDB}电源的欠压条件。上电、断电或正常工作期间的电源电压跌落都有可能产生欠压事件。当在任一侧电源检测到欠压故障时，无论输入状态如何，均将自动控制两侧的所有输出。双向输出变为高阻态，通过开漏输出的外部上拉电阻拉至高电平。欠压条件下，单向输出由内部拉至V_{DDA}或V_{DDB}电源电压。

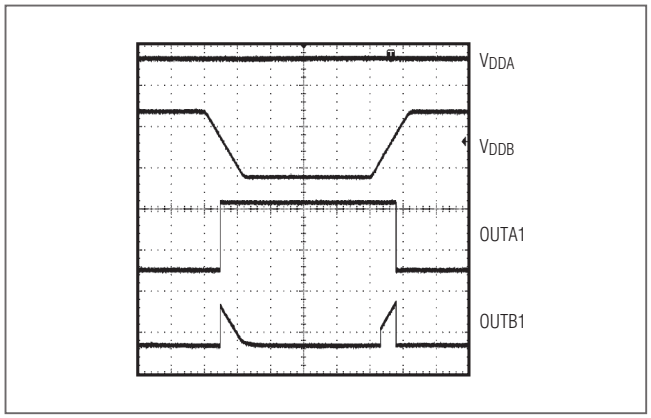


图3. 欠压锁定

图3所示为上电和断电期间的输出。

应用信息

V_{GG}上的交流分量

地电位差V_{GG}具有时变(交流)分量，需要对其幅度加以限制，以确保MAX14842工作在规定条件下。V_{GG}上交流分量的最大允许幅度是频率的函数。

电源排序

MAX14842没有特定的供电顺序要求，每一侧的逻辑电平由V_{DDA}和V_{DDB}分别设置。每路电源都允许保持在正常的供电状态，与另一侧电源是否供电以及供电电压的大小无关。

电源去耦

为降低电源纹波以及引起数据误码的几率，利用0.1µF陶瓷电容分别将V_{DDA}和V_{DDB}旁路至GNDA和GNDB，旁路电容应尽量靠近电源输入引脚安装。

单向和双向电平转换

MAX14842可同时提供单向和双向信号传输，每个单向通道仅可用于*功能框图*所示方向，双向通道的信号传输无需方向控制。

芯片信息

PROCESS: BiCMOS

封装信息

如需最近的封装外形信息和焊盘布局(占位面积)，请查询**china.maxim-ic.com/packages**。请注意，封装编码中的“+”、“#”或“–”仅表示RoHS状态。封装图中可能包含不同的尾缀字符，但封装图只与封装有关，与RoHS状态无关。

封装类型	封装编码	外形编号	焊盘布局编号
16 TQFN-EP	T1644+4	**21-0139**	**90-0070**

修订历史

修订号	修订日期	说明	修改页
0	12/10	最初版本。	—
1	3/11	从*定购信息*中删除MAX14842ETE+，删除*定购信息*中MAX14842ATE+的未来产品状态，在*特性*、*Absolute Maximum Ratings*和*Electrical Characteristics*部分增加了汽车级温度范围。	1–4

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