19-4349; Rev 0; 10/08

MAXIM

16位、单声道音频codec

MAX9860

概述

MAX9860是低功耗、单声道音频codec，可以为无线音频耳机和其它单声道音频设备提供完备的解决方案。MAX9860采用片上桥接负载单声道耳机放大器，在1.8V单电源供电时能够向32Ω听筒输出30mW的功率。器件的超低功耗使其成为电池供电设备的理想选择。

MAX9860灵活的时钟电路采用10MHz至60MHz的公共系统时钟频率，省去了外部PLL和多个晶体振荡器。无论工作在同步或异步方式，ADC和DAC均可支持8kHz至48kHz的采样速率。器件同时还支持主机定时和从机定时模式。

器件具有两路差分麦克风输入、用户可编程的前置放大器以及可编程增益放大器。自动增益控制结合可选的启动/释放时间和信号门限，可实现最大的动态范围。噪声选通结合可选门限，可以在没有连接信号的情况下保证通道安静。DAC和ADC数字滤波器可实现带外信号的全衰减以及5阶GSM兼容的数字高通滤波。数字侧音频混音器可实现麦克风/ADC信号至DAC/耳机输出的环回。

串行DAC和ADC数据通过灵活的数字I^2S兼容接口传输，并且支持TDM模式。模式设定、音量控制以及关断等可通过2线、I^2C兼容接口进行编程设置。

MAX9860工作在-40°C至+85°C扩展级温度范围，采用小尺寸的4mm x 4mm、24引脚薄形QFN封装。

应用

音频耳机

便携式导航设备

移动电话

智能手机

VoIP电话

音频配件

引脚配置和典型工作电路在数据资料的最后给出。

特性

- ♦ 1.8V单电源供电
- ♦ 数字高通椭圆滤波器，带217Hz的陷波(GSM)
- ♦ 单声道30mW BTL耳机放大器
- ♦ 双路低噪声麦克风输入
- ♦ 自动麦克风增益控制和噪声选通
- ♦ 90dB DAC DR (f_S = 48kHz)
- ♦ 81dB ADC DR (f_S = 48kHz)
- ♦ 支持10MHz至60MHz的主时钟频率
- ♦ 支持8kHz至48kHz的采样速率
- ♦ 灵活的数字音频接口
- ♦ 无咔嗒/噼噗声操作
- ♦ 2线、I^2C兼容控制接口
- ♦ 采用24引脚、薄型QFN、4mm x 4mm x 0.8mm封装

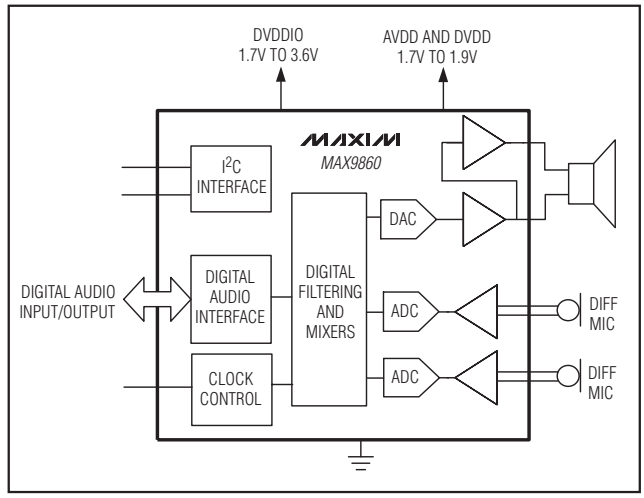
定购信息

PART	TEMP RANGE	PIN-PACKAGE
MAX9860ETG+	-40°C to +85°C	24 TQFN-EP*

+表示无铅/符合RoHS标准的封装。

**EP = 裸焊盘。*

简化框图



ABSOLUTE MAXIMUM RATINGS

(Voltages referenced to AGND.)
DVDDIO, SDA, SCL, $\overline{IRQ}$.....-0.3V to +3.6V
AVDD, DVDD.....-0.3V to +2V
AGND, DGND, MICGND.....-0.3V to +0.3V
OUTP, OUTN, PREG, REF, MICBIAS.....-0.3V to (AVDD + 0.3V)
MICLP, MICLN, MICRP, MICRN, REG ....-0.3V to (PREG + 0.3V)
MCLK, LRCLK, BCLK,
SDOUT, SDIN.....-0.3V to (DVDDIO + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
24-Pin TQFN (derate 27.8mW/°C above +70°C, multilayer board) 2222mW
Junction-to-Ambient Thermal Resistance (θ_{JA}) (Note 1)
24-Pin TQFN (derate 27.8mW/°C above +70°C, multilayer board) .....36°C/W
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com.cn/thermal-tutorial**.

ELECTRICAL CHARACTERISTICS

(V_{AVDD} = V_{DVDD} = V_{DVDDIO} = +1.8V, R_L = ∞, headphone load (R_L) connected between OUTP and OUTN, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, A_{VPRE} = +20dB, $A_{VMICPGA}$ = 0dB, MCLK = 13MHz, LRCLK = 8kHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage Range		AVDD (inferred from HP output PSRR)		1.7	1.8	1.9	V
		DVDD (inferred from codec performance tests)		1.7	1.8	1.9	
		DVDDIO		1.7	1.8	3.6	
Total Supply Current (Note 3)	$I_{AVDD+DVDD}$	DAC playback mode (48kHz)	AVDD		1.46	2.2	mA
			DVDD		1.05	1.6	
		Full operation 8kHz mono ADC + DAC	AVDD		4.08	5.7	
			DVDD		0.78	1.0	
		Full operation 8kHz stereo ADC + DAC	AVDD		6.17	9.0	
			DVDD		0.8	1.2	
		Stereo ADC only (48kHz)	AVDD		5.38	8.0	
			DVDD		1.68	2.2	
Shutdown Supply Current	$I_{\overline{SHDN}}$	T_A = +25°C	AVDD		0.56	5	µA
			DVDD + DVDDIO		1.65	5	
Shutdown to Full Operation					10		ms
DAC (Note 4)							
Gain Error					±1	±5	%
Dynamic Range (Note 5)	DR	+0dB volume setting, f_S = 8kHz, measured at headphone output, T_A = +25°C		84	90		dB
DAC Full-Scale Output					1		V_{RMS}
DAC Path Phase Delay		f = 1kHz, 0dBFS, HP filter disabled, digital input to analog output	f_S = 8kHz		1.2		ms
			f_S = 16kHz		0.59		
Total Harmonic Distortion + Noise	THD+N	f = 1kHz, MCLK = 12.288MHz, LRCLK = 48kHz			-87		dB

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{DVDD} = V_{DVDDIO} = +1.8V, R_L = ∞, headphone load (R_L) connected between OUTP and OUTN, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, A_{VPRE} = +20dB, $A_{VMICPGA}$ = 0dB, MCLK = 13MHz, LRCLK = 8kHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power-Supply Rejection Ratio	PSRR	f = 1kHz, V_{RIPPLE} = 100mV_{P-P}, A_{VPGA} = 0dB		94		dB
		f = 10kHz, V_{RIPPLE} = 100mV_{P-P}, A_{VPGA} = 0dB		71		
DAC LOWPASS DIGITAL FILTER						
Passband Cutoff	f_{PLP}	With respect to f_S within ripple; f_S = 8kHz to 48kHz		0.448 x f_S		Hz
		-3dB cutoff		0.451		f_S
Passband Ripple		$f < f_{PLP}$		±0.1		dB
Stopband Cutoff	f_{SLP}	With respect to f_S; f_S = 8kHz to 48kHz		0.476 x f_S		Hz
Stopband Attenuation		$f > f_{SLP}$, f = 20Hz to 20kHz		75		dB
DAC HIGHPASS DIGITAL FILTER						
5th Order Passband Cutoff (-3dB from Peak, I²C Register Programmable) (Note 6)	f_{DHPPB}	DVFLT = 0x1 (elliptical for 16kHz GSM)		0.0161 x f_S		Hz
		DVFLT = 0x2 (500Hz Butterworth for 16kHz)		0.0312 x f_S		
		DVFLT = 0x3 (elliptical for 8kHz GSM)		0.0321 x f_S		
		DVFLT = 0x4 (500Hz Butterworth for 8kHz)		0.0625 x f_S		
		DVFLT = 0x5 (200Hz Butterworth for 48kHz)		0.0042 x f_S		
5th Order Stopband Cutoff (-30dB from Peak, I²C Register Programmable) (Note 6)	f_{DHPSB}	DVFLT = 0x1 (elliptical for 16kHz GSM)		0.0139 x f_S		Hz
		DVFLT = 0x2 (500Hz Butterworth for 16kHz)		0.0156 x f_S		
		DVFLT = 0x3 (elliptical for 8kHz GSM)		0.0279 x f_S		
		DVFLT = 0x4 (500Hz Butterworth for 8kHz)		0.0312 x f_S		
		DVFLT = 0x5 (200Hz Butterworth for 48kHz)		0.0021 x f_S		
DC Blocking	DC_{Atten}	DVFLT ≠ 0x0		90		dB
ADC						
Full-Scale Input Voltage	0dBFS	Differential MIC Input, A_{VPRE} = 0dB, A_{VPGA} = 0dB		1		V_{P-P}
Channel Gain Mismatch				±0.3		%

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{DVDD} = V_{DVDDIO} = +1.8V, R_L = ∞, headphone load (R_L) connected between OUTP and OUTN, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, A_{VPRE} = +20dB, $A_{VMICPGA}$ = 0dB, MCLK = 13MHz, LRCLK = 8kHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Dynamic Range (Note 5)	DR	f_S = 8kHz, A_{VPRE} = 0dB, A-weighted from 20Hz to f_S/2			81		dB
		f_S = 48kHz, A_{VPRE} = 0dB, T_A = +25°C		75	83		
ADC Phase Delay		f = 1kHz, 0dBFS, HP filter disabled, analog input to digital output	f_S = 8kHz		1.2		ms
			f_S = 16kHz		0.61		
Total Harmonic Distortion	THD	f = 1kHz, f_S = 48kHz, T_A = +25°C		-70	-75		dB
Power-Supply Rejection Ratio	PSRR	f = 1kHz, V_{RIPPLE} = 100mV_{P-P}, A_{VPGA} = 0dB			82		dB
		f = 10kHz, V_{RIPPLE} = 100mV_{P-P}, A_{VPGA} = 0dB			76		
Channel Crosstalk		Driven channel at -1dBFS, f = 1kHz			-92		dB
ADC LOWPASS DIGITAL FILTER							
Passband Cutoff	f_{PLP}	With respect to f_S within ripple; f_S = 8kHz to 48kHz			0.445 x f_S		Hz
		-3dB cutoff			0.449		f_S
Passband Ripple		f < f_{PLP}			±0.1		dB
Stopband Cutoff	f_{SLP}	With respect to f_S; f_S = 8kHz to 48kHz			0.469 x f_S		Hz
Stopband Attenuation		f > f_{SLP}			74		dB
ADC HIGHPASS DIGITAL FILTER							
5th Order Passband Cutoff (-3dB from Peak, I²C Register Programmable) (Note 6)	f_{AHPPB}	AVFLT = 0x1 (elliptical for 16kHz GSM)			0.0161 x f_S		Hz
		AVFLT = 0x2 (500Hz Butterworth for 16kHz)			0.0312 x f_S		
		AVFLT = 0x3 (elliptical for 8kHz GSM)			0.0321 x f_S		
		AVFLT = 0x4 (500Hz Butterworth for 8kHz)			0.0625 x f_S		
		AVFLT = 0x5 (200Hz Butterworth for 48kHz)			0.0042 x f_S		

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{DVDD} = V_{DVDDIO} = +1.8V, R_L = ∞, headphone load (R_L) connected between OUTP and OUTN, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, A_{VPRE} = +20dB, $A_{VMICPGA}$ = 0dB, MCLK = 13MHz, LRCLK = 8kHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
5th Order Stopband Cutoff (-30dB from peak, I²C Register Programmable) (Note 6)	f_{AHPSB}	AVFLT = 0x1 (elliptical for 16kHz GSM)			0.0139 x f_S		Hz
		AVFLT = 0x2 (500Hz Butterworth for 16kHz)			0.0156 x f_S		
		AVFLT = 0x3 (elliptical for 8kHz GSM)			0.0279 x f_S		
		AVFLT = 0x4 (500Hz Butterworth for 8kHz)			0.0312 x f_S		
		AVFLT = 0x5 (200Hz Butterworth for 48kHz)			0.0021 x f_S		
DC Blocking	DC_{ATTEN}	AVFLT ≠ 0x0			90		dB
CLOCKING							
MCLK Input Frequency		MCLK is not required to be synchronous or related to the desired LRCLK data rate		10		60	MHz
MCLK Duty Cycle				40	50	60	%
Maximum MCLK Input Jitter		For guaranteed performance limits			100		ps_{RMS}
LRCLK Data Rate Frequency				8		48	kHz
LRCLK PLL Lock Time					12	25	ms
LRCLK Acceptable Jitter for Maintaining PLL Lock					±20		ns
MONO HEADPHONE AMPLIFIER							
Output Power	P_{OUT}	f = 1kHz, THD+N ≤ 1%, T_A = +25°C	R_L = 16Ω	30	50		mW
			R_L = 32Ω		33		
Total Harmonic Distortion + Noise	THD+N	R_L = 32Ω, P_{OUT} = 25mW, f = 1kHz			0.05		%
		R_L = 16Ω, P_{OUT} = 25mW, f = 1kHz			0.08		
Dynamic Range (Note 5)	DR	+0dB volume setting, DAC input at f_S = 8kHz to 48kHz			90		dB
Power-Supply Rejection Ratio	PSRR	AVDD = 1.7V to 1.9V		60	84		dB
		V_{RIPPLE} = 100mV_{P-P}, f = 217Hz			86		
		V_{RIPPLE} = 100mV_{P-P}, f = 20kHz			71		
Output Offset Voltage	V_{OS}	V_{OUTP} - V_{OUTN}, T_A =+25°C			± 0.25	± 1	mV
Capacitive Drive Capability		No sustained oscillations	R_L = 32Ω		500		pF
			R_L = ∞		100		
Click-and-Pop Level		Peak voltage into/out of shutdown, 32sps, A-weighted			-70		dBV

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{DVDD} = V_{DVDDIO} = +1.8V, R_L = ∞, headphone load (R_L) connected between OUTP and OUTN, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, A_{VPRE} = +20dB, $A_{VMICPGA}$ = 0dB, MCLK = 13MHz, LRCLK = 8kHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
MICROPHONE AMPLIFIER							
Preamplifier Gain	A_{VPRE}	T_A = +25°C	PAM = 00		Off		dB
			PAM = 01	-0.5	0	+0.5	
			PAM = 10	19	20	21	
			PAM = 11	29	30	31	
MIC PGA Gain	$A_{VMICPGA}$	PGAM = 0x14–0x1F			0		dB
		PGAM = 0x00			+20		
MIC PGA Gain Step Size					1		dB
Common-Mode Rejection Ratio	CMRR	V_{IN} = 100mV_{P-P} at 217Hz			50		dB
MIC Input Resistance	R_{IN_MIC}	All gain settings, measured at MICLN/MICRN		30	50		kΩ
MIC Input Bias Voltage				0.7	0.8	0.9	V
Total Harmonic Distortion + Noise	THD+N	A_{VPRE} = 0dB, $A_{VMICPGA}$ = 0dB, V_{IN} = 1V_{P-P}, f = 1kHz			-75		dB
		A_{VPRE} = +30dB, $A_{VMICPGA}$ = 0dB, V_{IN} = 31mV_{P-P}, f = 1kHz			-66		dB
MIC Power-Supply Rejection Ratio	PSRR	AVDD = 1.7V to 1.9V		60	95		dB
		V_{RIPPLE} = 100mV at 1kHz, input referred			82		dB
		V_{RIPPLE} = 100mV at 10kHz, input referred			76		dB
MICROPHONE BIAS							
MICBIAS Output Voltage	$V_{MICBIAS}$	I_{LOAD} = 1mA, T_A = +25°C		1.5	1.55	1.6	V
Load Regulation		I_{LOAD} = 1mA to 2mA			0.2	10	mV
MICBIAS Line Ripple Rejection	LRR	V_{RIPPLE} = 100mV_{P-P} at 217Hz			82		dB
		V_{RIPPLE} = 100mV_{P-P} at 10kHz			81		dB
MICBIAS Noise Voltage		A-weighted			9.5		$µV_{RMS}$
AUTOMATIC GAIN CONTROL							
AGC Hold Duration		AGCHLD[1:0] setting range, FREQ ≠ 0		50		400	ms
AGC Attack Time		AGCATK[1:0] setting range, FREQ ≠ 0		3		200	ms
AGC Release Time		AGCRLS[2:0] setting range, FREQ ≠ 0		0.078		10	s
AGC Threshold Level		AGCSTH[3:0] setting range, FREQ ≠ 0		-3		-18	dB
NOISE GATE							
NG Attack and Release Time					0.5		s
NG Threshold Level				-72		-16	dB
Noise Gate Threshold Step Size					4		dB
NG Attenuation				0		12	dB
DIGITAL SIDETONE							
Sidetone Gain Adjust	DVST	2dB steps		-60		0	dB
Sidetone Phase Delay	PDLY	MIC input to headphone output, f = 1kHz, HP filter disabled	8kHz		2.2		ms
			16kHz		1.1		

DIGITAL AUDIO INTERFACE ELECTRICAL CHARACTERISTICS

(V_{DVDD} = V_{DVDDIO} = 1.8V, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
BCLK Cycle Time	t_{BCLKS}	Slave operation	75			ns
BCLK High Time	t_{BCLKH}	Slave operation	30			ns
BCLK Low Time	t_{BCLKL}	Slave operation	30			ns
BCLK or LRCLK Rise and Fall Time	t_R, t_F	Master operation		7		ns
SDIN or LRCLK to BCLK Rising Setup Time	t_{SU}	ABCI = DBCI = 0	25			ns
SDIN or LRCLK to BCLK Falling Setup Time	t_{SU}	ABCI = DBCI = 1	25			ns
SDIN or LRCLK to BCLK Rising Hold Time	t_{HD}	ABCI = DBCI = 0	0			ns
SDIN or LRCLK to BCLK Falling Hold Time	t_{HD}	ABCI = DBCI = 1	0			ns
SDOUT Delay Time from BCLK Rising Edge	t_{DLY}	ABCI = DBCI = 0, C_L = 30pF	0		40	ns

I²C INTERFACE ELECTRICAL CHARACTERISTICS

(V_{DVDD} = V_{DVDDIO} = 1.8V, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Serial-Clock Frequency	f_{SCL}		0		400	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		1.3			µs
Hold Time (Repeated) START Condition	$t_{HD,STA}$		0.6			µs
SCL Pulse Width Low	t_{LOW}		1.3			µs
SCL Pulse Width High	t_{HIGH}		0.6			µs
Setup Time for a Repeated START Condition	$t_{SU,STA}$		0.6			µs
Data Hold Time	$t_{HD,DAT}$		0		900	ns
Data Setup Time	$t_{SU,DAT}$		100			ns
SDA and SCL Receiving Rise Time	t_R	C_B is in pF	$20 + 0.1C_B$		300	ns
SDA and SCL Receiving Fall Time	t_F	C_B is in pF	$20 + 0.1C_B$		300	ns

I²C INTERFACE ELECTRICAL CHARACTERISTICS (continued)

(V_{DVDD} = V_{DVDDIO} = 1.8V, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SDA Transmitting Fall Time	t_F	C_B is in pF	20 + 0.1C_B		250	ns
Setup Time for STOP Condition	$t_{SU,STO}$		0.6			µs
Bus Capacitance	C_B				400	pF
Pulse Width of Suppressed Spike	t_{SP}		0		50	ns
DIGITAL INPUTS (LRCLK, BCLK, SDIN, MCLK)						
Input Voltage High	V_{IH}		0.7 x DVDDIO			V
Input Voltage Low	V_{IL}				0.3 x DVDDIO	V
MCLK Input Voltage High			1.4			V
MCLK Input Voltage Low					0.4	V
Input Leakage Current	I_{IH}, I_{IL}	T_A = +25°C	-1		+1	µA
Input Capacitance				3		pF
DIGITAL INPUTS (SCL, SDA)						
Input Voltage High	V_{IH}		0.7 x DVDD			V
Input Voltage Low	V_{IL}				0.3 x DVDD	V
Input Hysteresis				200		mV
Input Leakage Current	I_{IH}, I_{IL}	T_A = +25°C	-1		+1	µA
Input Capacitance				3		pF
CMOS DIGITAL OUTPUTS (BCLK, LRCLK, SDOUT)						
Output Low Voltage	V_{OL}	I_{OL} = 3mA			0.4	V
Output High Voltage	V_{OH}	I_{OL} = 3mA	DVDDIO - 0.4			V
OPEN-DRAIN DIGITAL OUTPUTS (SDA, $\overline{IRQ}$)						
Output High Leakage Current	I_{OH}	V_{OUT} = DVDDIO, T_A = +25°C	-1		+1	µA
Output Low Voltage	V_{OL}	I_{OL} = 3mA			0.4	V

Note 2: All devices are 100% production tested at room temperature. All temperature limits are guaranteed by design.

Note 3: Supply current measurements taken with no applied signal at microphone inputs. A digital zero audio signal used for all digital serial audio inputs. Headphone outputs are loaded as stated in the global conditions.

Note 4: DAC performance is measured at headphone outputs.

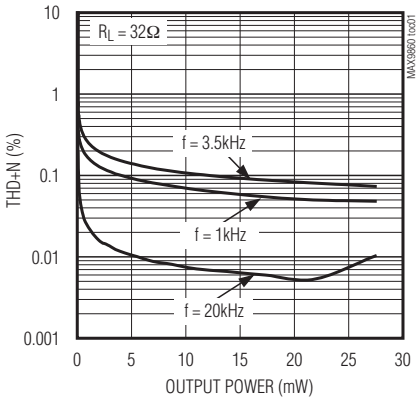
Note 5: ADC, DAC, and headphone amplifier dynamic ranges are measured using the EIAJ method. -60dBV 1kHz input signal, A-weighted and normalized to 0dBFS.

Note 6: Notch for GSM filters occurs at 217Hz.

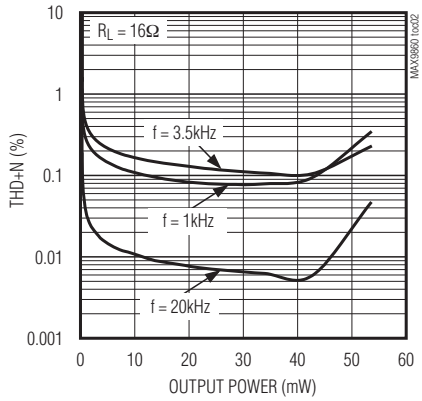
典型工作特性

(V_{AVDD} = +1.8V, V_{DVDD} = V_{DVDDIO} = +1.8V, R_L = ∞, headphone load (R_L) connected between OUTP and OUTN, C_{REF} = 2.2µF, C_{PREG} = C_{REG} = 1µF, $C_{MICBIAS}$ = 1µF $A_{VMICPGA}$ = 0dB, A_{VPRE} = +20dB, MCLK = 13MHz, T_A = +25°C, unless otherwise noted.)

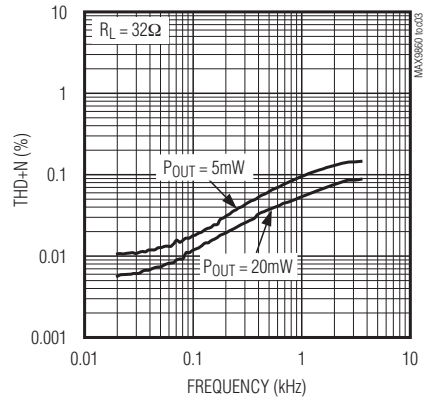
TOTAL HARMONIC DISTORTION + NOISE vs. OUTPUT POWER (DAC TO HP)



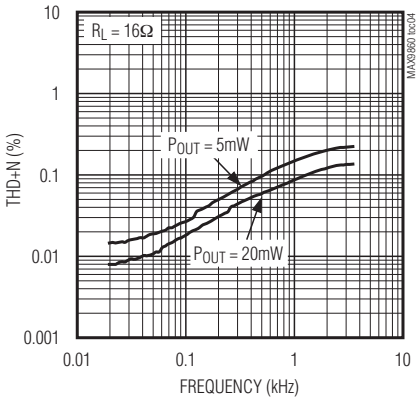
TOTAL HARMONIC DISTORTION + NOISE vs. OUTPUT POWER (DAC TO HP)



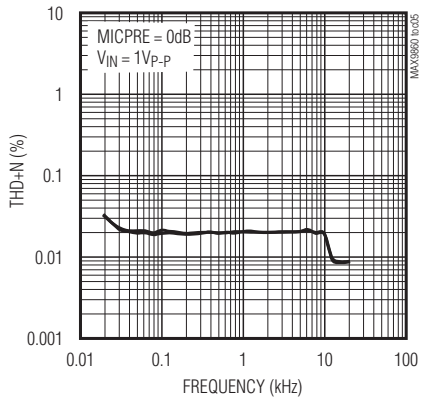
TOTAL HARMONIC DISTORTION + NOISE vs. FREQUENCY (DAC TO HP)



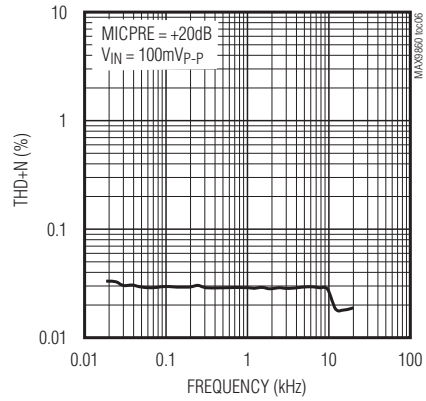
TOTAL HARMONIC DISTORTION + NOISE vs. FREQUENCY (DAC TO HP)



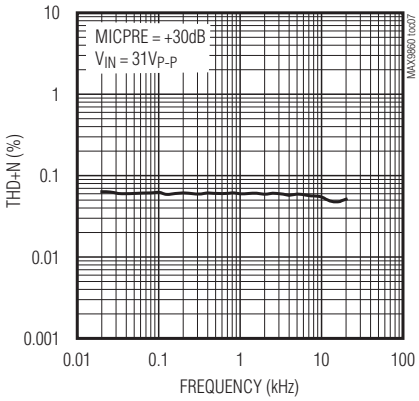
TOTAL HARMONIC DISTORTION + NOISE vs. FREQUENCY (MICL TO ADC)



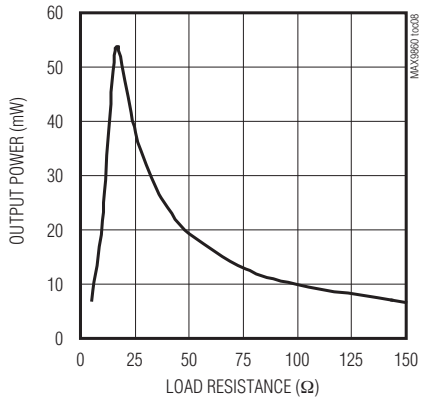
TOTAL HARMONIC DISTORTION + NOISE vs. FREQUENCY (MICL TO ADC)



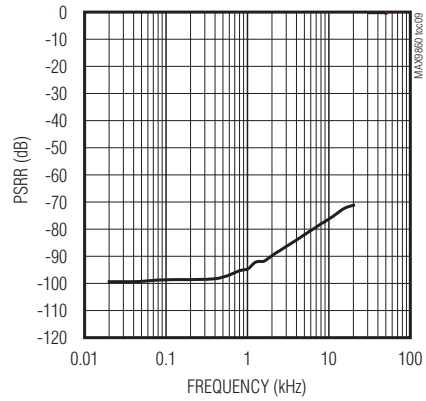
TOTAL HARMONIC DISTORTION + NOISE vs. FREQUENCY (MICL TO ADC)



HEADPHONE OUTPUT POWER vs. LOAD RESISTANCE



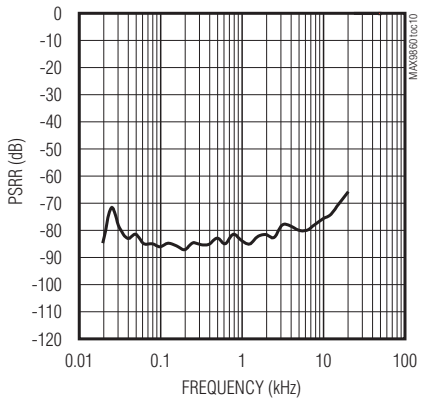
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY (DAC TO HP)



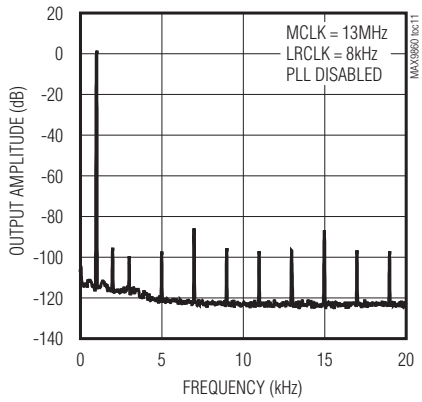
典型工作特性(续)

(V_{AVDD} = +1.8V, V_{DVDD} = V_{DVDDIO} = +1.8V, R_L = ∞, headphone load (R_L) connected between OUTP and OUTN, C_{REF} = 2.2µF, C_{PREG} = C_{REG} = 1µF $C_{MICBIAS}$ = 1µF $A_{VMICPGA}$ = 0dB, A_{VPRE} = +20dB, MCLK = 13MHz, T_A = +25°C, unless otherwise noted.)

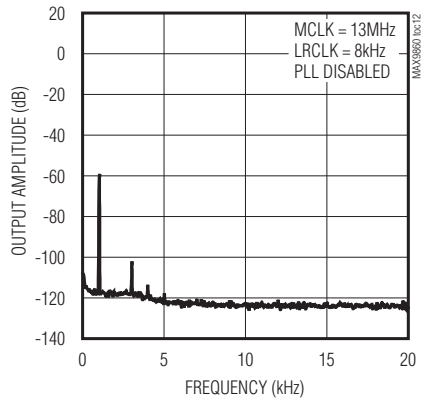
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY (MIC TO ADC)



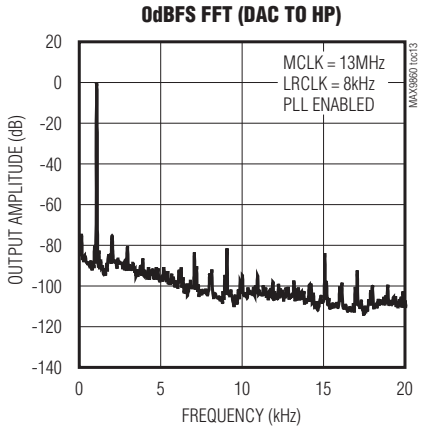
0dBFS FFT (DAC TO HP)



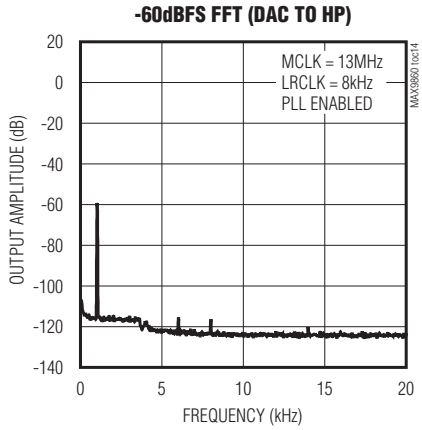
-60dBFS FFT (DAC TO HP)



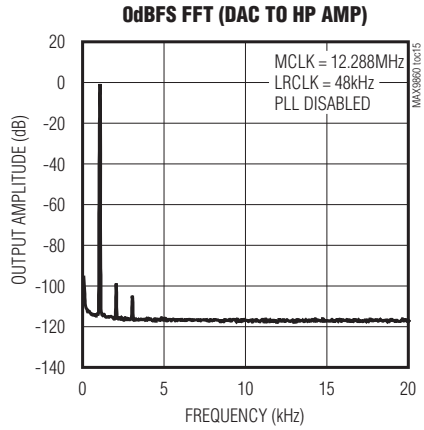
0dBFS FFT (DAC TO HP)



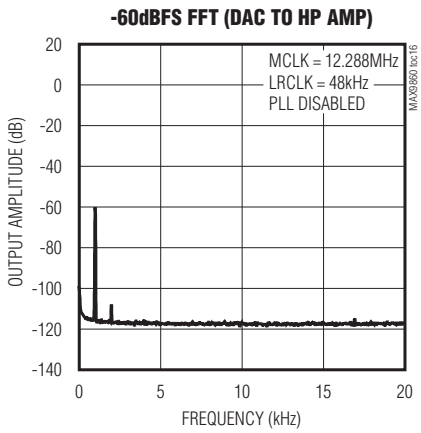
-60dBFS FFT (DAC TO HP)



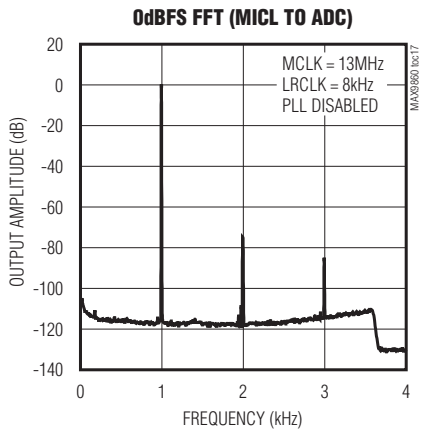
0dBFS FFT (DAC TO HP AMP)



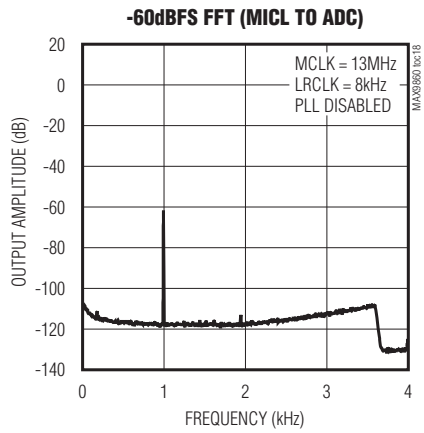
-60dBFS FFT (DAC TO HP AMP)



0dBFS FFT (MICL TO ADC)



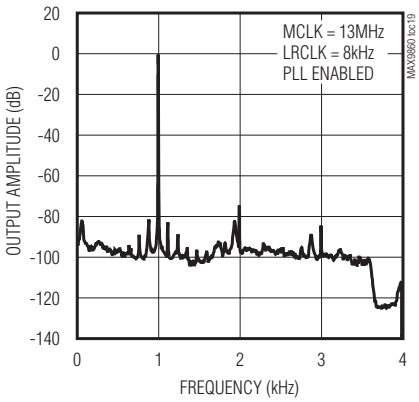
-60dBFS FFT (MICL TO ADC)



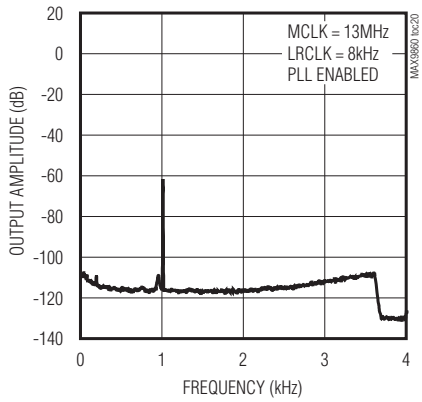
典型工作特性(续)

(V_{AVDD} = +1.8V, V_{DVDD} = V_{DVDDIO} = +1.8V, R_L = ∞, headphone load (R_L) connected between OUTP and OUTN, C_{REF} = 2.2µF, C_{PREG} = C_{REG} = 1µF, $C_{MICBIAS}$ = 1µF $A_{VMICPGA}$ = 0dB, A_{VPRE} = +20dB, MCLK = 13MHz, T_A = +25°C, unless otherwise noted.)

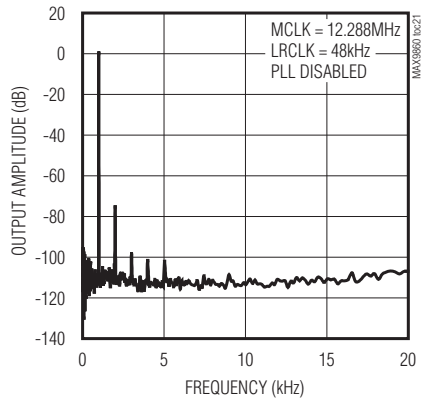
0dBFS FFT (MICL TO ADC)



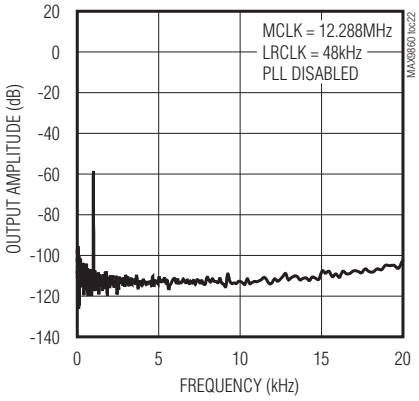
-60dBFS FFT (MICL TO ADC)



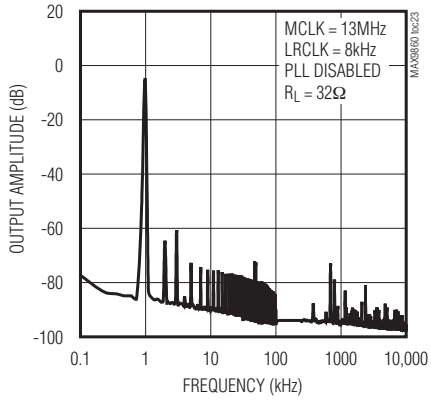
0dBFS FFT (MICL TO ADC)



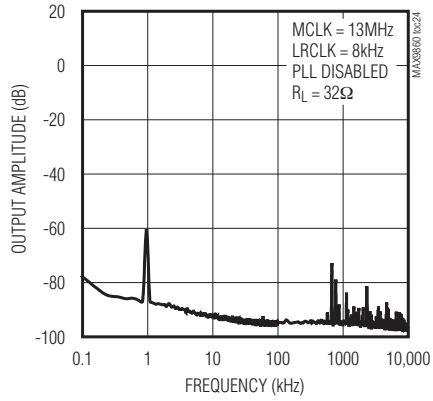
-60dBFS FFT (MICL TO ADC)



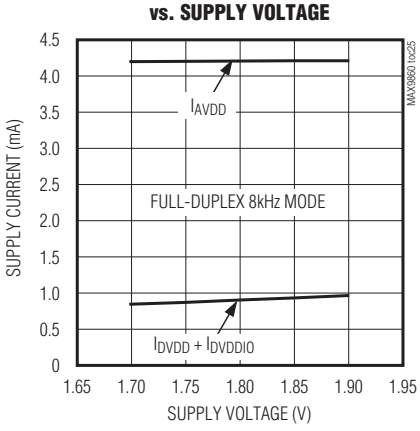
-5dBFS WIDEBAND FFT (DAC TO HP)



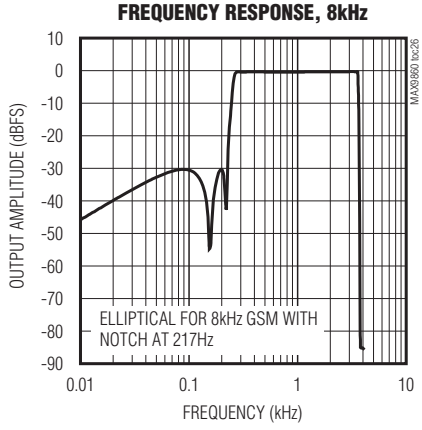
-60dBFS WIDEBAND FFT (DAC TO HP)



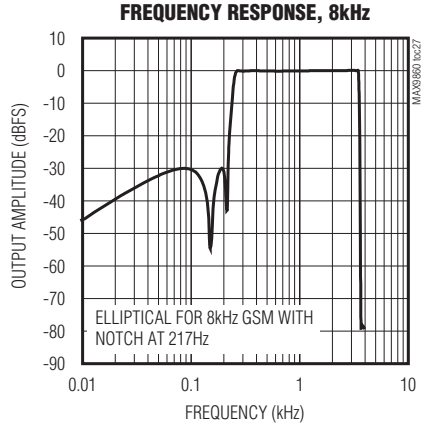
SUPPLY CURRENT vs. SUPPLY VOLTAGE



DAC DIGITAL FILTER FREQUENCY RESPONSE, 8kHz



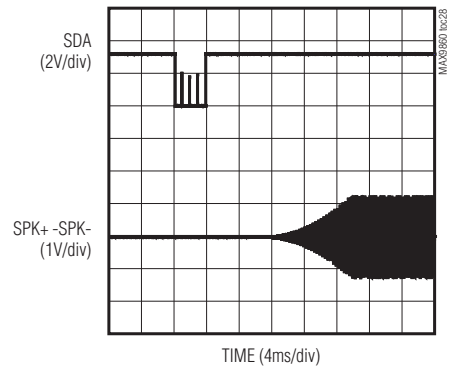
ADC DIGITAL FILTER FREQUENCY RESPONSE, 8kHz



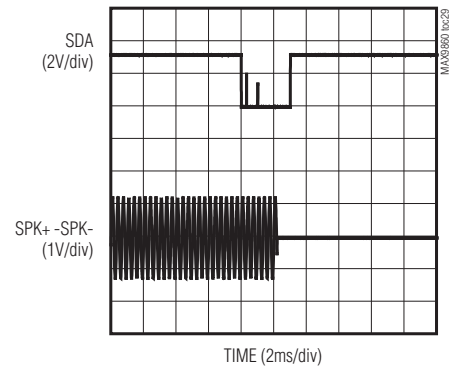
典型工作特性(续)

(V_{AVDD} = +1.8V, V_{DVDD} = V_{DVDDIO} = +1.8V, R_L = ∞, headphone load (R_L) connected between OUTP and OUTN, C_{REF} = 2.2µF, C_{PREG} = C_{REG} = 1µF, $C_{MICBIAS}$ = 1µF $A_{VMICPGA}$ = 0dB, A_{VPRE} = +20dB, MCLK = 13MHz, T_A = +25°C, unless otherwise noted.)

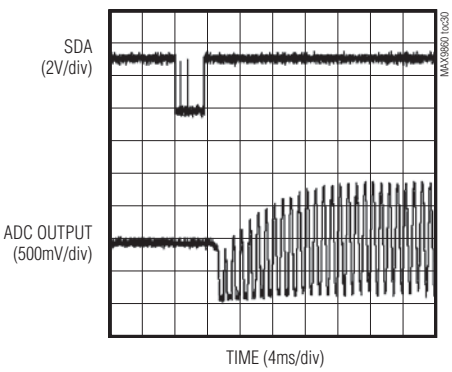
HEADPHONE STARTUP WAVEFORM



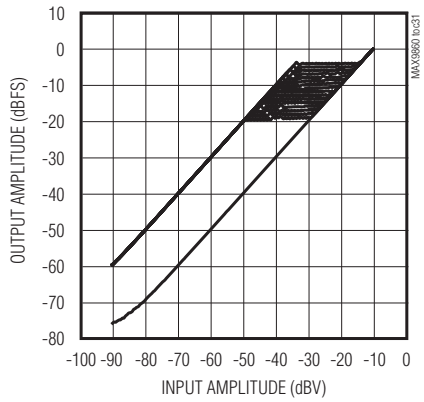
HEADPHONE SHUTDOWN WAVEFORM



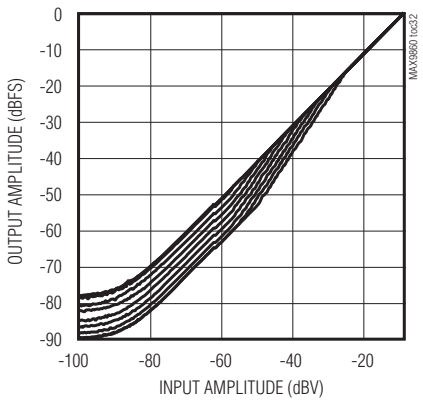
SOFT-START ADC



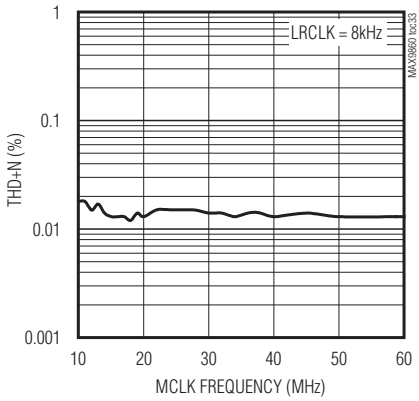
AUTOMATIC GAIN CONTROL THRESHOLDS



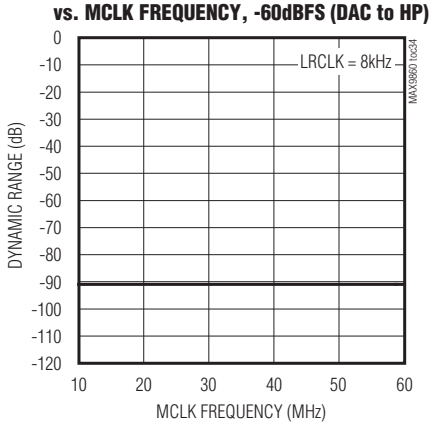
NOISE GATE THRESHOLDS



TOTAL HARMONIC DISTORTION + NOISE vs. MCLK FREQUENCY, 0dBFS (DAC to HP)



DYNAMIC RANGE vs. MCLK FREQUENCY, -60dBFS (DAC to HP)



引脚说明

引脚	名称	功能
1	MICBIAS	麦克风偏置。+1.55V内部和/或外部麦克风偏置。应采用2.2kΩ至470Ω的外部电阻设置麦克风电流。利用一个1µF的电容旁路至MICGND。
2	REG	内部偏置。PREG/2电压基准。采用一个1µF的电容旁路至AGND (+0.8V)。
3	PREG	正内部稳压源。用一个1µF的电容旁路至AGND (+1.6V)。
4	REF	转换器基准(1.23V)。用一个2.2µF的电容旁路至AGND。
5	AGND	模拟地。
6	AVDD	模拟电源。用10µF和0.1µF的电容旁路至AGND。
7	OUTP	耳机输出正端。
8	OUTN	耳机输出负端。
9	SDA	I^2C串行数据输入/输出。
10	SCL	I^2C串行数据时钟。
11	DVDDIO	数字接口电源。数字音频接口电源。用一个1µF的电容旁路至DGND。
12	DGND	数字地。
13	DVDD	数字核电源。用一个1µF电容旁路至DGND。
14	MCLK	主时钟输入。
15	SDOUT	串行音频接口ADC数据输出。
16	SDIN	串行音频接口DAC数据输入。
17	LRCLK	串行音频接口左/右声道时钟。
18	BCLK	串行音频接口位时钟。
19	$\overline{IRQ}$	中断请求。$\overline{IRQ}$为低有效漏极开路输出。用一个10kΩ的电阻上拉至DVDDIO。
20	MICRN	右声道麦克风负输入端。交流耦合至麦克风的低边或者连接至负信号。单端工作时交流耦合至地。
21	MICRP	右声道麦克风正输入端。交流耦合至麦克风的高边或者连接至正信号。单端工作时交流耦合至信号。
22	MICLN	左声道麦克风负输入端。交流耦合至麦克风的低边或者连接至负信号。单端工作时交流耦合至地。
23	MICLP	左声道麦克风正输入端。交流耦合至麦克风的高边或者连接至正信号。单端工作时交流耦合至信号。
24	MICGND	MICBIAS地。连接至AGND。
—	EP	裸焊盘。连接至AGND。

详细说明

MAX9860是一款低功耗、音频带宽、单声道音频codec，可为无线音频耳机和其它单声道音频装置提供完整的音频解决方案。

单声道播放通路通过一个灵活的、兼容I²S、TDM以及左对齐音频信号的数字音频接口接受数字音频。过采样Σ-Δ DAC将输入的数字数据流转换为模拟音频，并通过单声道桥接负载耳机放大器输出。

立体声录音通路带有两路麦克风输入，具有可选增益。麦克风由集成麦克风偏置供电。过采样Σ-Δ ADC转换麦克风信号，并且通过数字音频接口输出数字比特流。

录音通路包括可优化信号电平的自动增益控制(AGC)和可降低空闲噪声的噪声选通功能。自动增益控制监测ADC的输出，不断调整输入增益，从而将输入麦克风信号的动态范围减小20dB。噪声选通通过降低无音频信号时的增益，修正通常AGC所引入的噪声。集成数字滤波为播放和录音通路提供一系列的陷波和高通滤波器，从而限制不希望的低频信号和GSM传输噪声。数字滤波提供的带外能量衰减高达76dB，消除了音频混叠。数字侧音功能将来自于录音通路的音频信号在数字滤波后叠加到播放通路。

MAX9860灵活的时钟电路采用可编程时钟分频器结合数字PLL，使DAC和ADC能够在任何的主时钟(MCLK)和采样率(LRCLK)组合方式下实现最大的工作动态范围。在8kHz至48kHz之间的采样率下，主时钟支持10MHz至60MHz之间的任意频率。器件支持主和从模式，可实现最大灵活性。

I²C寄存器

MAX9860音频codec是完全由软件通过I²C接口进行控制的。上电默认设置为软件关断，需要通过编程内部寄存器来激活器件。器件的完整寄存器映射请参阅表1。

I²C从地址

MAX9860响应从地址0x20的所有写命令和从地址0x21的所有读操作。

表1. I²C寄存器映射

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	REGISTER ADDRESS	POR	R/W
STATUS/INTERRUPT											
Interrupt Status	CLD	SLD	ULK	0	0	0	0	0	0x00	—	R
Microphone NG/AGC Readback	NG			AGC					0x01	—	R
Interrupt Enable	ICLD	ISLD	IULK	0	0	0	0	0	0x02	0x00	R/W
CLOCK CONTROL											
System Clock	0	0	PSCLK		0	FREQ		16KHZ	0x03	0x00	R/W
Stereo Audio Clock Control High	PLL	NHI							0x04	0x00	R/W
Stereo Audio Clock Control Low	NLO								0x05	0x00	R/W
DIGITAL AUDIO INTERFACE											
Interface	MAS	WCI	DBCI	DDLY	HIZ	TDM	0	0	0x06	0x00	R/W
Interface	0	0	ABCI	ADLY	ST	BSEL			0x07	0x00	R/W
DIGITAL FILTERING											
Voice Filter	AVFLT				DVFLT				0x08	0x00	R/W
DIGITAL LEVEL CONTROL											
DAC Attenuation	DVA								0x09	0x00	R/W
ADC Output Levels	ADCRL				ADCLL				0x0A	0x00	R/W
DAC Gain and Sidetone	0	DVG		DVST					0x0B	0x00	R/W
MICROPHONE LEVEL CONTROL											
Microphone Gain	0	PAM		PGAM					0x0C	0x00	R/W
RESERVED											
Reserved	0	0	0	0	0	0	0	0	0x0D	0x00	
MICROPHONE AUTOMATIC GAIN CONTROL											
Microphone AGC	AGCSRC	AGCRLS			AGCATK			AGCHLD	0x0E	0x00	R/W
Noise Gate, Microphone AGC	ANTH				AGCTH				0x0F	0x00	R/W
POWER MANAGEMENT											
System Shutdown	$\overline{\text{SHDN}}$	0	0	0	DACEN	0	ADCLEN	ADCREN	0x10	0x00	R/W

状态/中断

状态寄存器0x00和0x01为只读寄存器，用于报告各种不同设备功能的状态。当对状态寄存器进行读操作时，状态寄存器位被清除，并且在下一次事件发生时被置位。寄存器0x02决定了寄存器0x00的状态标识是否同时将$\overline{IRQ}$置为逻辑高。

表2. 状态/中断寄存器

REGISTER ADDRESS	B7	B6	B5	B4	B3	B2	B1	B0
0x00	CLD	SLD	ULK	0	0	0	0	0
0x01	NG			AGC				
0x02	ICLD	ISLD	IULK	0	0	0	0	0

BITS	FUNCTION	
CLD	Clip Detect Flag. Indicates that a signal has become clipped in the ADC or DAC digital signal paths. CLD also indicates that the AGC function, when enabled, has set the microphone PGA to 0dB and no further gain reduction is possible.	
SLD	Slew Level Detect Flag. When volume or gain changes are made, the slewing circuitry smoothly steps through all intermediate settings. When SLD is set high, all slewing has completed and the volume or gain is at its final value.	
ULK	Digital PLL Unlock Flag. Indicates that the digital audio PLL for the ADC or DAC has become unlocked and digital signal data is not reliable. When beginning operation in master mode, this flag goes high and can be cleared by reading the status register.	
NG	Noise Gate Attenuation. When the noise gate is enabled these bits indicate the current noise gate attenuation.	
	Code	Attenuation
	000	0dB
	001	1dB
	010	2dB
	011	3dB
	100	6dB
	101	8dB
	110	10dB
	111	12dB
AGC	AGC Gain. When the AGC is enabled these bits indicate the AGC controlled level to the MIC preamp. The levels indicated by these bits correspond to the levels defined for the PGAM bits described in register 0x0C.	

时钟控制

MAX9860采用介于10MHz至60MHz的系统时钟作为主时钟(MCLK)。在内部，MAX9860需要10MHz至20MHz的时钟，因而将主时钟1、2或4预分频以产生内部时钟(PCLK)。PCLK用于为MAX9860的所有部分提供时钟。

MAX9860支持从8kHz至48kHz的任何采样率，包括了全部的常见采样率(8kHz、16kHz、24kHz、32kHz、44.1kHz和48kHz)。为了适应各种各样的系统架构，MAX9860支持三种主要时钟模式：

常规模式：该模式用一个15位的时钟分频系数设置相对于预分频MCLK输入(PCLK)的采样率。这样就使MCLK和LRCLK频率具有高度灵活性，并且可用于主模式和从模式。

整数模式：在整数模式下，当采样率为8kHz和16kHz时，可编程工作在常见的MCLK频率(12MHz、13MHz和19.2MHz)。在这些模式下，MCLK和LRCLK速率可通过FREQ和16KHZ位选择，而无需使用NHI、NLO和PLL控制位。

PLL模式：在从模式下工作时，使能PLL，将其锁相至与PCLK异步的外部LRCLK信号。

表3. 时钟控制寄存器

REGISTER ADDRESS	B7	B6	B5	B4	B3	B2	B1	B0
0x03	0	0	PSCLK		0	FREQ		16KHZ
0x04	PLL	NHI						
0x05	NLO							

BITS	FUNCTION
PSCLK[1:0]	**MCLK Prescaler** Divides MCLK down to generate a PCLK between 10MHz and 20MHz. 00 = Disable clock for low-power shutdown. 01 = Select if MCLK is between 10MHz and 20MHz. 10 = Select if MCLK is between 20MHz and 40MHz. 11 = Select if MCLK is greater than 40MHz.
FREQ[1:0]	**Integer Clock Mode** Enables exact integer mode for three predefined PCLK frequencies. Exact integer mode is normally intended for master mode, but can be enabled in slave mode if the externally supplied LRCLK exactly matches the frequency specified in each mode. 00 = Normal operation (configure clocking with the PLL, NHI, and NLO bits). 01 = Select when PCLK is 12MHz (LRCLK = PCLK/1500 or PCLK/750). 10 = Select when PCLK is 13MHz (LRCLK = PCLK/1625 or PCLK/812.5). 11 = Select when PCLK is 19.2MHz (LRCLK = PCLK/2400 or PCLK/1200). When FREQ ≠ 00, the PLL, NHI, and NLO bits are unused.
16KHZ	**16kHz Mode** When FREQ ≠ 00: 0 = LRCLK is exactly 8kHz. 1 = LRCLK is exactly 16kHz. When FREQ = 00, 16KHZ is used to set the AGC clock rate: 0 = Use when LRCLK ≤ 24kHz. 1 = Use when LRCLK > 24kHz.

表3. 时钟控制寄存器(续)

BITS	FUNCTION
PLL	**PLL Enable** 0 = (Valid for slave and master mode)—The frequency of LRCLK is set by the NHI and NLO divider bits. Set PLL = 0 in slave mode only if the externally generated LRCLK can be exactly selected using the LRCLK divider. 1 = (Valid for slave mode only)—Used when the audio master generates an LRCLK not selectable using the LRCLK divider. A digital PLL locks on to the externally supplied LRCLK signal regardless of the MCLK frequency. **Rapid Lock Mode** To enable rapid lock mode set NHI and NLO to the nearest desired ratio and set NLO[0] = 1 (Register 0x05, bit 0) before setting the PLL mode bit.
NHI and NLO	**LRCLK Divider** NHI and NLO control a 15-bit clock divider (N). When the PLL = 0 and FREQ = 00, the frequency of LRCLK is determined by the clock divider. See Table 4 for common N values. $N = (65{,}536 \times 96 \times f_{LRCLK})/f_{PCLK}$ f_{LRCLK} = LRCLK frequency f_{PCLK} = prescaled MCLK internal clock frequency (PCLK)

表4. 常见N值

MCLK (MHz)	LRCLK (kHz)					
	PSCLK	**8**	**16**	**32**	**44.1**	**48**
11.2896	01	116A	22D4	45A9	***6000***	687D
12	01	1062	20C5	4189	5A51	624E
12.288	***01***	***1000***	***2000***	***4000***	5833	***6000***
13	01	F20	1E3F	3C7F	535F	5ABE
19.2	01	A3D	147B	28F6	3873	3D71
24	10	1062	20C5	4189	5A51	624E
26	10	F20	1E3F	3C7F	535F	5ABE
27	10	E90	1D21	3A41	5048	5762

注：用粗斜体表示的整数值可提供最大满度性能。

数字音频接口

MAX9860的数字音频接口支持各种工作模式，可实现最大兼容性。请参阅图1至4的时序图。在主模式下，MAX9860输出LRCLK和BCLK，而从模式下，它们则为输入。在主模式下工作时，能以各种方式配置BCLK，以确保与其它音频装置相兼容。

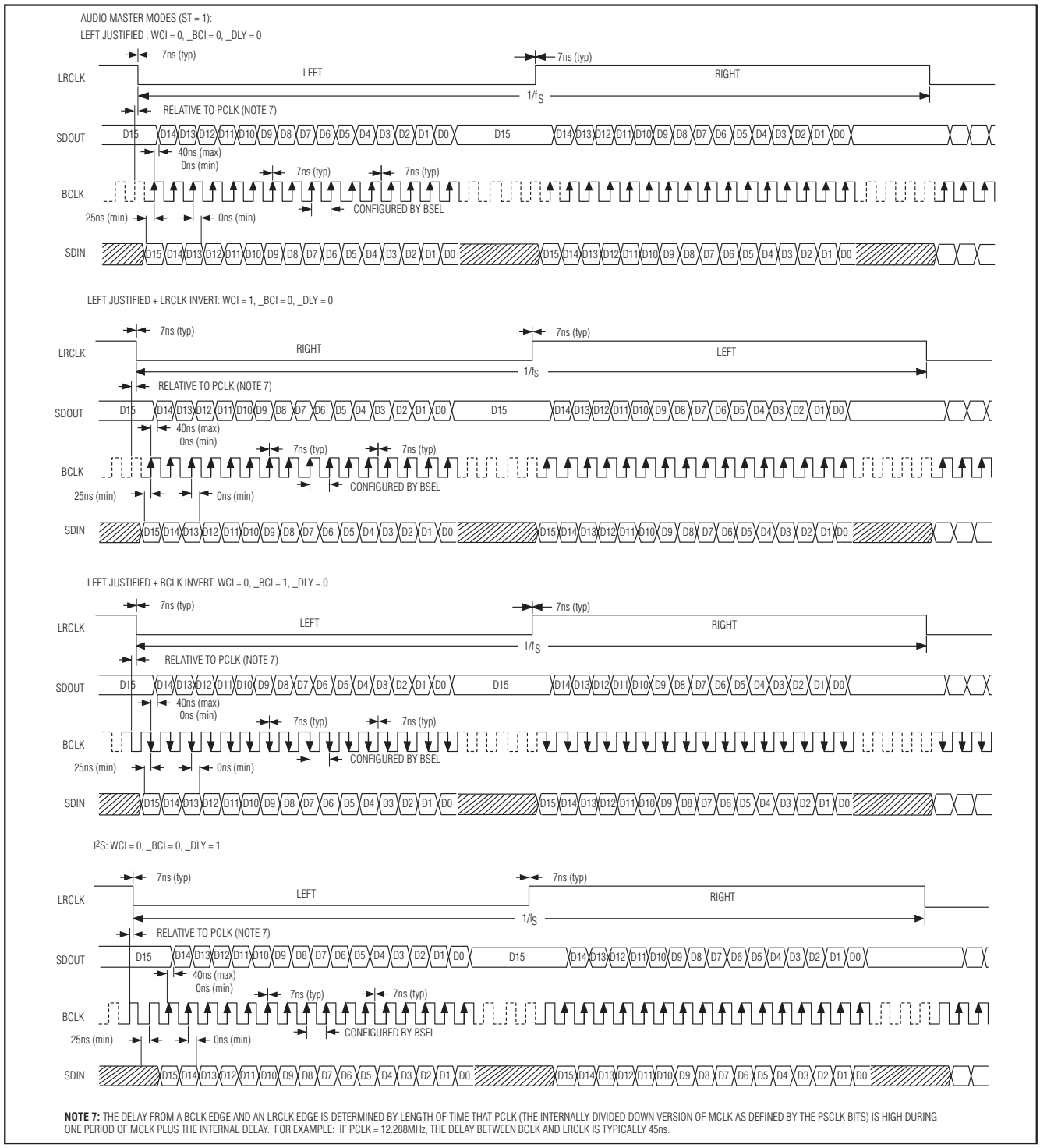
表5. 数字音频接口寄存器

REGISTER ADDRESS	B7	B6	B5	B4	B3	B2	B1	B0
0x06	MAS	WCI	DBCI	DDLY	HIZ	TDM	0	0
0x07	0	0	ABCI	ADLY	ST	BSEL		

BITS	FUNCTION
MAS	**Master Mode** 0 = The MAX9860 operates in slave mode with LRCLK and BCLK configured as inputs. 1 = The MAX9860 operates in master mode with LRCLK and BCLK configured as outputs.
WCI	**LRCLK Invert** 0 = Left-channel data is input and output while LRCLK is low. 1 = Right-channel data is input and output while LRCLK is low. WCI is ignored when TDM = 1.
DBCI	**DAC BCLK Invert (must be set to ABCI)** In master and slave mode: 0 = SDIN is latched into the part on the rising edge of BCLK. 1 = SDIN is latched into the part on the falling edge of BCLK. In master mode: 0 = LRCLK changes state following the rising edge of BCLK. 1 = LRCLK changes state following the falling edge of BCLK.
DDLY	**DAC Delay Mode** 0 = SDIN data is latched on the first BCLK edge following an LRCLK edge. 1 = SDIN data is assumed to be delayed one BCLK cycle so that it is latched on the 2nd BCLK edge following an LRCLK edge (I^2S-compatible mode). DDLY is ignored when TDM = 1.
HIZ	**SDOUT High-Impedance Mode** 0 = SDOUT is set either high or low after all data bits have been transferred out of the part. 1 = SDOUT goes to a high-impedance state after all data bits have been transferred out of the part, allowing SDOUT to be shared by other devices. Use HIZ only when TDM = 1.
TDM	**TDM Mode Select** 0 = LRCLK signal polarity indicates left and right audio. 1 = LRCLK is a framing pulse which transitions polarity to indicate the start of a frame of audio data consisting of multiple channels. When operating in TDM mode the left channel is output immediately following the frame sync pulse. If right-channel data is being transmitted, the 2nd channel of data immediately follows the 1st channel data.
ABCI	**ADC BCLK Invert (must be set to DBCI)** 0 = SDOUT is valid on the rising edge of BCLK and transitions immediately after the rising edge. 1 = SDOUT is valid on the falling edge of BCLK and transitions immediately after the falling edge.

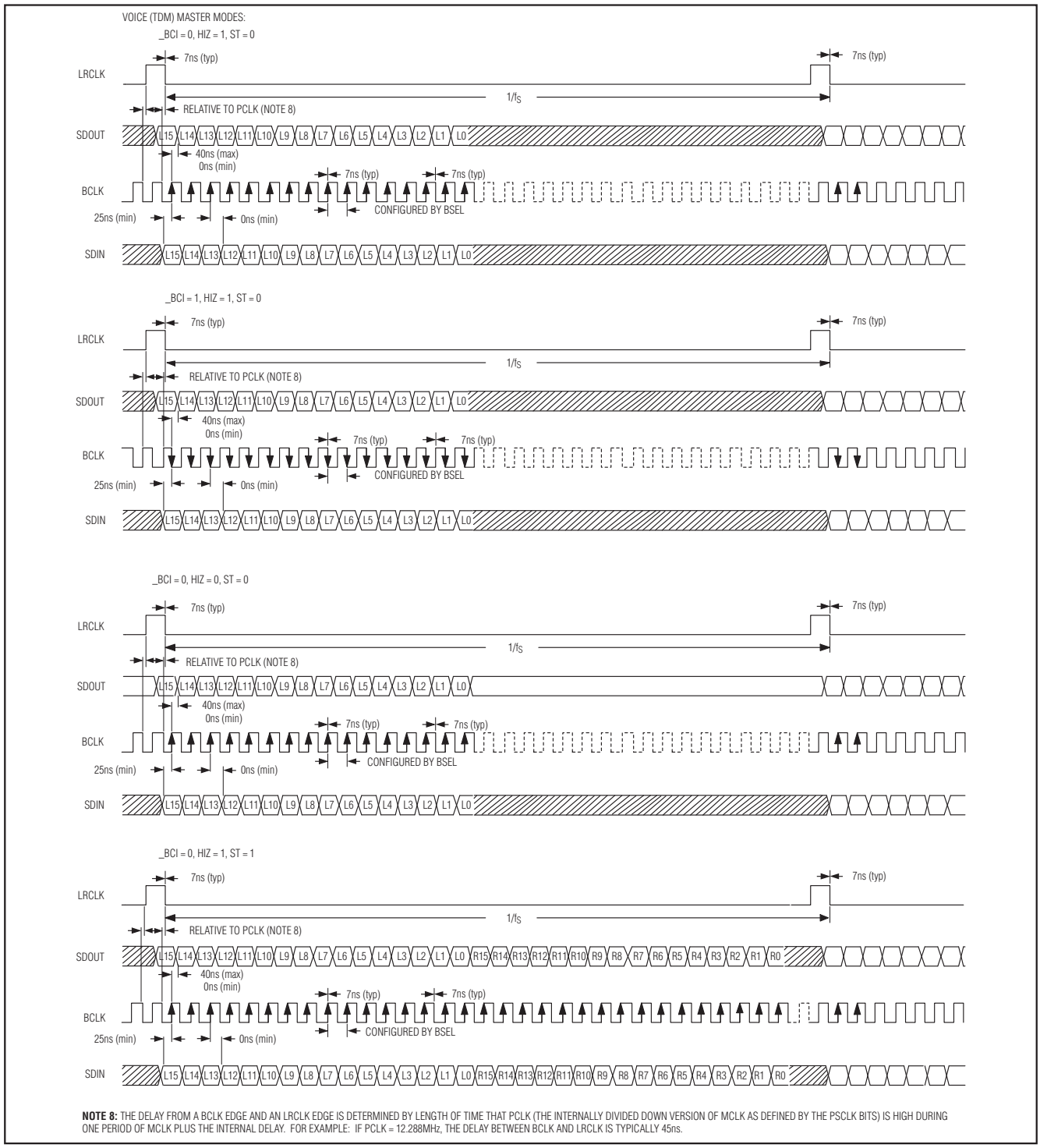
表5. 数字音频接口寄存器(续)

BITS	FUNCTION
ADLY	**ADC Delay Mode** 0 = SDOUT data is valid on the first BCLK edge following an LRCLK edge. 1 = SDOUT data is delayed one BCLK cycle so that it is valid on the 2nd BCLK edge following an LRCLK edge (I^2S-compatible mode). ADLY is ignored when TDM = 1.
ST	**Stereo Enable** 0 = The interface transmits and receives only one channel of data. If right record path is enabled, no data from this channel is transmitted. 1 = The interface operates in stereo. The left and right incoming data are summed to mono and then routed to the DAC. The summed data is divided by 2 to prevent overload. Both the left and right record signals are transmitted.
BSEL	**BCLK Select** Configures BCLK when operating in master mode. BSEL has no effect in slave mode. Set BSEL = 010, unless sharing the bus with multiple devices. 000 = Off 001 = 64x LRCLK (192x internal clock divided by 3) 010 = 48x LRCLK (192x internal clock divided by 4) 011 = Reserved for future use. 100 = PCLK/2 101 = PCLK/4 110 = PCLK/8 111 = PCLK/16



NOTE 7: THE DELAY FROM A BCLK EDGE AND AN LRCLK EDGE IS DETERMINED BY LENGTH OF TIME THAT PCLK (THE INTERNALLY DIVIDED DOWN VERSION OF MCLK AS DEFINED BY THE PSCLK BITS) IS HIGH DURING ONE PERIOD OF MCLK PLUS THE INTERNAL DELAY. FOR EXAMPLE: IF PCLK = 12.288MHz, THE DELAY BETWEEN BCLK AND LRCLK IS TYPICALLY 45ns.

图1. 数字音频接口音频主模式实例



NOTE 8: THE DELAY FROM A BCLK EDGE AND AN LRCLK EDGE IS DETERMINED BY LENGTH OF TIME THAT PCLK (THE INTERNALLY DIVIDED DOWN VERSION OF MCLK AS DEFINED BY THE PSCLK BITS) IS HIGH DURING ONE PERIOD OF MCLK PLUS THE INTERNAL DELAY. FOR EXAMPLE: IF PCLK = 12.288MHz, THE DELAY BETWEEN BCLK AND LRCLK IS TYPICALLY 45ns.

图2. 数字音频接口语音主模式实例

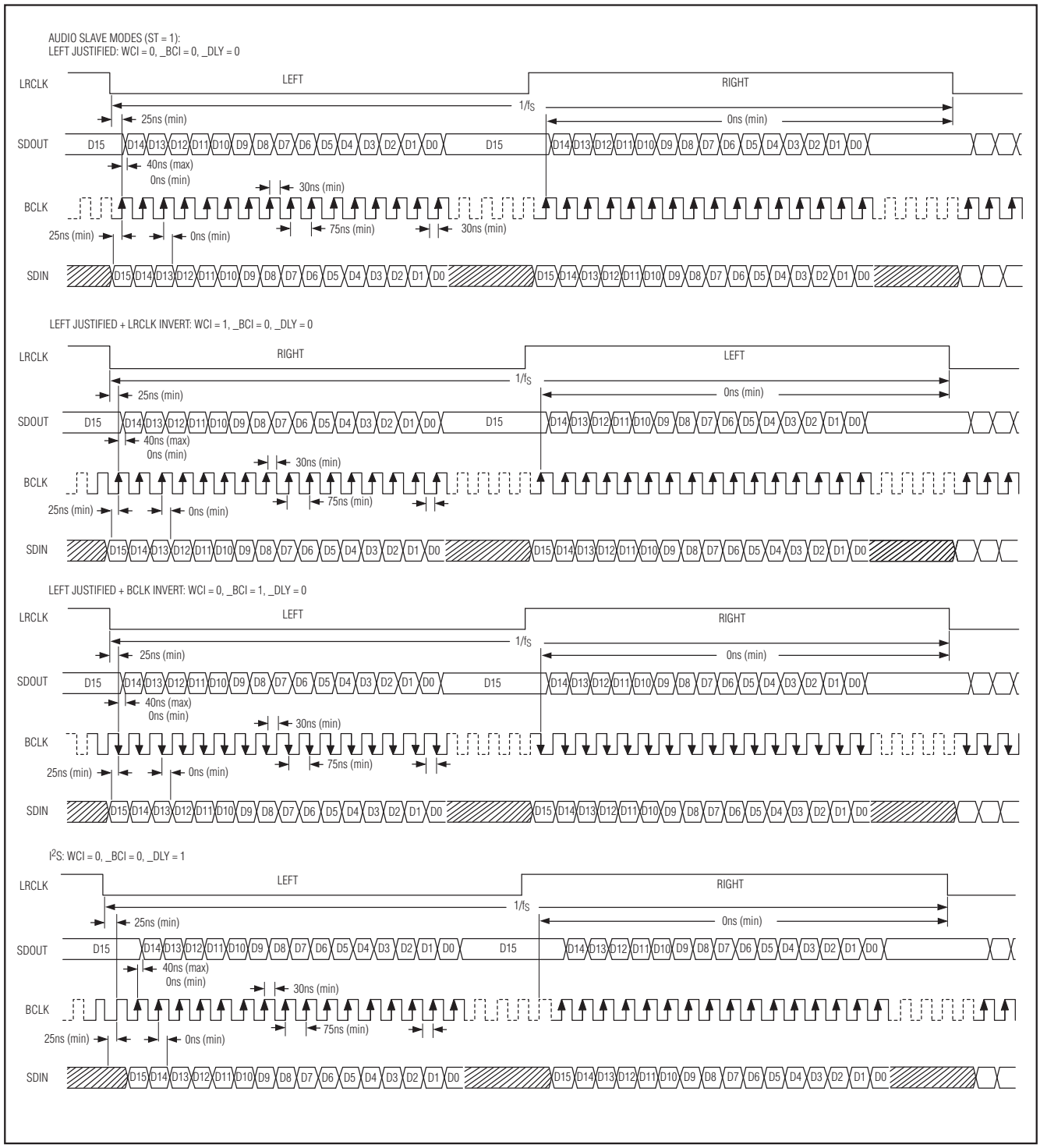


图3. 数字音频接口音频从模式实例

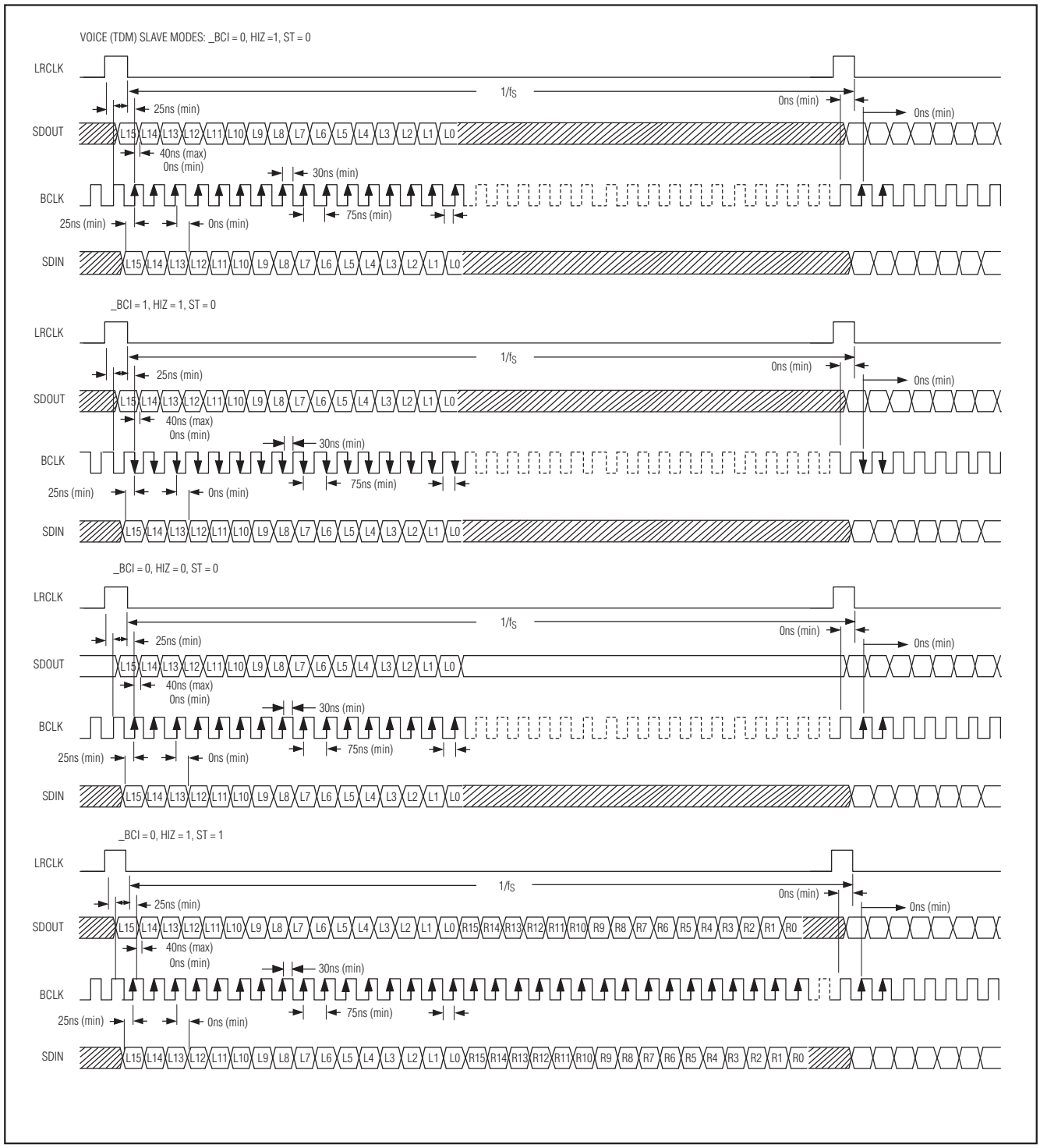


图4. 数字音频接口语音从模式实例

数字滤波

MAX9860带有可选的高通和陷波滤波器，可用于播放和录音通路。每个滤波器都针对特定的采样率。

表6. 数字滤波器寄存器

REGISTER ADDRESS	B7	B6	B5	B4	B3	B2	B1	B0
0x08	AVFLT				DVFLT			

BITS	FUNCTION
AVFLT	ADC Voice Filter Frequency Select. See Table 7.
DVFLT	DAC Voice Filter Frequency Select. See Table 7.

表7. 数字滤波器

CODE	FILTER TYPE	SAMPLE RATE	DESCRIPTION
0x0	—	—	Disabled
0x1	Elliptical	16kHz	Elliptical highpass with 217Hz notch
0x2	Butterworth	16kHz	500Hz Butterworth highpass
0x3	Elliptical	8kHz	Elliptical highpass with 217Hz notch
0x4	Butterworth	8kHz	500Hz Butterworth highpass
0x5	Butterworth	48kHz	200Hz Butterworth highpass
0x6 to 0xF	—	—	Reserved

数字电平控制

MAX9860为播放和录音通路提供了数字增益调整功能。两个录音通道的增益调整是独立的。器件还提供了侧音增益调整，用于设置相对于播放电平的侧音电平。

表8. 数字电平控制寄存器

REGISTER ADDRESS	B7	B6	B5	B4	B3	B2	B1	B0
0x09	DVA							
0x0A	ADCRL				ADCLL			
0x0B	0	DVG		DVST				

BITS	FUNCTION					
DVA	DAC Level Adjust Adjusts the digital audio level before being converted by the DAC. The least significant bit of DVA is always 0.					
	CODE	**GAIN**	**CODE**	**GAIN**	**CODE**	**GAIN**
	0x00	+3	0x40	-29	0x80	-61
	0x02	+2	0x42	-30	0x82	-62
	0x04	+1	0x44	-31	0x84	-63
	0x06	0	0x46	-32	0x86	-64
	0x08	-1	0x48	-33	0x88	-65
	0x0A	-2	0x4A	-34	0x8A	-66
	0x0C	-3	0x4C	-35	0x8C	-67
	0x0E	-4	0x4E	-36	0x8E	-68
	0x10	-5	0x50	-37	0x90	-69
	0x12	-6	0x52	-38	0x92	-70
	0x14	-7	0x54	-39	0x94	-71
	0x16	-8	0x56	-40	0x96	-72
	0x18	-9	0x58	-41	0x98	-73
	0x1A	-10	0x5A	-42	0x9A	-74
	0x1C	-11	0x5C	-43	0x9C	-75
	0x1E	-12	0x5E	-44	0x9E	-76
	0x20	-13	0x60	-45	0xA0	-77
	0x22	-14	0x62	-46	0xA2	-78
	0x24	-15	0x64	-47	0xA4	-79
	0x26	-16	0x66	-48	0xA6	-80
	0x28	-17	0x68	-49	0xA8	-81
	0x2A	-18	0x6A	-50	0xAA	-82
	0x2C	-19	0x6C	-51	0xAC	-83
	0x2E	-20	0x6E	-52	0xAE	-84
	0x30	-21	0x70	-53	0xB0	-85
	0x32	-22	0x72	-54	0xB2	-86
	0x34	-23	0x74	-55	0xB4	-87
	0x36	-24	0x76	-56	0xB6	-88
	0x38	-25	0x78	-57	0xB8	-89
	0x3A	-26	0x7A	-58	0xBA	-90
	0x3C	-27	0x7C	-59	≥ 0xBC	MUTE
	0x3E	-28	0x7E	-60	—	—

表8. 数字电平控制寄存器(续)

<table>
<tr><th>BITS</th><th colspan="5">FUNCTION</th></tr>
<tr><td rowspan="18">ADCRL/ADCLL</td><td colspan="5">Left and Right ADC Output Level
Adjusts the digital audio level output by the ADCs.</td></tr>
<tr><td>CODE</td><td>GAIN</td><td colspan="3" rowspan="17"></td></tr>
<tr><td>0x0</td><td>+3</td></tr>
<tr><td>0x1</td><td>+2</td></tr>
<tr><td>0x2</td><td>+1</td></tr>
<tr><td>0x3</td><td>0</td></tr>
<tr><td>0x4</td><td>-1</td></tr>
<tr><td>0x5</td><td>-2</td></tr>
<tr><td>0x6</td><td>-3</td></tr>
<tr><td>0x7</td><td>-4</td></tr>
<tr><td>0x8</td><td>-5</td></tr>
<tr><td>0x9</td><td>-6</td></tr>
<tr><td>0xA</td><td>-7</td></tr>
<tr><td>0xB</td><td>-8</td></tr>
<tr><td>0xC</td><td>-8</td></tr>
<tr><td>0xD</td><td>-10</td></tr>
<tr><td>0xE</td><td>-11</td></tr>
<tr><td>0xF</td><td>-12</td></tr>
<tr><td rowspan="6">DVG</td><td colspan="5">DAC Gain
The gain set by DVG adds to the level set by DVA.</td></tr>
<tr><td>CODE</td><td>GAIN</td><td colspan="3" rowspan="5"></td></tr>
<tr><td>00</td><td>0</td></tr>
<tr><td>01</td><td>+6</td></tr>
<tr><td>10</td><td>+12</td></tr>
<tr><td>11</td><td>+18</td></tr>
<tr><td rowspan="18">DVST</td><td colspan="5">Sidetone
Sets the level of left ADC output mixed into the DAC.</td></tr>
<tr><td>CODE</td><td>GAIN</td><td>CODE</td><td>GAIN</td><td rowspan="17"></td></tr>
<tr><td>0x00</td><td>Disabled</td><td>0x10</td><td>-30</td></tr>
<tr><td>0x01</td><td>0</td><td>0x11</td><td>-32</td></tr>
<tr><td>0x02</td><td>-2</td><td>0x12</td><td>-34</td></tr>
<tr><td>0x03</td><td>-4</td><td>0x13</td><td>-36</td></tr>
<tr><td>0x04</td><td>-6</td><td>0x14</td><td>-38</td></tr>
<tr><td>0x05</td><td>-8</td><td>0x15</td><td>-40</td></tr>
<tr><td>0x06</td><td>-10</td><td>0x16</td><td>-42</td></tr>
<tr><td>0x07</td><td>-12</td><td>0x17</td><td>-44</td></tr>
<tr><td>0x08</td><td>-14</td><td>0x18</td><td>-46</td></tr>
<tr><td>0x09</td><td>-16</td><td>0x19</td><td>-48</td></tr>
<tr><td>0x0A</td><td>-18</td><td>0x1A</td><td>-50</td></tr>
<tr><td>0x0B</td><td>-20</td><td>0x1B</td><td>-52</td></tr>
<tr><td>0x0C</td><td>-22</td><td>0x1C</td><td>-54</td></tr>
<tr><td>0x0D</td><td>-24</td><td>0x1D</td><td>-56</td></tr>
<tr><td>0x0E</td><td>-26</td><td>0x1E</td><td>-58</td></tr>
<tr><td>0x0F</td><td>-28</td><td>0x1F</td><td>-60</td></tr>
</table>

麦克风输入

MAX9860提供了两路差分麦克风输入以及一个用于麦克风供电的低噪声1.55V麦克风偏置。在典型应用中，左声道麦克风用于记录语音信号，右声道麦克风用于记录背景噪声信号。对于那些仅需要一个麦克风的应用，只使用左声道麦克风输入，而不使用右声道ADC。麦克风信号经过两级增益放大，然后送至ADC。第一级提供可选的0dB、20dB或者30dB设置；第二级是一个可编程增益放大器(PGA)，从0dB至20dB可调，步长为1dB。PGA提供过零检测功能，将增益改变时的拉链噪声降至最小。麦克风输入结构的详图请参见图5。

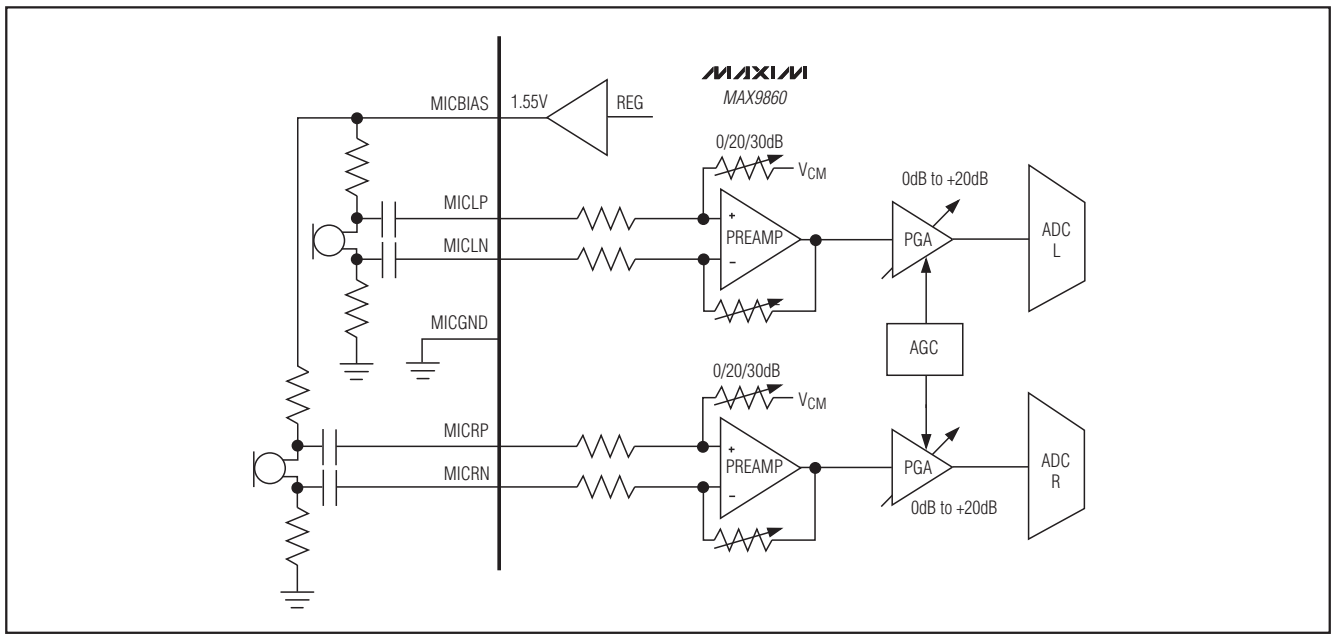


图5. 麦克风输入框图

表9. 麦克风输入寄存器

REGISTER ADDRESS	B7	B6	B5	B4	B3	B2	B1	B0
0x0C	0	PAM		PGAM				

BITS	FUNCTION
PAM	**Left and Right Microphone Preamp Gain** **CODE** / **GAIN (dB)**: 00 / Disabled; 01 / 0; 10 / +20; 11 / +30 **Note:** Selecting 00 disables the microphone inputs and microphone bias automatically.
PGAM	**Left and Right Microphone PGA** **CODE** / **GAIN (dB)** / **CODE** / **GAIN (dB)**: 0x00 / +20 / 0x0B / +9 0x01 / +19 / 0x0C / +8 0x02 / +18 / 0x0D / +7 0x03 / +17 / 0x0E / +6 0x04 / +16 / 0x0F / +5 0x05 / +15 / 0x10 / +4 0x06 / +14 / 0x11 / +3 0x07 / +13 / 0x12 / +2 0x08 / +12 / 0x13 / +1 0x09 / +11 / ≥ 0x14 / 0 0x0A / +10 / — / — **Note:** When AGC is enabled, the AGC controller overrides these settings.

自动增益控制(AGC)和噪声选通

MAX9860的两路麦克风输入均带有AGC。通过AGCHLD设置保持时间来使能AGC。AGC动态地控制模拟PGA麦克风输入增益，使电平在20dB输入范围内保持恒定，改善了各种条件下音频通路的性能。AGC使能时，器件将监测ADC输出处的信号电平，然后通过控制模拟麦克风PGA进行增益调整。当AGC使能时，PGAM不能被用户编程。

由于AGC增大了所有用户自定义门限以下的信号，所以噪底实际上增大了20dB。为了解决这一问题，器件提供了噪声选通功能，可降低低电平的增益。与常见噪声选通功能将低于门限的输出完全置于静音状态不同，MAX9860中的噪声选通是减小低于规定电平的信号增益。信号电平低于门限越多，增益降低得就越大。*典型工作特性*中的Automatic Gain Control Thresholds和Noise Gate Thresholds曲线图给出了使能AGC和噪声选通时的稳态传递曲线。

表10. AGC和噪声选通寄存器

REGISTER ADDRESS	B7	B6	B5	B4	B3	B2	B1	B0
0x0E	AGCSRC	AGCRLS			AGCATK		AGCHLD	
0x0F	ANTH				AGCTH			

BITS	FUNCTION
AGCSRC	**AGC/Noise Gate Signal Source Select** 0 = The left ADC output is used by the AGC and noise gate. 1 = The sum of the left and right ADC outputs is used by the AGC and noise gate.
AGCRLS	**AGC Release Time** Time taken by the AGC circuit to increase the gain from minimum to maximum.

CODE	TIME
000	78ms
001	156ms
010	312ms
011	625ms
100	1.25s
101	2.5s
110	5s
111	10s

BITS	FUNCTION
AGCATK	**AGC Attack Time** The time constant of the AGC gain reduction curve.

CODE	TIME (ms)
00	3
01	12
10	50
11	200

BITS	FUNCTION
AGCHLD	**AGC Hold Time** Time the AGC circuit waits before beginning to increase gain when a signal below the threshold is detected.

CODE	TIME (ms)
00	AGC disabled
01	50
10	100
11	400

表10. AGC和噪声选通寄存器(续)

<table>
<tr><th>BITS</th><th>FUNCTION</th></tr>
<tr><td>ANTH</td><td>Noise Gate Threshold
The signal level at which the noise gate begins reducing the gain. When the signal level is above the threshold the noise gate has no effect. When the signal level is below the threshold, the noise gate decreases the gain by 1dB for every 2dB the signal is below the threshold.

The noise gate can be enabled independently from AGC. When AGC is enabled, PGAM must be set to +20dB (indicating a small signal is present) for the noise gate to attenuate.

For microphone signals, use the noise gate and AGC simultaneously with ANTH set between -16dB and -28dB.
<table>
<tr><th>ANTH[3:0]</th><th>LEVEL (dBFS)</th><th>ANTH[3:0]</th><th>LEVEL (dBFS)</th></tr>
<tr><td>0x0</td><td>Disabled</td><td>0x8</td><td>-44</td></tr>
<tr><td>0x1</td><td>-72</td><td>0x9</td><td>-40</td></tr>
<tr><td>0x2</td><td>-68</td><td>0xA</td><td>-36</td></tr>
<tr><td>0x3</td><td>-64</td><td>0xB</td><td>-32</td></tr>
<tr><td>0x4</td><td>-60</td><td>0xC</td><td>-28</td></tr>
<tr><td>0x5</td><td>-56</td><td>0xD</td><td>-24</td></tr>
<tr><td>0x6</td><td>-52</td><td>0xE</td><td>-20</td></tr>
<tr><td>0x7</td><td>-48</td><td>0xF</td><td>-16</td></tr>
</table></td></tr>
<tr><td>AGCTH</td><td>AGC Signal Threshold
The target output signal level. When the signal level is below the threshold, the AGC increases the gain. The signal level is measured after ADCRL and ADCLL are applied to the ADC output.
<table>
<tr><th>ANTH[3:0]</th><th>LEVEL (dBFS)</th><th>ANTH[3:0]</th><th>LEVEL (dBFS)</th></tr>
<tr><td>0x0</td><td>-3</td><td>0x8</td><td>-11</td></tr>
<tr><td>0x1</td><td>-4</td><td>0x9</td><td>-12</td></tr>
<tr><td>0x2</td><td>-5</td><td>0xA</td><td>-13</td></tr>
<tr><td>0x3</td><td>-6</td><td>0xB</td><td>-14</td></tr>
<tr><td>0x4</td><td>-7</td><td>0xC</td><td>-15</td></tr>
<tr><td>0x5</td><td>-8</td><td>0xD</td><td>-16</td></tr>
<tr><td>0x6</td><td>-9</td><td>0xE</td><td>-17</td></tr>
<tr><td>0x7</td><td>-10</td><td>0xF</td><td>-18</td></tr>
</table></td></tr>
</table>

电源管理

MAX9860具有完整的电源管理控制，可最大程度降低功耗。DAC和两个ADC可以被分别使能，所以只有需要的电路被激活。

表11. 电源管理寄存器

REGISTER ADDRESS	B7	B6	B5	B4	B3	B2	B1	B0
0x10	$\overline{SHDN}$	0	0	0	DACEN	0	ADCLEN	ADCREN

BITS	FUNCTION
$\overline{SHDN}$	**Active-Low Software Shutdown** 0 = MAX9860 is in full shutdown. 1 = MAX9860 is powered on. When $\overline{SHDN}$ = 0. All register settings are preserved and the I²C interface remains active.
DACEN	**DAC Enable** 0 = DAC disabled. 1 = DAC enabled.
ADCLEN/ADCREN	**ADC Left/Right Enable** 0 = Left/right ADC enabled. 1 = Left/right ADC disabled. The left ADC must be enabled when using the right ADC.

版本编码

MAX9860带有一个版本编码，可方便识别器件版本。当前的版本编码为0x40。

表12. 版本编码寄存器

ADDR	B7	B6	B5	B4	B3	B2	B1	B0
0xFF	REV							

I²C串行接口

MAX9860采用I²C/SMBus™兼容的2线串行接口，包括一根串行数据线(SDA)和一根串行时钟线(SCL)。SDA和SCL的时钟速率高达400kHz，方便了MAX9860和主机之间的通信。图6所示为2线接口的时序图。主机在总线上产生SCL并发起数据传输。主机发送相应的从地址、随后跟寄存器地址、紧接着发送数据字，以向MAX9860写入数据。每一个传输序列由START (S)或REPEATED START (Sr)条件和STOP (P)条件构成帧。发送至MAX9860的每个字长为8位，其后是应答时钟脉冲。主机从MAX9860读取数据时，发送相应的从地址，随后紧接着9个SCL脉冲。MAX9860通过SDA发送数据，与主机产生的SCL脉冲同步。主机在接收到每字节的数据后将对其进行应答。每一个读序列由START或REPEATED START条件、非应答和STOP条件构成帧。SDA既是输入又是开漏输出。SDA上需要一个上拉电阻，通常大于500Ω。SCL仅作为输入。如果总线上有多个主机，或者单主机具有开漏SCL输出，SCL上则需要一个上拉电阻，通常大于500Ω。SDA和SCL线上的串联电阻是可选的。串联电阻保护MAX9860的数字输入免受总线上高压毛刺的损坏，并最大程度降低总线信号的串扰和下冲。

SMBus是Intel Corp.的商标。

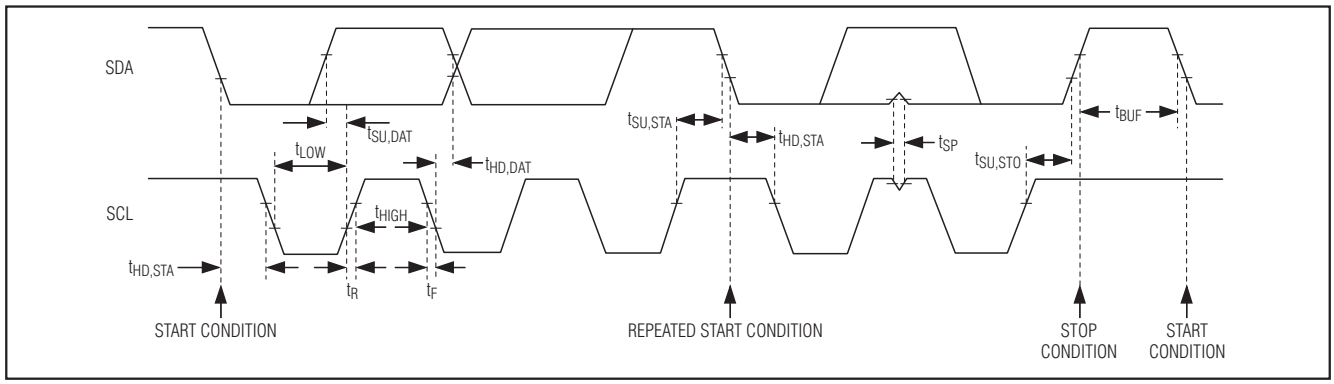


图6. 2线接口时序图

位传输

每个SCL周期传输一个数据位。在SCL脉冲的高电平期间内，SDA上的数据必须保持稳定。当SCL为高电平时，SDA上的变化表示控制信号(请参见*START和STOP条件*部分)。

START和STOP条件

总线空闲时，SDA和SCL的空闲状态为高电平。主机通过发送START (S)条件来启动通信，START条件是SCL为高电平时，SDA由高到低的跳变。STOP (P)条件是SCL为高时，SDA由低到高的跳变(图7)。来自于主机的START条件通知MAX9860开始传输。主机通过发送STOP条件终止传输并释放总线。如果产生的是REPEATED START (Sr)条件而不是STOP条件，则总线保持有效。

提前STOP条件

MAX9860在数据传输期间可随时识别STOP条件，除非STOP条件与START条件出现在同一高电平脉冲。为了正常工作，请勿在与START条件相同的SCL高电平脉冲期间发送STOP条件。

从地址

从地址定义为7个最高位(MSB)，后边跟读/写控制位。对于MAX9860，7个最高位为0010000。将读/写控制位设置为1 (从地址 = 0x21)可将MAX9860配置为读模式。将读/写控制位设置为0 (从地址 = 0x20)可将MAX9860配置为写模式。该地址是在START条件后发送到MAX9860的信息的第一个字节。

应答

在写入模式时，应答位(ACK)是第9个时钟位，是MAX9860对其接收的每个数据字节的握手信号(见图8)。如果成功地接收了之前的字节，那么MAX9860在主机产生的第9个时钟脉冲期间内拉低SDA。监视ACK可以检测失败的数据传输。如果接收器件忙或者系统发生故障，则会出现失败的数据传输。若数据传输失败，总线主机会重试通信。当MAX9860处于读模式时，在第9个时钟脉冲期间，主机拉低SDA来应答数据的接收。每次读取字节后，主机均发送应答信号，使数据继续传输。当主机从MAX9860读取数据的最后字节时，发送非应答，随后是STOP条件。

写数据格式

对MAX9860的写操作包括START条件、从机地址和R/$\overline{W}$位(置0)、用来配置内部寄存器地址指针的一个数据字节、1个或多个数据字节和STOP条件。图9所示为向MAX9860写入1个字节数据时的正确帧格式。图10所示为向MAX9860写入n个字节数据时的正确帧格式。

R/$\overline{W}$位被设置为0的从地址表示主机要向MAX9860写数据。MAX9860在主机产生的第9个SCL脉冲期间应答接收到的地址。

从主机发送的第二字节配置MAX9860的内部寄存器地址指针。指针告诉MAX9860写入下一个字节的位置。MAX9860在接收到地址指针数据后发送应答脉冲。

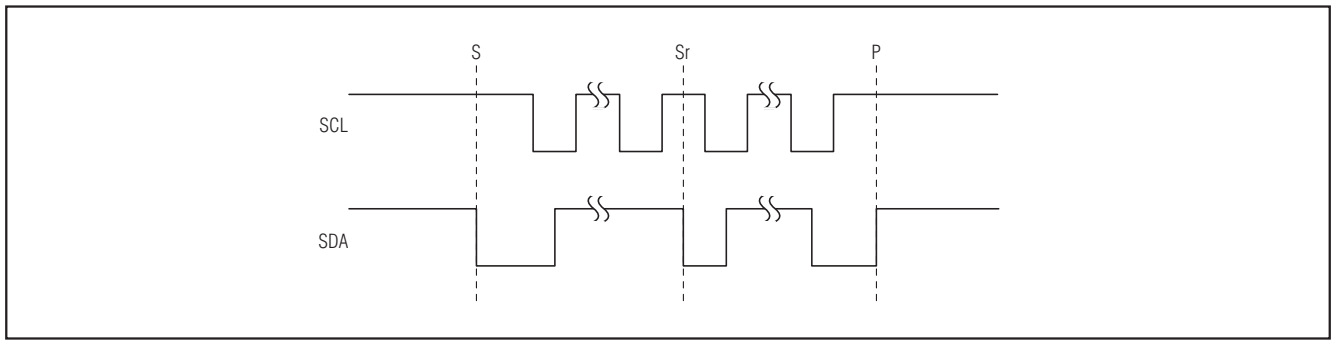


图7. START (S)、STOP (P)和REPEATED START (Sr)条件

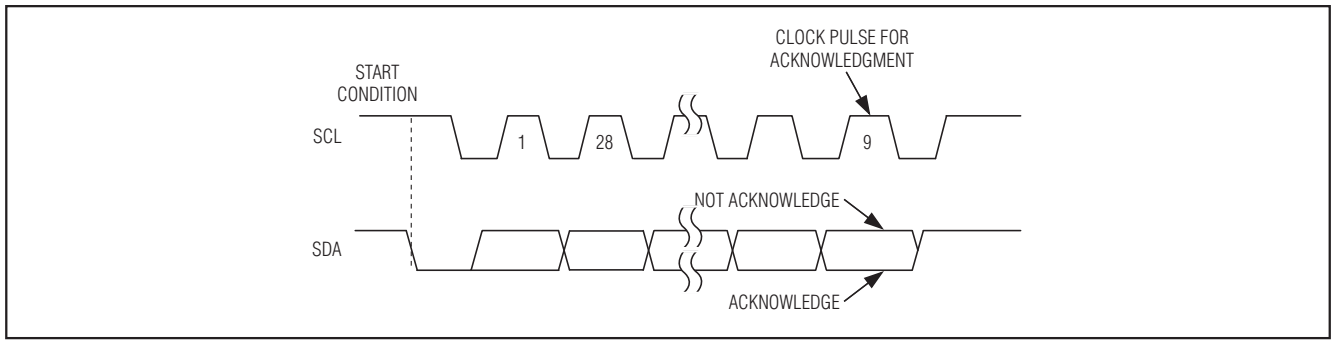


图8. 应答

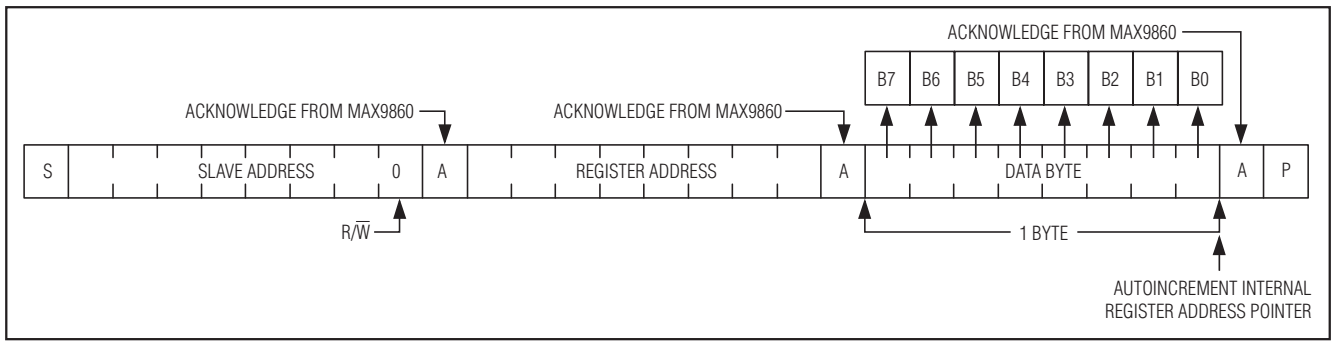


图9. 向MAX9860写入1个数据字节

发送到MAX9860的第三字节为写入指定寄存器的数据。MAX9860发送应答脉冲表示接收到数据字节。每次接收数据之后，地址指针自动递增至下一个寄存器地址。自动递增特性使主机能够在一个连续帧内对连续的寄存器进行写操作。图10所示为如何用一个帧写入多个寄存器。主机通过发送STOP条件，终止传输。大于0x10的寄存器地址被保留。不要对这些地址进行写操作。

读数据格式

通过发送从地址，并将R/$\overline{W}$位置1，启动读操作。MAX9860在第9个SCL时钟脉冲期间拉低SDA，应答接收到的从地址。START条件后跟读命令，将地址指针复位为寄存器0x00。

从MAX9860发送的第一个字节是寄存器0x00的内容。发送的数据在SCL的上升沿有效。地址指针在每次读取数据字

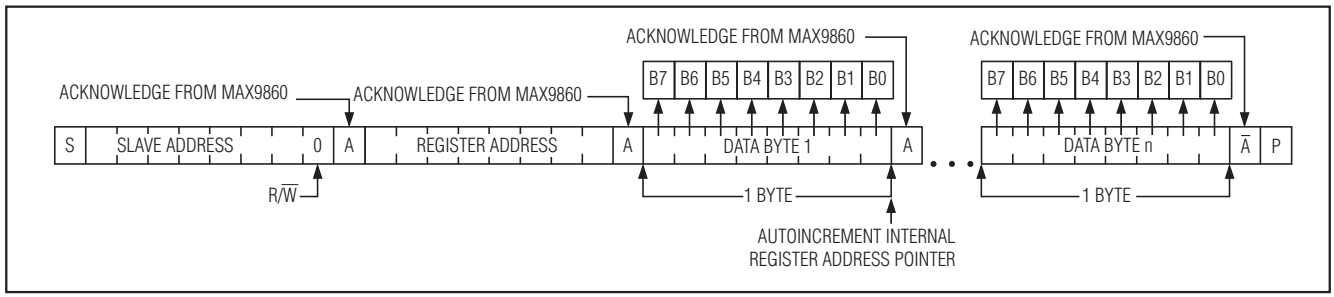


图10. 向MAX9860写入N个字节数据

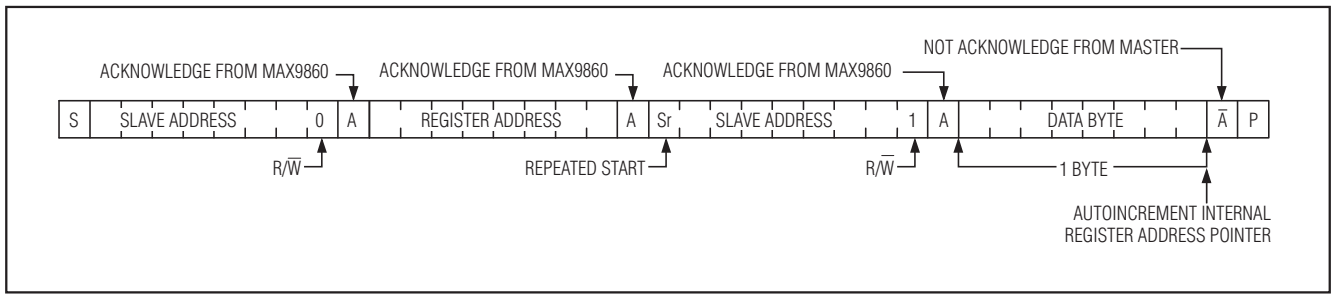


图11. 从MAX9860读取1个字节的数据

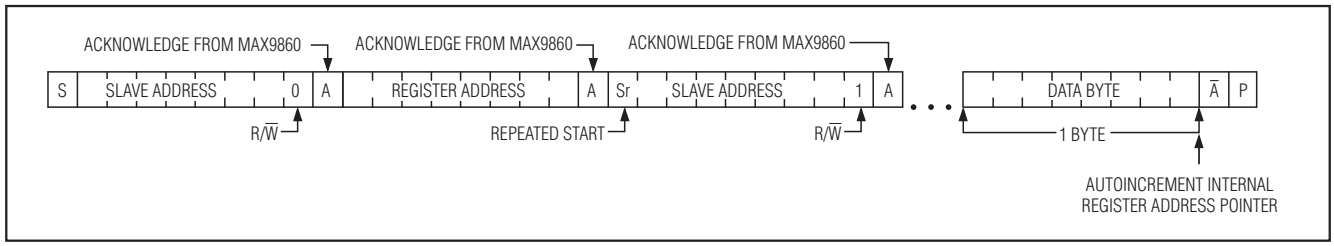


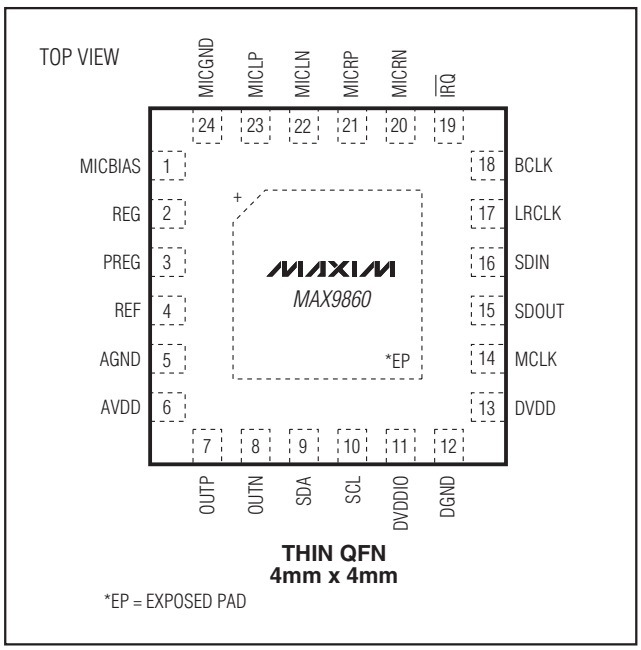
图12. 从MAX9860读取N个字节的数据

节后都自动递增。这种自动递增功能使得在一个连续帧内即可连续读取全部的寄存器。读数据字节的任意过程中，可发送STOP (P)条件。如果发送了一个STOP条件，其后又跟随另一个读操作，则读取的第一个字节为寄存器0x00的数据。

发送读命令之前，可将地址指针预置到一个特定的寄存器。主机通过首先发送MAX9860的从地址，并将R/$\overline{W}$位置为0，然后再发送寄存器地址来预置地址指针。之后发送REPEATED START (Sr)条件，然后紧接发送从地址并将R/$\overline{W}$位置为1。MAX9860随后发送指定寄存器中的内容。发送完第一个字节后，地址指针自动递增。

主机在应答时钟脉冲期间对每个接收到的字节进行应答。主机必须应答除最后一个字节之外的所有成功接收的字节。最后一个字节之后是由主机发送的非应答信号，然后是STOP条件。图11给出了从MAX9860读取一个字节的帧格式，图12所示为从MAX9860读取多个字节的帧格式。

引脚配置



应用信息

适当的布局和接地对获得最佳性能至关重要。设计MAX9860的PCB时，适当的电路隔离可以将MAX9860的模拟部分与数字部分分开。这样保证了模拟音频走线不会出现在数字走线附近。

在PCB的专用层上使用大面积连续接地层可以最小化环路面积。采用尽可能短的走线将AGND、DGND和MICGND直接连接至接地面。适当的接地可改善音频性能、最大程度降低通道之间的串扰，并可防止数字噪声耦合至模拟音频信号。

以最短的走线长度将REG、PREG和REF上的旁路电容直接连接至接地面。还要确保连接至AGND和MICGND的通路长度最短。将AVDD直接旁路至AGND。将MICBIAS直接旁路至MICGND。

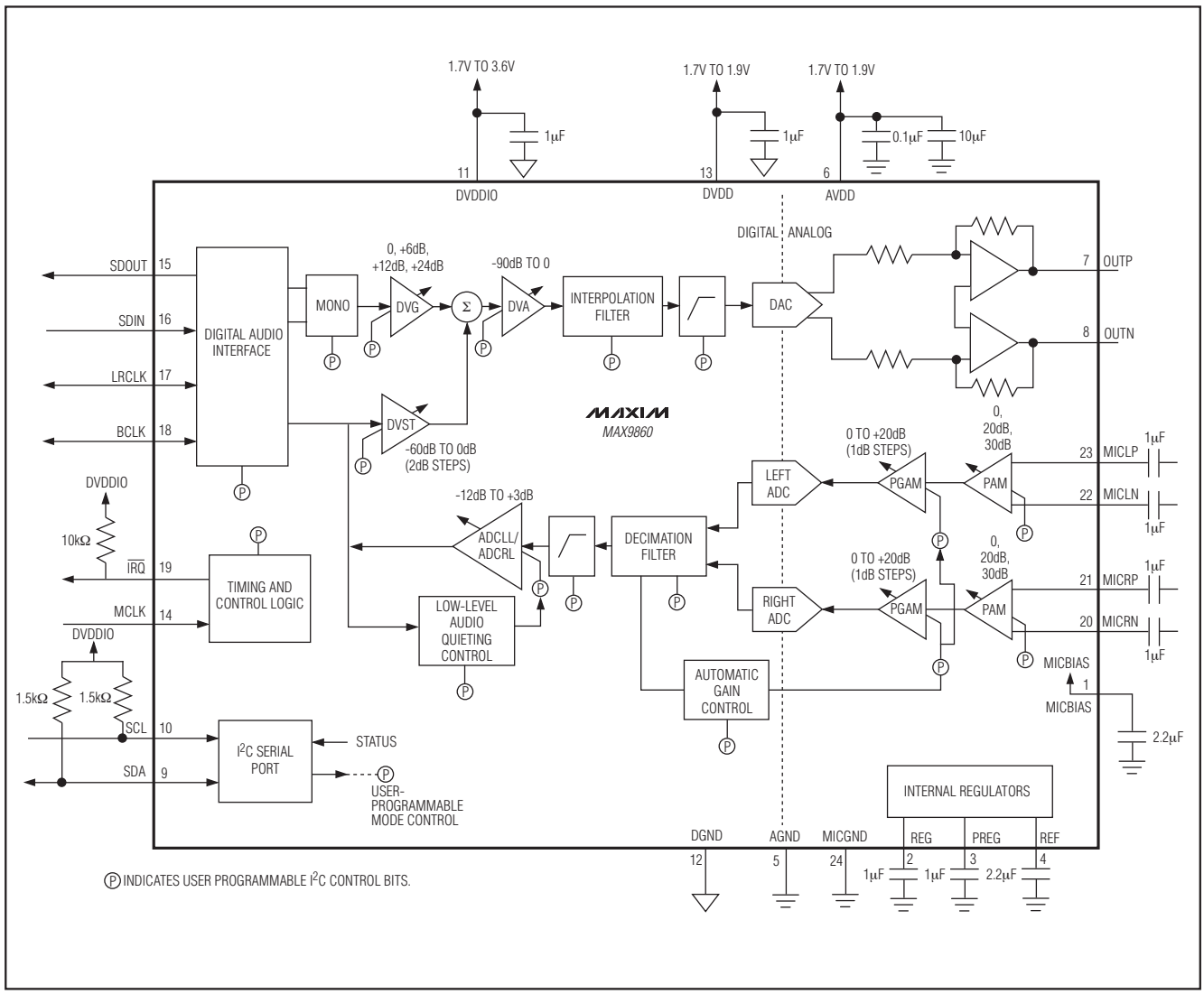
以最短的通路长度，将端接至接地层的所有数字I/O端子连接至DGND。将DVDD和DVDDIO直接旁路至DGND。

把麦克风至MAX9860的麦克风信号以差分对方式布线，确保正和负信号尽可能靠近、并且具有相同的走线长度。当使用单端麦克风或其它单端音频源时，在尽量靠近音频源的位置将负麦克风输入信号交流接地，然后将正和负走线作为差分对。

MAX9860的薄型QFN封装下方有一个裸焊盘，该焊盘提供了从管芯到PCB的直接导热通路，可降低封装的热阻。请将该裸焊盘连接到AGND。

现备有一个评估板(EV kit)，可作为MAX9860的PCB布局实例。利用该评估板可快速设置MAX9860，并提供了易于使用的软件，用于控制其内部寄存器。

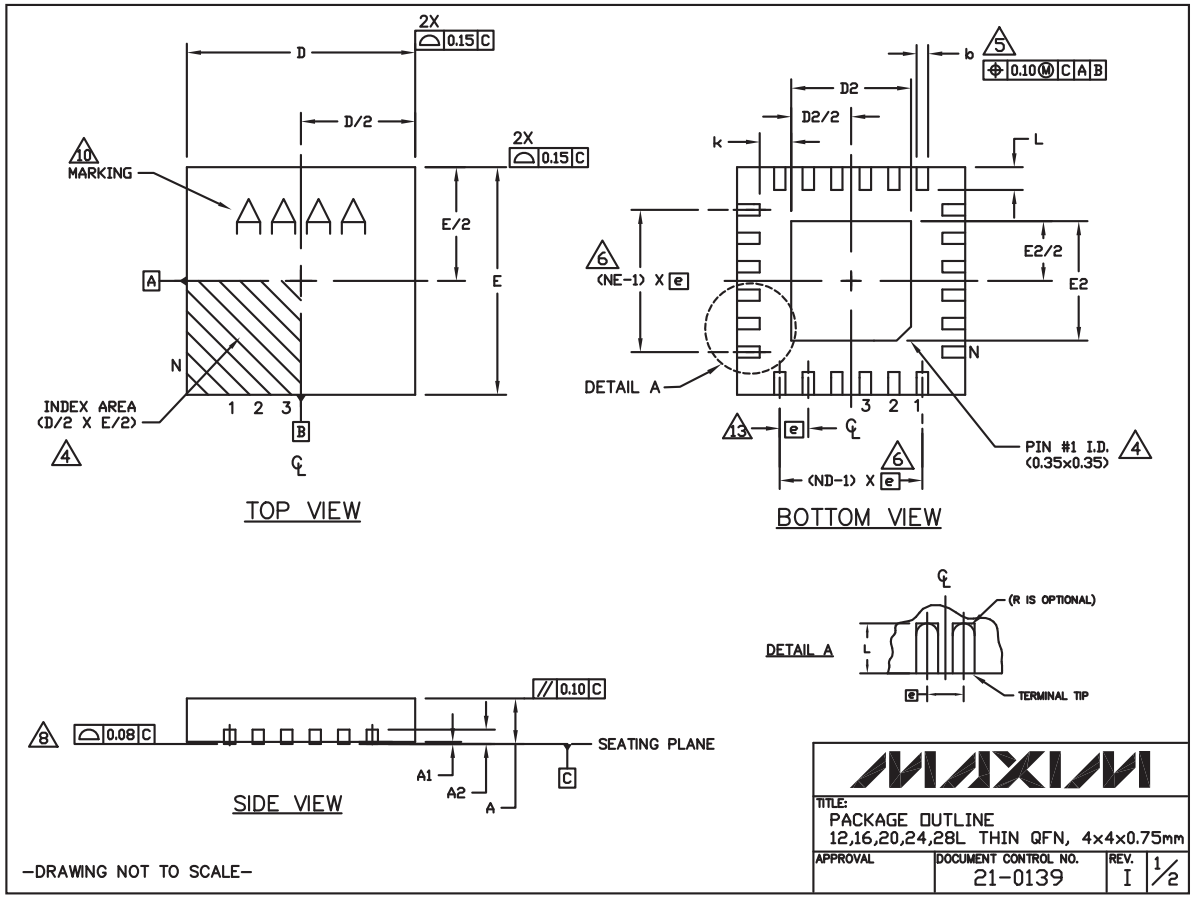
功能框图/典型工作电路


1.7V TO 3.6V
1.7V TO 1.9V
1.7V TO 1.9V
1µF
1µF
0.1µF
10µF
11
DVDDIO
13
DVDD
6
AVDD
DIGITAL
ANALOG
SDOUT 15
SDIN 16
LRCLK 17
BCLK 18
DIGITAL AUDIO INTERFACE
MONO
0, +6dB, +12dB, +24dB
DVG
Σ
-90dB TO 0
DVA
INTERPOLATION FILTER
DAC
7 OUTP
8 OUTN
DVST
-60dB TO 0dB (2dB STEPS)
MAXIM
MAX9860
0 TO +20dB (1dB STEPS)
0, 20dB, 30dB
LEFT ADC
PGAM
PAM
23 MICLP
22 MICLN
1µF
1µF
DVDDIO
10kΩ
IRQ 19
MCLK 14
TIMING AND CONTROL LOGIC
-12dB TO +3dB
ADCLL/ ADCRL
DECIMATION FILTER
RIGHT ADC
PGAM
PAM
21 MICRP
20 MICRN
1µF
1µF
LOW-LEVEL AUDIO QUIETING CONTROL
AUTOMATIC GAIN CONTROL
MICBIAS
1
MICBIAS
2.2µF
DVDDIO
1.5kΩ
1.5kΩ
SCL 10
SDA 9
I²C SERIAL PORT
STATUS
USER-PROGRAMMABLE MODE CONTROL
INTERNAL REGULATORS
DGND
12
AGND
5
MICGND
24
REG
2
PREG
3
REF
4
1µF
1µF
2.2µF
Ⓟ INDICATES USER PROGRAMMABLE I²C CONTROL BITS.

封装信息

如需最近的封装外形信息和焊盘布局，请查询 **www.maxim-ic.com.cn/packages**。

封装类型	封装编码	文档编号
24 TQFN-EP	T2444+4	**21-0139**



封装信息(续)

如需最近的封装外形信息和焊盘布局，请查询 **www.maxim-ic.com.cn/packages**。

COMMON DIMENSIONS																
PKG	12L 4x4			16L 4x4			20L 4x4			24L 4x4			28L 4x4			
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	
A1	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	
A2	0.20 REF			0.20 REF			0.20 REF			0.20 REF			0.20 REF			
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.18	0.23	0.30	0.15	0.20	0.25	
D	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	
E	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.			
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	
L	0.45	0.55	0.65	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50	
N	12			16			20			24			28			
ND	3			4			5			6			7			
NE	3			4			5			6			7			
Jedec Var.	WGGB			WGGC			WGGD-1			WGGD-2			WGGE			

EXPOSED PAD VARIATIONS						
PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T1244-3	1.95	2.10	2.25	1.95	2.10	2.25
T1244-4	1.95	2.10	2.25	1.95	2.10	2.25
T1644-3	1.95	2.10	2.25	1.95	2.10	2.25
T1644-4	1.95	2.10	2.25	1.95	2.10	2.25
T2044-2	1.95	2.10	2.25	1.95	2.10	2.25
T2044-3	1.95	2.10	2.25	1.95	2.10	2.25
T2444-2	1.95	2.10	2.25	1.95	2.10	2.25
T2444-3	2.45	2.60	2.63	2.45	2.60	2.63
T2444-4	2.45	2.60	2.63	2.45	2.60	2.63
T2444N-4	2.45	2.60	2.63	2.45	2.60	2.63
T2444M-1	2.45	2.60	2.63	2.45	2.60	2.63
T2844-1	2.50	2.60	2.70	2.50	2.60	2.70

NOTES:
1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR T2444-3, T2444-4 AND T2844-1.
10. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
11. COPLANARITY SHALL NOT EXCEED 0.08mm.
12. WARPAGE SHALL NOT EXCEED 0.10mm.
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION 'e', ±0.05.
14. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
15. ALL DIMENSIONS ARE THE SAME FOR LEADED (-) & PbFREE (+) PACKAGE CODES.

-DRAWING NOT TO SCALE-

MAXIM

TITLE:
PACKAGE OUTLINE
12,16,20,24,28L THIN QFN, 4x4x0.75mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0139	I	2/2

Maxim北京办事处

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