

A Combined Socketed and Non-Socketed CDM Test Approach for Eliminating Real-World CDM Failures

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Abstract

Of 30 bipolar, BiCMOS, and CMOS products socketed CDM classified, 27 had $\geq 500\text{V}$ withstand voltages and experienced no real-world CDM fallout. Two of three products with $< 500\text{V}$ withstand voltages had numerous manufacturing-induced CDM failures until they were analyzed and redesigned. Analysis of these two products showed that both socketed and non-socketed CDM testing replicated the initial dielectric breakdown failure mechanisms at the same failure sites identified on real-world CDM failures. However, socketed CDM testing consistently induced more severe damage than non-socketed CDM testing. On one product, this resulted in a completely different failure mode than that on the socketed CDM and real-world failures. Based on this work, a combined socketed and non-socketed CDM test approach is proposed for classifying/evaluating new products and driving CDM robustness improvements.

Introduction

As semiconductor manufacturing, handling, and Printed Circuit Board (PCB) assembly operations become increasingly automated, Charged Device Model (CDM) classification testing of new ICs is becoming a necessity. CDM test results on a new product nearing production release can be used to predict future CDM-related manufacturing fallout, both during IC production and during PCB assembly. For released products, baseline failure analysis (FA) results on CDM classification rejects can facilitate rapid identification of CDM-related problems during manufacturing or field application. Most importantly, for both unreleased and released products, FA results on CDM failures can drive redesigns to boost CDM classification levels to effectively eliminate real-world CDM failures.

While its value is clear, developing an appropriate approach to CDM testing is difficult. Two general “competing” CDM test methods exist: non-socketed, (ns, also referred to as robotic), and socketed (s). ESD Association Draft Standard DS5.3 [1] includes waveform calibration and classification procedures for both these general CDM test methods. DS5.3 further subdivides these two methods based on the discharge mode: non-contact mode (nc), whereby the discharge is air-based, or contact mode (c), whereby the discharge is relay-based. Previous studies have concluded that non-contact mode CDM testing best replicates real-world CDM failures [2-4], but contact mode CDM testing generally provides satisfactory simulation of such failures [5-7] while offering advantages such as excellent waveform repeatability, ease of testing, high throughput, and *in-situ* electrical test capability [3,6,8]. For non-socketed CDM testing, DS5.3 provides two general options for component charging: field-induced charging or direct charging. Due to all these options, significant flexibility exists in the application of DS5.3. However, this flexibility along with metrology, correlation, and other issues have impeded full CDM standardization, and have often made drawing valid conclusions from industry CDM test results difficult.

This paper initially discusses the results of DS5.3 socketed CDM classification testing on 30 products fabricated on a broad range of technologies. Next, the results of an extensive analysis of three products with low socketed CDM robustness are presented, including comparisons of socketed and non-socketed test results and discussions of full root cause FA results. The redesigns undertaken to improve the CDM robustness of the three products are then described. Finally, a combined socketed and non-socketed test approach for predicting CDM

fallout and driving CDM improvements is outlined. The primary objectives were that this test approach (1) Meet the requirements of DS5.3; (2) Generate rejects with failure modes/locations/mechanisms that matched those on real-world CDM failures; and (3) Be suitable for implementation as a cost-effective method for quickly evaluating the CDM susceptibility of new products in a production environment.

SCDM Classification Testing

Ten bipolar, ten BiCMOS, and ten CMOS products covering a wide range of process and package technologies were initially selected for CDM analysis. Fabrication technologies ranged from a $625\mu\text{m}^2$ emitter bipolar process to a $0.5\mu\text{m}$ gate length CMOS process, and package lead counts ranged from 3 to 160 (see Appendices 1-3). These 30 products have been in high volume production (generally $>10\text{k}$ units/month) for anywhere from one month to >10 years. After passing automatic test equipment (ATE) testing to data sheet limits, 15 samples of each product were subjected to contact mode Socketed CDM (hereafter referred to as "SCDM") classification testing per DS5.3 using a commercially-available relay-based automated ESD test system. Products on a junction-isolated (JI) process were charged through the substrate pin(s), while products on a dielectrically-isolated (DI) process were charged through the pin(s) tied directly to the bulk diffusions comprising the field area outside the DI trenches. The device under test (DUT) boards used throughout the testing were vendor-supplied and met the discharge waveform requirements of DS5.3, though the measured waveforms varied substantially based on differences in DUT board parasitics. Consistent with DS5.3 requirements, for each product, three fresh samples were stressed at each of the following five charge voltage levels: ± 125 , 250, 500, 1000, & 1500V. [Note that $\pm 1500\text{V}$ was the maximum test capability of the particular test system used.] After stressing, each of the samples was again ATE tested to data sheet limits, with the SCDM withstand voltage defined as the highest level at which all samples met *all* data sheet electrical test limits. The results of this classification testing are summarized in Figure 1 and are detailed in Appendices 1-3.

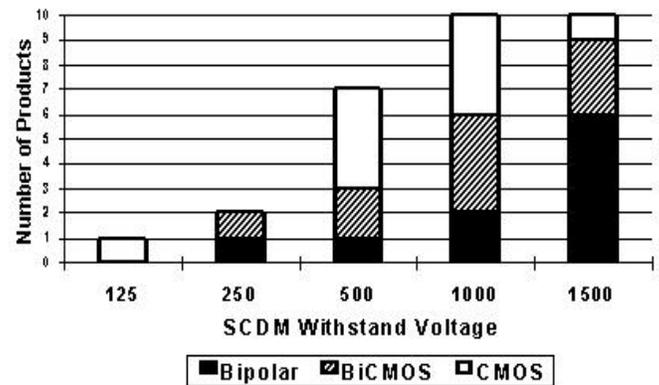


Fig. 1: SCDM Withstand Voltages on 30 products tested (10 Bipolar, 10 BiCMOS, & 10 CMOS)

Real-World CDM Results

The final column of Appendices 1-3 shows the real-world CDM failure rate for the 30 SCDM classified products. These qualitative failure rates were determined from an extensive review of databases of final electrical test fallout, outgoing electrical PPMs, and FA results for the 30 products. Since FAs were not conducted on every manufacturing reject and since end customers do not generally return every failure for FA, calculating exact CDM-related failure rates was not possible. However, either full root cause FAs or "signature" FAs were conducted on *all* customer returned products, and at least signature FAs were conducted on *many* outgoing electrical PPM rejects. Any product with suspected ESD damage that could not be simulated by the Human Body Model (HBM) or Machine Model (MM) was CDM tested in an attempt to replicate the failure mode and/or failure mechanism documented on the real-world failure. Prior to the procurement of automated CDM test equipment in '93, testing was conducted on a manual non-socketed, contact mode CDM test system built in accordance with [9]. Although this system did not meet DS5.3 waveform requirements, it simulated the characteristic dielectric breakdown damage documented on real-world failures on product Bipolar2. Thus, even for the products in Appendices 1-3 that were released prior to '93, FA and related databases captured CDM failure information. Products with CDM failure rates listed as ~ 0 have had no documented real-world CDM ESD failures, while *estimates* of the "moderate" and "high" failure rate categories are in the few 100 and few 1000 PPM range, respectively.

Table 1: CDM Results on Three Focus Products

Product	Family	SCDM Failure Mode	NSCDM Failure Mode	Real-World CDM Failure Mode
Bipolar2	Voltage Reference	Non-functional at $\geq 500V$. Pin 1 resistively shorted to Gnd.	Non-functional at $\geq 500V$. Pin 1 resistively shorted to Gnd.	Non-functional. Pin 1 resistively shorted to Gnd.
BiCMOS3	Operational Amplifier	Non-functional at $\geq 500V$. Pin 1 open to Gnd (forward bias).	Non-functional at $\geq 500V$. Pin 1 resistively shorted to Gnd.	Non-functional. Pin 1 resistively shorted to Gnd.
CMOS5	Analog-to-Digital Converter	Excessive Driver Supply Current at $\geq 250V$. No pin-to-pin curve tracer anomalies.	Excessive Driver Supply Current at $\geq 1000V$. No pin-to-pin curve tracer anomalies.	Not Applicable. No such failures detected to date.

NSCDM Classification Testing

The three products with $<500V$ SCDM withstand voltages (i.e., Bipolar2, BiCMOS3, and CMOS5) were subsequently subjected to non-contact mode Non-Socketed (hereafter referred to as “NSCDM”) classification testing per ESD Association DS5.3 using a commercially-available automated robotic CDM ESD test system. [The 27 other products listed in Appendices 1-3 were not subjected to NSCDM testing since they have satisfactory SCDM robustness and have no history of any real-world CDM failures.] For each of the three focus products, charging was conducted directly through the P-type substrate pin. Direct charging (rather than field-induced charging) was selected to provide consistency with the SCDM charge method. As with the SCDM testing, three fresh samples were stressed at each of the following five charge voltage levels: ± 125 , 250, 500, 1000, & 1500V. For both products Bipolar2 and BiCMOS3, the NSCDM classification was C3 (250V withstand voltage), while for Product CMOS5 the NSCDM classification was C4 (500V withstand voltage).

Failure Mode Characterization

For products Bipolar2, BiCMOS3, and CMOS5, the failure modes for the SCDM and NSCDM classification rejects were determined by reviewing the post-stress ATE data logs and conducting low current (nA range) curve tracer analysis. For products Bipolar2 and BiCMOS3, the failure modes on typical manufacturing-induced CDM rejects were also determined in a similar manner. (No real-world CDM failures have been detected to date on product CMOS5.) The results are listed in Table 1.

Additional SCDM and NSCDM Testing

The most interesting result in Table 1 is the difference in failure modes seen on product BiCMOS3. To determine whether this difference might be related to the relatively large charge voltage steps used in the SCDM and NSCDM classification testing, products Bipolar2 and BiCMOS3 were further tested using 25V steps. SCDM testing was initially conducted on product Bipolar2 samples using conventional dual polarity triple discharging per pin. During this testing, the I-V characteristics at pin 1 were monitored immediately after *each* discharge event using the curve tracing capability of the ESD test system. [Current was limited to $1\mu A$ to ensure any CDM damage was not altered.] While conducting SCDM testing on a fresh (previously unstressed) Bipolar2 sample at $\pm 375V$, an unexpected phenomenon was observed: The first discharge after positive polarity charging resulted in the characteristic resistive short to substrate, while the third such discharge resulted in full recovery of the I-V characteristics. Previous FA experience with CDM manufacturing failures on both products Bipolar2 and BiCMOS3 had shown a related effect: Pin 1 resistive shorts could often be corrected by curve tracing in the low mA range, resulting in fully functional units.

Since multiple discharges on the same sample could thus induce failure and subsequently recover the failure, the test method for SCDM and NSCDM characterization testing was subsequently modified to consist of only *one* discharge applied to pin 1 (the most susceptible pin) *per sample*. Such characterization testing therefore required

Table 2: Single Discharge SCDM & NSCDM Evaluation Results

Product	SCDM First Failure Voltages	SCDM Failure Mode (For both failing samples per product analyzed)	NSCDM First Failure Voltages	NSCDM Failure Mode (For both failing samples per product analyzed)
Bipolar2	-350V & +375V	Pin 1 resistively shorted to Gnd.	+450V & -425V	Pin 1 resistively shorted to Gnd.
BiCMOS3	-425V & -450V	Pin 1 open to Gnd (forward bias).	-550V & -500V	Pin 1 resistively shorted to Gnd.

many samples, but eliminated the possibility of “false passes”. This testing was initiated at $\pm 250V$ and incremented in 25V steps (with the charge voltage polarity alternated for each new sample) until a failure was detected using low current curve tracer analysis immediately after each discharge. After a failure was identified, this procedure was repeated (starting at $\pm 250V$ with 25V steps) until a second failure was detected. Thus, two SCDM and two NSCDM withstand voltages were determined for each product (see Table 2). Throughout this testing, any changes in I-V characteristics were abrupt; most samples exhibited no change in leakage current, while the eight failing samples developed a resistive short or open (see Table 2).

The failure modes identified on Products Bipolar2 and BiCMOS3 using small SCDM and NSCDM charge voltage steps (25V) were the same as those identified during the classification testing using larger steps. Thus, the difference between

SCDM & NSCDM failure modes for product BiCMOS3 is not related to the magnitude of the charge voltage increments during testing.

Root Cause Failure Analysis Results

Full root cause FAs were conducted on the eight samples listed in Table 2; typical manufacturing-induced CDM failures for products Bipolar2 & BiCMOS3; and typical SCDM & NSCDM classification failures for product CMOS5. The FA flow included delidding/decapsulating; high magnification optical die inspection; emission microscopy; bond wire removal (to eliminate the possibility of inadvertent additional ESD damage during subsequent destructive analysis); cross-sectioning/focused ion beam (FIB) analysis; wet chemical delayering; and scanning electron microscope (SEM) inspection as appropriate. Table 3 and Figures 2-9 summarize the results of this analysis.

Table 3: Root Cause FA Results

Product	SCDM Failure Mechanism (All Samples)	NSCDM Failure Mechanism (All Samples)	Manufacturing CDM Failure Mechanism
Bipolar2	Thermal oxide breakdown between pin 1 metal and edge of P+ diffusion into P-substrate (Schematic 1A). Readily visible as delidded (Fig. 2).	Thermal oxide breakdown between pin 1 metal and edge of P+ diffusion into P-substrate (Schematic 1A). Faintly visible as delidded. FIB analysis showed similar damage as on mfg failure.	Thermal oxide breakdown at same site as on SCDM & NSCDM samples. Faintly visible as delidded. FIB analysis showed Al-Si melt filament across ~350nm oxide at pin 1 metal edge (Fig. 3).
BiCMOS3	Electrothermal metal migration above edge of Gnd poly underpass (Schematic 2A). Readily visible as delidded (Fig. 4). FIB analysis showed BPSG & melt filament at breakdown site were vaporized/redeposited (Fig. 5).	BPSG breakdown between Pin 1 metal and edge of Gnd poly underpass (Schematic 2A). Not visible as delidded. Cross-sectional/SEM analysis showed similar damage (Fig. 6) as on manufacturing failure (Fig. 7).	BPSG breakdown between Pin 1 metal and edge of Gnd polysilicon underpass (Schematic 2A). Not visible as delidded. FIB analysis showed Al-Poly melt filament across ~200nm BPSG dielectric at poly corner (Fig. 7).
CMOS5	Gate oxide ruptures at output PMOS drivers (Schematic 3A). Not visible optically. Detected by emission microscopy & verified by SEM analysis (Fig. 8).	Gate oxide ruptures at output PMOS drivers (Schematic 3A). Not visible optically. Detected by emission microscopy & verified by SEM analysis (Fig. 9).	Not Applicable. No such failures detected to date.

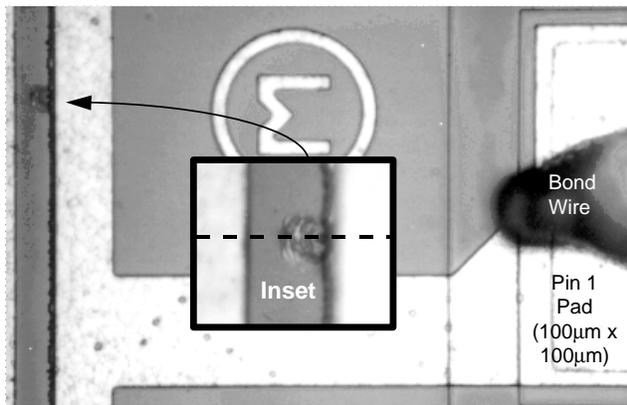


Fig. 2: Optical images (400X & 1000X Inset) of thermal oxide breakdown site on a Bipolar2 sample stressed at -350V SCDM. Damage on the NSCDM & mf'g failures was in the same area, but was subtle.

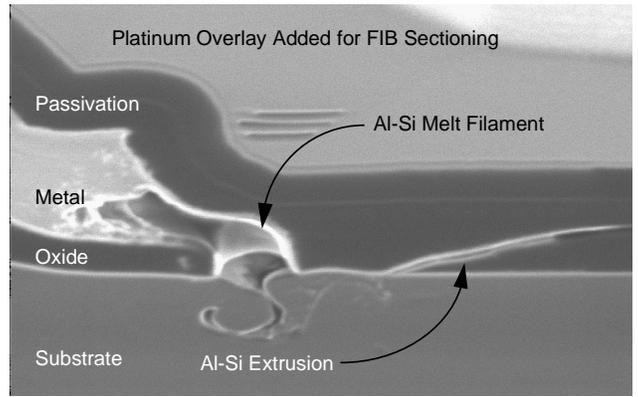


Fig. 3: FIB ion image (8kX) of Al-Si melt filament at breakdown site on a Bipolar2 **manufacturing** failure. FIB section was along plane indicated by dashed line in Fig. 2 (an SCDM sample). Note the Al-Si extrusion.

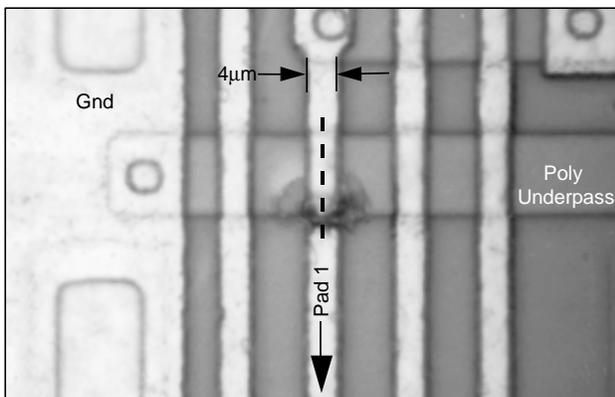


Fig. 4: Optical image (1.0kX) of fused open pin 1 metal and ruptured passivation above the BPSG breakdown site (metal to poly) on a BiCMOS3 sample stressed at -425V SCDM. Note: FIB section shown in Fig. 5 was along plane indicated by dashed line.

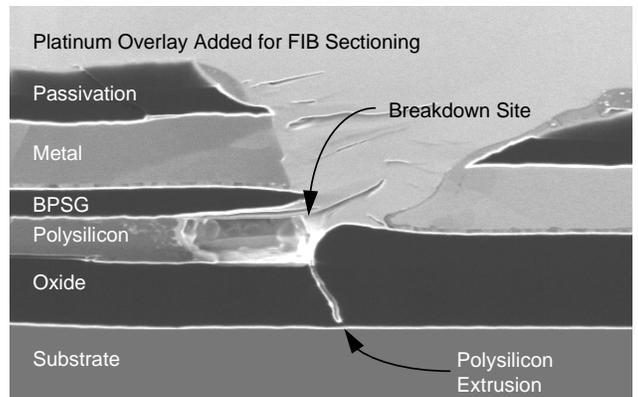


Fig. 5: FIB ion-induced secondary electron image (12kX) of FIB section of SCDM sample shown in Fig. 4. SCDM stressing caused the BPSG & Al-Poly at the initial breakdown site to vaporize/re-deposit. The Pt overlay added later filled-in the void at this site.

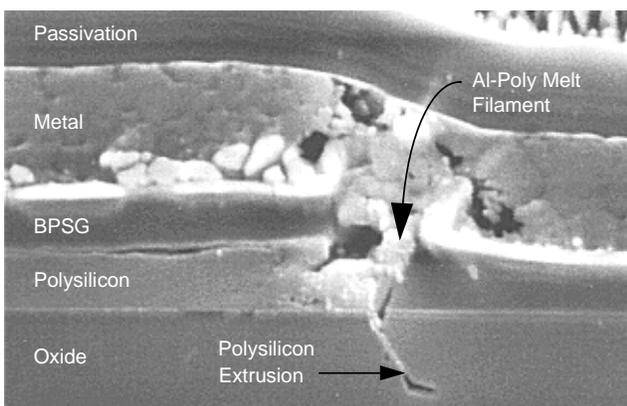


Fig. 6: SEM secondary electron image (21kX) of mechanical cross-section through BPSG breakdown site on a BiCMOS3 sample stressed at -500V NSCDM. Note the polysilicon extrusion.

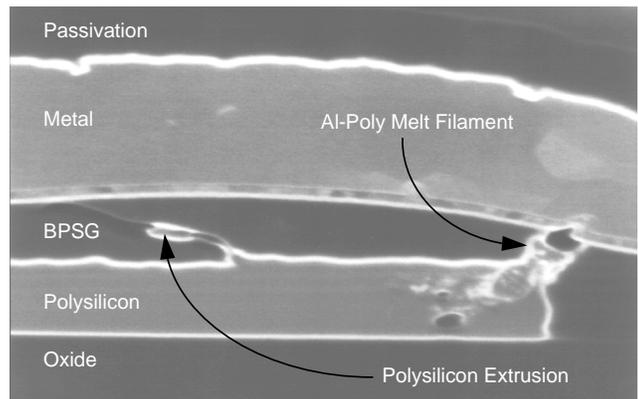


Fig. 7: FIB ion image (24kX) of FIB section through BPSG breakdown site on a BiCMOS3 **manufacturing** failure. Note: Polysilicon extrusion is characteristic of SCDM, NSCDM, & manufacturing failures.

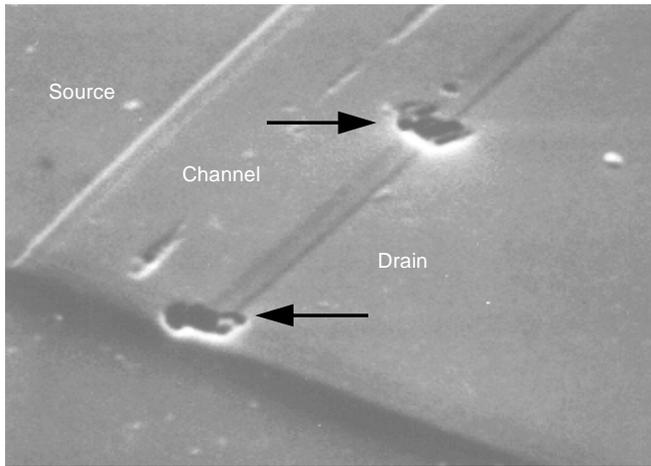


Fig. 8: SEM secondary electron image (20kX) of two gate oxide rupture sites on a CMOS5 sample stressed at $\pm 1500V$ **SCDM**. Notes: (1) The sample was deprocessed to silicon level. (2) Damage sites are typically $0.7-0.8\mu m$ in diameter.

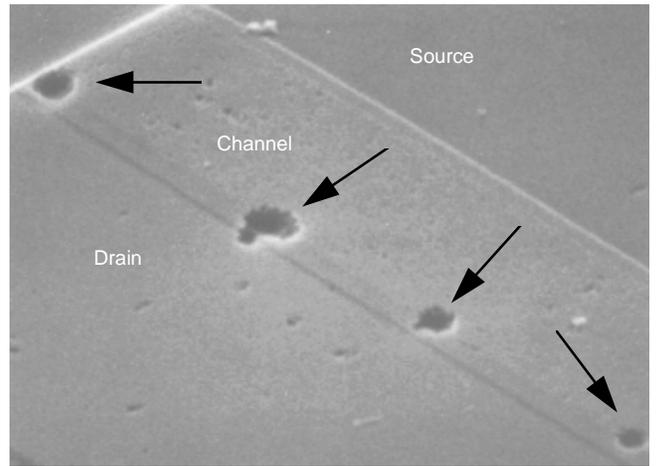


Fig. 9: SEM secondary electron image (20kX) of four gate oxide rupture sites on a CMOS5 sample stressed at $\pm 1500V$ **NSCDM**. Notes: (1) The sample was deprocessed to silicon level. (2) Damage sites are typically $0.2-0.5\mu m$ in diameter.

The preceding FA results on products Bipolar2 & BiCMOS3 demonstrate that NSCDM testing was most effective at simulating the failure modes, failure sites, and failure mechanisms documented on real-world CDM rejects. However, for both these products, SCDM testing identified the same failure sites and initial failure mechanisms (dielectric breakdown) as seen on the manufacturing failures. The primary difference between the SCDM and NSCDM failures on all three focus products was the degree of damage; the damage on the SCDM failures was consistently worse, and in the case of product BiCMOS3, this resulted in a completely different failure mode (an open vs. a resistive short). These differences in damage severity are as expected since an SCDM discharge has a much longer duration and higher energy than an NSCDM discharge for a given charge voltage. This is because the total capacitance that is charged and discharged during SCDM testing includes not only the capacitance between the DUT and the test system ground but also the capacitance associated with all conductors between the floating DUT pins and the test system relay matrix [6,8].

Technical Analysis and CDM Redesigns

1. Product Bipolar2

No explicit ESD protection was initially used at any bond pad on product Bipolar2 (Schematic 1A). Large geometry bipolar transistors and wide, high resistance thin-film resistors were relied on for inherent ESD protection. For all SCDM, NSCDM, and manufacturing samples analyzed, oxide breakdown occurred along the edge of the pin 1 single-level metalization (MET1, Al 1% Cu) where it tapered to a point. These sharp points were due to processing effects associated with the edge of MET1 being coincident with the oxide step above the edge of a P+ diffusion into P- substrate. Along these points, the dielectric thickness was $\sim 350nm$, compared to the much thicker ($\sim 1800nm$) field oxide under the pin 1 MET1 closer to the bond pad. For sufficient charge voltages ($\geq 350V$), this unusual topography resulted in points of highly enhanced electric field ($>> 10^7 V/cm$) that resulted in the following sequence: dielectric breakdown, high current flow/localized heating, and the formation of an Al-Si melt filament resistively shorting the pin 1 MET1 to Gnd/substrate. Interestingly, the localized overheating also caused cracking of the surrounding thermal oxide, providing an

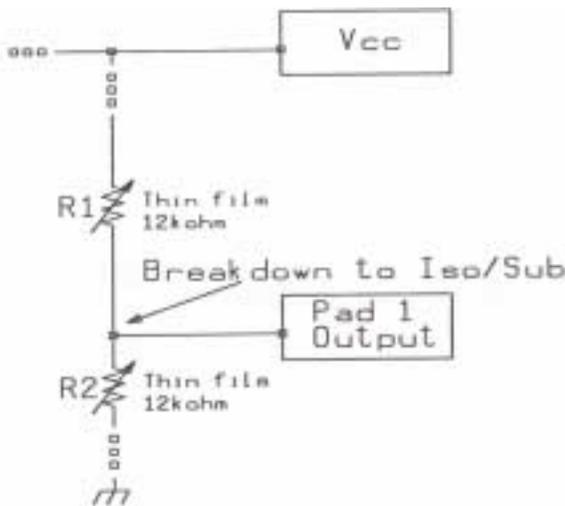
extrusion path for melted Al-Si (see Fig. 3). As discussed earlier, the pin 1 MET1 to Gnd/substrate resistive short could develop and then disappear during multiple discharge CDM testing at a given voltage level, indicating that once formed, the melt filament could be electrothermally fused open by the high current/localized heating associated with a subsequent discharge.

As schematic 1B indicates, the ESD redesign on product Bipolar2 consisted of adding a diode-connected vertical NPN transistor, E1, adjacent to output pad 1 (collector shorted to pad 1, and base shorted to emitter shorted to Gnd/substrate). E1 is a minimum geometry transistor (having a $25\mu\text{m} \times 25\mu\text{m}$ emitter on this >25 year old process) to ensure fast turn-on during a CDM event. E1 has an initial breakdown voltage of BV_{CES} , nominally 70V for this process. Due to the rapid NPN snapback action during an ESD event, the clamp voltage of E1 is typically <20V, ensuring ample protection of all dielectric layers on this product, even at topographically-enhanced high electric field points. This same ESD protection device was added to other I/O pads on product Bipolar 2 on an available-space basis. Due to space constraints, an under-the-pad open-base lateral PNP transistor, E2, was used for protection at the V_{CC} pad. The redesigned version of the Bipolar2 product

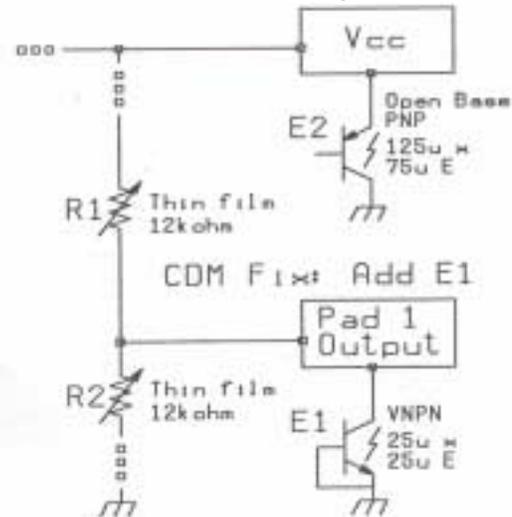
consistently passes 1000V SCDM classification testing. At 1500V SCDM, a capacitor connected to a pad that had no explicit ESD protection (due to space constraints) failed due to oxide breakdown. As with other products with $\geq 1000\text{V}$ SCDM withstand voltages (see Appendices 1-3), no real-world CDM failures have been documented on this redesigned product. The ESD design rules for this mature bipolar process have been revised to require the use of E1 or a similar protection device at all non-substrate pads. Other products using E1 consistently pass >1000V SCDM testing.

2. Product BiCMOS3

As Schematic 2A shows, input pad 1 and the V_{CC} pad on product BiCMOS3 each initially had explicit ESD protection consisting of large lateral NPN transistors, E1 and E2 (collector shorted to the pad, emitter shorted to Gnd, and base resistively shorted to Gnd through the substrate). E1 and E2 each consist of two $105\mu\text{m}$ long N+ diffusions into P-epi/substrate, with a $20\mu\text{m}$ separation (i.e., base width). All other non-substrate pads on this product include this or a similar ESD protection device. E1/E2 have an initial breakdown voltage of BV_{DSS} , with a nominal value of 30V for this process. Although E1/E2 exhibit NPN snapback to <15V during relatively long ESD events, they do not exhibit such snapback during CDM events due



Schematic 1A: Initial Pin 1 Output Circuit on Product Bipolar2



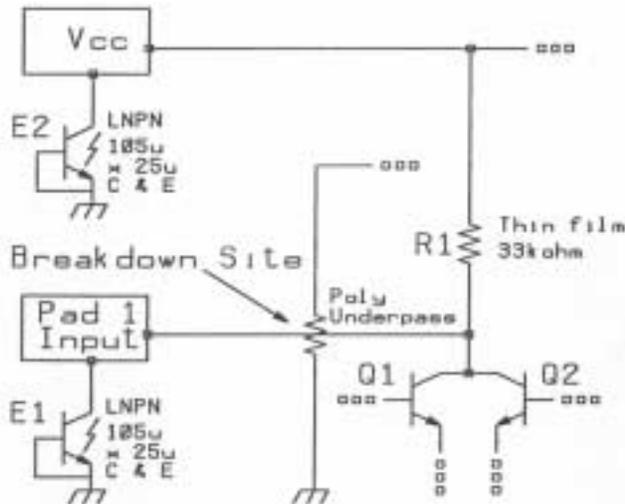
Schematic 1B: Redesigned Pin 1 Output Circuit on Product Bipolar2

to the slow NPN turn-on time associated with the large base width (20µm). Consequently, these protection devices provide adequate HBM protection (typically >3000V), but insufficient stand-alone CDM protection.

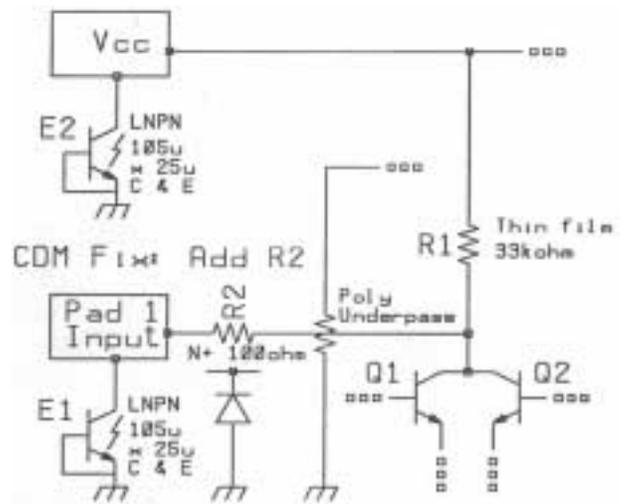
As with product Bipolar2, when pin 1 was discharged after Gnd/substrate charging, dielectric breakdown occurred at a point of topographically-enhanced electric field. For product BiCMOS3, these points were along the edge of the pin 1 MET1 (4µm wide, 1µm thick, Al 1% Cu) where it crossed a Poly underpass to Gnd. The nominal thickness of the borophosphosilica glass (BPSG) dielectric layer between MET1 and Poly is 400nm. However, at points where MET1 orthogonally crosses the edge of Poly, the BPSG can thin to ~200nm. Not surprisingly, FA results on NSCDM and real-world CDM failures showed that the pin 1 MET1 to Poly dielectric breakdown consistently occurred at these maximum electric field points where the field was enhanced by the 90° edge of the Poly (see Fig.'s 5-7), resulting in the subsequent formation of an Al-Poly melt filament resistively shorting pin 1 MET1 to the Gnd underpass. Similar to the Bipolar2 product CDM failures, the localized overheating also caused cracking/buckling of surrounding dielectric layers (BPSG and thermal oxide) providing an extrusion path for melted polysilicon (see Fig.'s

5-7). On the SCDM failures, the high current flow/localized overheating was sufficient to fuse open the pin 1 MET1 due to melting/vaporization (see Fig.'s 4-5). Although this SCDM damage obliterated the initial dielectric breakdown site between MET1 and the corner of the Poly, the location of this voiding along with the presence of a polysilicon extrusion (which is characteristic of NSCDM and manufacturing CDM failures on this product) confirms that the initial SCDM failure mechanism was likewise due to dielectric (BPSG) breakdown.

The CDM redesign on a subsequent generation of product BiCMOS3 consisted of adding a 100Ω N+ diffused series resistor, R2, to the interconnect between pad 1 and the Poly Gnd underpass (Schematic 2B). This same series diffused resistor was also used on other input and output interconnects with known CDM susceptibilities. Due to layout constraints, these interconnects could not be made wider. The combination of the series resistance and the distributed parasitic diode formed by the N+ diffusion into P-epi/substrate acts as an efficient CDM protection device. The resistance slows the rise time and limits the current associated with the CDM discharge, while the distributed diode limits the voltages along the interconnect at well below the dielectric breakdown voltages, even at high field "point sources."



Schematic 2A: Initial Pin 1 Input Circuit on Product BiCMOS3

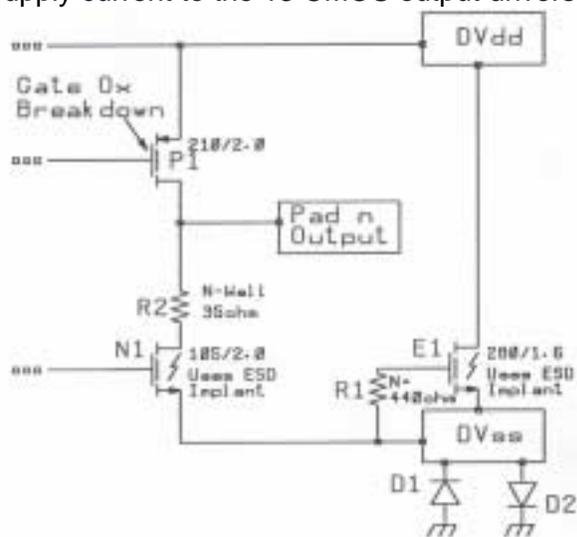


Schematic 2B: Redesigned Pin 1 Input Circuit on Product BiCMOS3

The subsequent generation of the BiCMOS3 product consistently passes 1500V SCDM classification testing (the maximum test capability of the particular system used), and no handling/manufacturing CDM failures have been identified on this product. The ESD design rules for this BiCMOS process have been revised to require the use of either a “ π -network” pad protection device (incorporating a diffused series resistor) or the combination of E1 and R2 off all pads with interconnects crossing polysilicon underpasses.

3. Product CMOS5

For ESD protection, the 13 CMOS output driver pins on Product CMOS5 initially relied on large multi-finger PMOS and NMOS devices to enhance self protection, along with additional output NMOSFET protection provided by an optional ESD implant and a 35 Ω series drain resistance (Schematic 3A). This protection scheme provided adequate HBM protection (>4000V) and SCDM protection (>1500V) to the output NMOSFET. However, after SCDM and NSCDM classification testing using $\pm 250V$ $AV_{SS/substrate}$ charge voltages, the Driver Supply Current, IDV_{DD} , increased dramatically on the SCDM samples *and* moderately on the NSCDM samples (see Figure 10). [On this Analog-to-Digital Converter, the DV_{DD} and DV_{SS} pins only supply current to the 13 CMOS output drivers.



Schematic 3A: Initial Output Driver Circuit on Product CMOS5

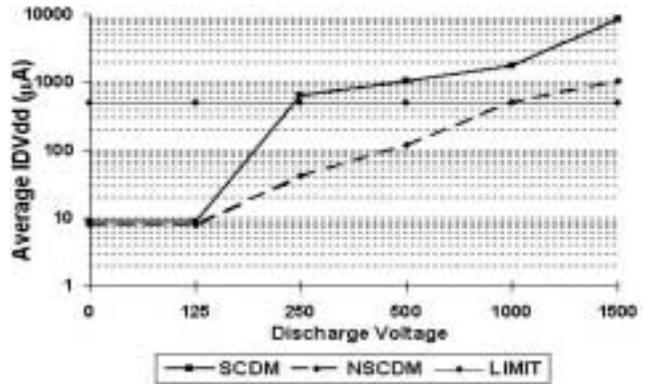
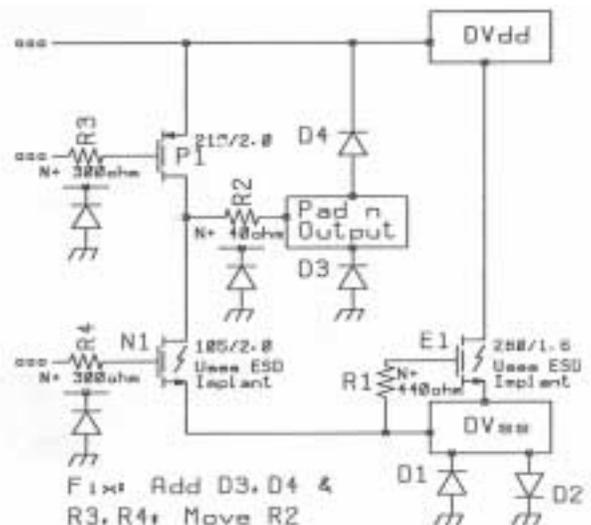


Fig. 10: Product CMOS5 Average Driver Supply Current, IDV_{DD} , at 5.0V, as a function of CDM discharge voltage levels.

IDV_{DD} is essentially just the sum of the output leakage currents for these 13 drivers.] Due to this difference in the rate of IDV_{DD} increases, the SCDM samples first failed the 500 μA maximum specification for this parameter (at $DV_{DD}=5.0V$) following $\pm 250V$ stressing, while the NSCDM samples did not fail until at least $\pm 1000V$. Of particular significance was that increased leakage current could not be detected via conventional non-powered curve tracer testing at the output pins. (Since the outputs could not be tri-stated, powered curve tracer testing was not an appropriate option.) This demonstrates that conducting full parametric and functional testing (not simply curve tracer testing) is particularly important when evaluating the CDM robustness of ICs.



Schematic 3B: Redesigned Output Driver Circuit on Product CMOS5

On representative SCDM and NSCDM failures, emission microscopy revealed emission sites along the Poly1 gates for the PMOS drivers. After concurrent deprocessing of the SCDM and NSCDM samples to the silicon level using 49% HF, SEM inspection revealed pits along the PMOS driver channel-drain interfaces where the edges of the PMOS driver gates overlapped the drain diffusions. Most PMOS driver fingers on the $\pm 1500\text{V}$ SCDM failures exhibited several damage sites each typically $0.7\text{-}0.8\mu\text{m}$ in diameter (Fig. 8), with each site contributing on average $50\mu\text{A}$ of leakage current, while such fingers on the $\pm 1500\text{V}$ NSCDM failures exhibited 2-3 times more damage sites but each site was typically $0.2\text{-}0.5\mu\text{m}$ in diameter (Fig. 9) and contributed on average only $\sim 2\mu\text{A}$ of leakage current. Based on these characteristics, it was concluded that the melt filaments at the gate oxide rupture sites on the SCDM failures were primarily polysilicon, whereas the melt filaments on the NSCDM failures were primarily amorphous silicon, the latter of which have been classified as “latent gate oxide defects” in previous studies [12-14]. Since amorphous silicon has a resistivity several orders of magnitude higher than polysilicon, this explains why the IDV_{DD} on the NSCDM samples is much lower than that for the SCDM failures above the damage threshold ($>125\text{V}$), despite the higher number of NSCDM rupture sites per sample.

Finally, since NSCDM testing provides better replication of real-world CDM failures than SCDM testing, the absence of any such failures to date on product CMOS5 is consistent with the higher withstand voltage determined by NSCDM testing. It is also explained by the division of SCDM and NSCDM leakage currents over 13 different PMOS drivers; real-world CDM damage on this product would typically occur at a corner pin, and only one digital output driver pin on product CMOS5 is a corner pin (i.e., pin 14). Nonetheless, due to the possibility of a latent CDM gate oxide defect eventually becoming a “hard” failure, an ESD redesign was undertaken.

As Schematic 3B shows, for each output driver on product CMOS3, the ESD redesign consisted of adding diodes D3 & D4 to each supply rail at

each output pad; moving R2 so that it is in series with both the driver PMOS, P1, and driver NMOS, N1, drains; and adding series resistors R3 & R4 to the gates of P1 and N1, respectively. R2 is an N+ diffused resistor having relatively low resistance (40Ω) to minimize its impact on the drive capability and switching speed of the outputs. R3 & R4 are also N+ diffused resistors, but are each 300Ω since more resistance can be tolerated on the high impedance gate nodes. The purpose of R2, R3, & R4 is to “steer” CDM discharge currents away from the P1 and N1 gate oxide layers and act as distributed parasitic diode protection devices, similar to R2 on product BiCMOS3. [Note that when R2 was initially in series with the N1 drain only, it prevented CDM damage to the N1 gate oxide.] Most of the high current associated with CDM testing of the output pins is designed to flow through the large, low resistance D3/D4 diodes that were not present in the original design. The redesigned version of product CMOS5 has not been CDM tested yet, but the output drivers are expected to pass $>1000\text{V}$ SCDM testing.

Summary/Conclusions

Contact mode Socketed Charged Device Model (“SCDM”) ESD test results provide a strong indicator of susceptibility to CDM failures during manufacturing operations. In this analysis of 30 products covering a wide range of fabrication and packaging technologies, none of the products with $\geq 500\text{V}$ SCDM robustness per ESD Association Draft Standard DS5.3 have had any documented instances of handling/manufacturing-induced CDM failures. However, this study demonstrated that SCDM testing does not always replicate the electrical failure **mode** observed on real-world CDM failures, though in all cases the failure **site** and the initial failure **mechanism** were the same. In the absence of FA results on NSCDM samples, discrepancies in failure modes could lead to real-world failures being erroneously attributed to problems other than ESD, possibly leading to inappropriate/ineffective redesigns. With the knowledge gained from full root cause FAs on NSCDM

samples, the CDM redesigns on three products with relatively low CDM robustness were relatively straightforward, involving the addition of voltage clamping and/or current limiting devices at the susceptible pins. These redesigns have been effective on two of the three products evaluated to date.

For semiconductor and electronics companies requiring ongoing CDM classification/characterization of many new IC products, this study has shown that a combined SCDM and NSCDM test approach is effective for predicting CDM fallout and driving CDM improvements:

1. Due to advantages such as high throughput and *in-situ* electrical test capability, use SCDM classification testing on *all* new products to identify which ones may be susceptible to handling/manufacturing failures. [If *in-situ* electrical test capability is limited to standard curve tracing and/or DC measurements, such testing should be augmented by full parametric and functional testing to detect internal circuit damage or subtle leakages that could lead to latent failures.] This study indicated products with <500V SCDM withstand voltages are particularly susceptible to real-world failures, warranting further analysis. However, a higher withstand voltage limit may be appropriate for prompting further analysis, depending on such factors as the parasitics associated with the SCDM test system/DUT boards used, the level of control over electrostatic charging during manufacturing, and CDM robustness improvement goals.
2. For products with <500V SCDM robustness (or an appropriately higher limit), augment SCDM testing with NSCDM testing to best replicate any real-world failures. When such products are available in multiple packages, NSCDM testing should be conducted on samples in all package options to identify withstand voltage dependencies on package parasitics. (Although not investigated here, earlier studies have shown NSCDM testing is

far superior to SCDM testing in detecting such package dependencies [8,17].)

3. Using detailed failure analysis results on NSCDM and/or real-world failures, revise CDM design rules and verify their effectiveness on redesigns/new products.

Final guidelines for CDM testing and CDM robustness improvement programs include:

1. Take precautions to ensure multiple discharges at a given pin (e.g., triple positive polarity and triple negative polarity) are not potentially inducing a dielectric breakdown failure and subsequently masking it. Such occurrences can usually be detected during SCDM testing by monitoring the low-current I-V characteristics after *each* discharge event. (Low current curve tracing or other low current post-stress electrical testing should be used to ensure such testing is likewise not resulting in recovery of CDM breakdowns.) If appropriate, conduct CDM evaluation testing using a single polarity single discharge per pin.
2. Products that can be damaged by a relatively low magnitude single discharge at a *corner* pin should be prime candidates for redesigns. Such products are particularly susceptible to handling/manufacturing failures, as evidenced by the history of CDM fallout on the initial versions of products Bipolar2 and BiCMOS3. When flexibility exists in defining any no connect pins on a product, select corner pins whenever possible.
3. For optimal detection of CDM damage thresholds (at and above which latency may be an issue [12-16]), examine CDM-induced *shifts* in key parameters (I_{SUPPLY} , I_{IH} , I_{IL} , etc.), rather than relying simply on pass/fail electrical test results per data sheet limits.

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References

- [1] "EOS/ESD-DS5.3-1993," ESD Association Draft Standard for Electrostatic Discharge (ESD) Sensitivity Testing - Charged Device Model (CDM) Component Testing, October 10, 1993.
- [2] M. Chaine, C.T. Liong, and H.F. San, "A Correlation Study Between Different Types of CDM Testers and 'Real' Manufacturing In-Line Leakage Failures," EOS/ESD Symposium Proceedings, 1994, pp. 63-68.
- [3] R.S. Deol, P. Philips, and M. Spencer, "CDM Failure in Microelectronics," EOS/ESD Technology, Autumn 1993 Edition, pp. 6-11.
- [4] R. Renninger, M.C. Jon, D. Lin, T. Diep, and T. Welsher, "A Field Induced Charged-Device Model Simulator," EOS/ESD Symposium Proceedings, 1989, pp. 59-71.
- [5] T. Maloney, "Designing MOS Inputs and Outputs to Avoid Oxide Failure in the Charged Device Model," EOS/ESD Symposium Proceedings, 1988, pp. 220-227.
- [6] H. Gieser, P. Egger, "Influence of Tester Parasitics on 'Charged Device Model' - Failure Thresholds," EOS/ESD Symposium Proceedings, 1994, pp. 69-84.
- [7] J.T. May, C. Robinson, M. Biegel, L. Tyler, "Charged Device Damage of PLCCs Inside an Antistatic Shipping Tube--A Case History," EOS/ESD Symposium Proceedings, 1994, pp. 85-89.
- [8] K. Verhaege, G. Groeseneken, H. Maes, P. Egger, H. Gieser, "Influence of Tester, Test Method, and Device Type on CDM ESD Testing," EOS/ESD Symposium Proceedings, 1994, pp. 49-62.
- [9] P. Bossard, R. Chemelli, and B. Unger, "ESD Damage from Triboelectrically Charged IC Pins," EOS/ESD Symposium Proceedings, 1980, pp. 17-22.
- [10] T. Maloney, "Integrated Circuit Metal in the Charged Device Model: Bootstrap Heating, Melt Damage, and Scaling Laws," EOS/ESD Symposium Proceedings, 1992, pp. 129-134.
- [11] R. Renninger, "Mechanisms of Charged-Device Electrostatic Discharges," EOS/ESD Symposium Proceedings, 1991, pp. 127-143.
- [12] J. Reiner, "Latent Gate Oxide Defects Caused by CDM-ESD," EOS/ESD Symposium Proceedings, 1995, pp. 311-321.
- [13] J. Reiner, "A Physical Model for the Creation of Latent Gate Oxide Defects by Very Fast Electrostatic Discharges," Proceedings of the ESREF, 1994, p. 467.
- [14] J. Colvin, "The Identification and Analysis of Latent ESD Damage in CMOS Input Gates," EOS/ESD Symposium Proceedings, 1993, pp. 109-116.
- [15] M. Song, D. Eng, K. MacWilliams, "Quantifying ESD/EOS Latent Damage and Integrated Circuit Leakage Currents," EOS/ESD Symposium Proceedings, 1995, pp. 304-310.
- [16] W. Tan, "Minimizing ESD Hazards in IC Test Handlers and Automatic Trim/Form Machines," EOS/ESD Symposium Proceedings, 1993, pp. 109-116.
- [17] L. Avery, "Charged Device Model Testing; Trying to Duplicate Reality," EOS/ESD Symposium Proceedings, 1987, pp. 88-92.
- [18] N. Clark, K. Parat, T. Maloney, Y. Kim, "Melt Filaments in n+pn+ Lateral Bipolar ESD Protection Devices," EOS/ESD Symposium Proceedings, 1995, pp. 295-303.
- [19] N. Maene, J. Vandenbroeck, L. Van den Bempt, "Failure Analysis of CDM Failures in a Mixed Analog/Digital Circuit," EOS/ESD Symposium Proceedings, 1994, pp. 307-314.
- [20] C. Duvvury, A. Amerasekera, "Advanced CMOS Protection Device Trigger Mechanisms During CDM," EOS/ESD Symposium Proceedings, 1995, pp. 162-174.

Appendix 1: SCDM Classification Results on Ten Bipolar Products

Product	Family	Fabrication Process	Package	SCDM Withstand Voltage	Actual CDM Failure Rate
Bipolar1	RMS-to-DC Converter	625 μm^2 emitter junction-isolated bipolar with thin-film resistors	10-lead 350 mil diameter metal can (TO-100)	1500V (C6)	~0
Bipolar2	Voltage Reference	625 μm^2 emitter junction-isolated bipolar with thin-film resistors	14-lead 300 mil side brazed ceramic DIP (D-14)	250V (C3)	High
Bipolar3	Operational Amplifier	400 μm^2 emitter junction-isolated bipolar with thin-film resistors	8-lead 300 mil plastic DIP (N-8)	1000V (C5)	~0
Bipolar4	Line Driver	121 μm^2 emitter junction-isolated complementary bipolar with thin-film resistors	15-lead 420 mil plastic SIP with heat slug (Y-15)	1500V (C6)	~0
Bipolar5	Operational Amplifier	121 μm^2 emitter junction-isolated complementary bipolar with thin-film resistors	16-lead 300 mil plastic SOIC (R-16)	1500V (C6)	~0
Bipolar6	Voltage Reference	120 μm^2 emitter junction-isolated bipolar with thin-film resistors	14-lead 300 mil side brazed ceramic DIP (D-14)	500V (C4)	~0
Bipolar7	Voltage Reference	56 μm^2 emitter junction-isolated bipolar with thin-film resistors	3-lead 50 mil plastic surface mount (SOT-23)	1500V (C6)	~0
Bipolar8	Operational Amplifier	2.25 μm^2 emitter dielectrically-isolated with thin-film resistors	8-lead 150 mil plastic SOIC (SO-8)	1500V (C6)	~0
Bipolar9	Sensor	2.25 μm^2 emitter dielectrically-isolated with thin-film resistors	8-lead 150 mil plastic SOIC (SO-8)	1500V (C6)	~0
Bipolar10	ASIC	2.25 μm^2 emitter dielectrically-isolated with thin-film resistors	16-lead 450 mil side brazed ceramic gull wing (GW-16)	1000V (C5)	~0

Appendix 2: SCDM Classification Results on Ten BiCMOS Products

Product	Family	Fabrication Process	Package	SCDM Withstand Voltage	Actual CDM Failure Rate
BiCMOS1	Analog-to-Digital Converter	169 μm^2 emitter & 4 μm CMOS junction-isolated BiCMOS with thin-film resistors	28-lead 600 mil side brazed ceramic DIP (D-28)	1000V (C5)	~0
BiCMOS2	ASIC	169 μm^2 emitter & 4 μm CMOS junction-isolated BiCMOS with thin-film resistors	28-lead 300 mil plastic SOIC (R-28)	500V (C4)	~0
BiCMOS3	Operational Amplifier	169 μm^2 emitter & 4 μm CMOS junction-isolated BiCMOS with thin-film resistors	8-lead 300 mil ceramic DIP (Q-8)	250V (C3)	Moderate
BiCMOS4	Operational Amplifier	36 μm^2 emitter & 2 μm CMOS junction-isolated BiCMOS with thin-film resistors	8-lead 300 mil plastic DIP (N-8)	1500V (C6)	~0
BiCMOS5	Voltage Reference	36 μm^2 emitter & 2 μm CMOS junction-isolated BiCMOS with thin-film resistors	8-lead 150 mil plastic SOIC (SO-8)	1500V (C6)	~0

Appendix 2: SCDM Classification Results on Ten BiCMOS Products - Continued

Product	Family	Fabrication Process	Package	SCDM Withstand Voltage	Actual CDM Failure Rate
BiCMOS6	Digital-to-Analog Converter	4 μm^2 emitter & 2 μm CMOS junction-isolated BiCMOS with thin-film resistors	16-lead 300 mil plastic SOIC (R-16)	1000V (C5)	~0
BiCMOS7	Digital-to-Analog Converter	4 μm^2 emitter & 2 μm CMOS junction-isolated BiCMOS with thin-film resistors	28-lead 300 mil plastic SOIC (R-28)	1000V (C5)	~0
BiCMOS8	Analog-to-Digital Converter	4 μm^2 emitter & 2 μm CMOS junction-isolated BiCMOS with thin-film resistors	44-lead 350 mil ceramic leadless chip carrier (E-44)	500V (C4)	~0
BiCMOS9	Analog-to-Digital Converter	4 μm^2 emitter & 2 μm CMOS junction-isolated BiCMOS with thin-film resistors	28-lead 600 mil side brazed ceramic DIP (D-28)	1500V (C6)	~0
BiCMOS 10	Analog-to-Digital Converter	1 μm^2 emitter & 1 μm CMOS junction-isolated BiCMOS	28-lead 210 mil plastic shrink SOIC (SSOP-28)	1000V (C3)	~0

Appendix 3: SCDM Classification Results on Ten CMOS Products

Product	Family	Fabrication Process	Package	SCDM Withstand Voltage	Actual CDM Failure Rate
CMOS1	Analog-to-Digital Converter	2.0 μm junction-isolated double polysilicon double metal CMOS	28-lead 600 mil side brazed ceramic DIP (D-28)	1000V (C5)	~0
CMOS2	Sample Rate Converter	0.8 μm junction-isolated single polysilicon double metal CMOS	28-lead 600 mil plastic DIP (N-28)	1500V (C6)	~0
CMOS3	Video Encoder	0.8 μm junction-isolated double polysilicon double metal CMOS	16-lead 300 mil plastic SOIC (R-16)	500V (C4)	~0
CMOS4	Analog-to-Digital Converter	0.8 μm junction-isolated double polysilicon double metal CMOS	28-lead 300 mil plastic SOIC (R-28)	500V (C3)	~0
CMOS5	Analog-to-Digital Converter	0.8 μm junction-isolated double polysilicon double metal CMOS	28-lead 300 mil plastic SOIC (R-28)	125V (C2)	~0
CMOS6	ASIC	0.6 μm junction-isolated double polysilicon double metal CMOS	160-lead 1100 mil plastic quad flatpack (PQFP-160)	500V (C4)	~0
CMOS7	Digital-to-Analog Converter	0.6 μm junction-isolated double polysilicon double metal CMOS	28-lead 210 mil plastic shrink SOIC (SSOP-28)	1000V (C5)	~0
CMOS8	Digital-to-Analog Converter	0.6 μm junction-isolated double polysilicon double metal CMOS	24-lead 600 mil plastic SOIC (SSOP-28)	1000V (C5)	~0
CMOS9	DSP Micro-computer	0.6 μm junction-isolated single polysilicon double metal CMOS	68-lead 950 mil plastic quad flatpack (PQFP-68)	500V (C5)	~0
CMOS10	DSP Signal Processor	0.5 μm junction-isolated single polysilicon double metal CMOS	100-lead 550 mil plastic thin quad flatpack (TQFP-100)	1000V (C6)	~0