Product/Process Change Notice - PCN 16_0159 Rev. -

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This notice is to inform you of a change that will be made to certain ADI products (see Appendix A) that you may have purchased in the last 2 years. **Any inquiries or requests with this PCN (additional data or samples) must be sent to ADI within 30 days of publication date.** ADI contact information is listed below.

PCN Title: AD9144 Die Revision and Data Sheet Update

Publication Date: 31-Aug-2016

Effectivity Date: 29-Nov-2016 *(the earliest date that a customer could expect to receive changed material)*

Revision Description:

Initial Release

Description Of Change

Die Revision Changes:
- Rewire charge pump circuitry to increase the initial charge pump voltage.
- Update JESD204B SERDES interface blocks to increase the maximum operating lane rate supported.

Data Sheet Update:
- The new JESD204B SERDES maximum operating lane rates have increased from 10.64Gbps to 12.4Gbps due to die circuitry enhancements made to the JESD204B SERDES interface blocks.

Reason For Change

Die Revision Changes:
- The change addresses an issue where at cold temperatures, the on-chip phase-locked loops (PLLs) for either the SERDES or DAC clock PLLs may not lock from startup due to a low initial charge pump voltage.
- A new JESD204B SERDES design was implemented to allow customers to operate at higher lane rates than was previously supported.

Data Sheet Update:
- The new SERDES maximum operating lane rate specification allows for higher data throughput capabilities than was previously supported.

Impact of the change (positive or negative) on fit, form, function & reliability

There is no change to the fit, form and reliability of the devices.
The functionality is improved with the revision when attempting to lock the SERDES and/or DAC PLLs at cold temperatures. The SERDES or DAC clock PLL will always lock at cold temperatures.
The functionality of the JESD204B interface is unchanged, however the maximum speed capability is improved from 10.64Gbps to 12.4Gbps.

Product Identification *(this section will describe how to identify the changed material)*

The Revision ID Register Address 0x06 default value changes from 0x06 to 0x08 for silicon revision traceability.
Changes will be reflected in the Rev. B of the AD9144 data sheet.

Summary of Supporting Information

Qualification has been performed per Industry Standard Test Methods. See attached Qualification Results Summary.

Supporting Documents

Attachment 1: Type: Qualification Results Summary

ADI_PCN_16_0159_Rev_-_AD9144_QualificationResultsSummary.pdf

For questions on this PCN, please send an email to the regional contacts below or contact your local ADI sales representatives.					
Americas:	PCN_Americas@analog.com	**Europe:**	PCN_Europe@analog.com	**Japan:**	PCN_Japan@analog.com
				Rest of Asia:	PCN_ROA@analog.com

Appendix A - Affected ADI Models				
Added Parts On This Revision - Product Family / Model Number (4)				
AD9144 / AD9144BCPAZ	AD9144 / AD9144BCPAZRL	AD9144 / AD9144BCPZ	AD9144 / AD9144BCPZRL	

Appendix B - Revision History			
Rev	**Publish Date**	**Effectivity Date**	**Rev Description**
Rev. -	31-Aug-2016	29-Nov-2016	Initial Release