# 4-Channel PMBus Power System Manager Featuring Accurate Output Current Measurement

## FEATURES

- **Sequence, Trim, Margin and Supervise Four Power Supplies**
- **Manage Faults, Monitor Telemetry and Create Fault Logs**
- **PMBus Compliant Command Set**
- **Supported by LTpowerPlay® GUI**
- **Margin or Trim Supplies to within 0.25% of Target**
- **Fast OV/UV Supervisors Per Channel**
- **Fast Output Current Supervisors Per Channel**
- **Coordinate Sequencing and Fault Management Across Multiple LTC PSM Devices**
- **Automatic Fault Logging to Internal EEPROM**
- **Operate Autonomously without Additional Software**
- External Temperature and Input Voltage Supervisors
- Accurate Monitoring of Four Output Voltages, Four Output Currents, Four External Temperatures, Input Voltage and Internal Die Temperature
- $I^2C$/SMBus Serial Interface
- Can Be Powered from 3.3V, or 4.5V to 15V
- Available in 64-Lead 9mm × 9mm QFN Package

## APPLICATIONS

- Computers and Network Servers
- Industrial Test and Measurement
- High Reliability Systems
- Medical Imaging
- Video

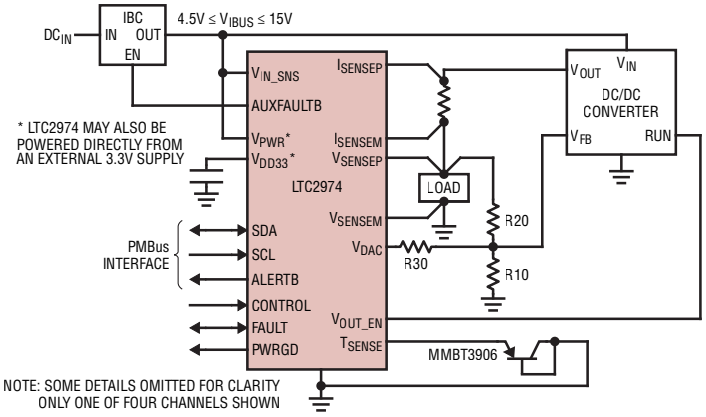
## DESCRIPTION

The LTC®2974 is a 4-channel Power System Manager used to sequence, trim (servo), margin, supervise, manage faults, provide telemetry and create fault logs. PMBus commands support power supply sequencing, precision point-of-load voltage adjustment and margining. DACs use a proprietary soft-connect algorithm to minimize supply disturbances. Supervisory functions include over and under current, voltage and temperature threshold limits for four power supply output channels as well as over and under voltage threshold limits for a single power supply input channel. Programmable fault responses can disable the power supplies with optional retry after a fault is detected. Faults that disable a power supply can automatically trigger black box EEPROM storage of fault status and associated telemetry. An internal 16-bit ADC monitors four output voltages, four output currents, four external temperatures, one input voltage and die temperature. Output power is also calculated. A programmable watchdog timer monitors microprocessor activity for a stalled condition and resets the microprocessor if necessary. A single wire bus synchronizes power supplies across multiple LTC Power System Management (PSM) devices. Configuration EEPROM with ECC supports autonomous operation without additional software.

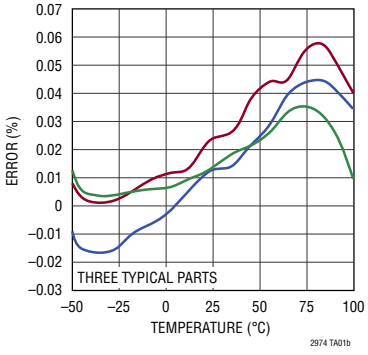


## TYPICAL APPLICATION

**4-Channel PMBus Power System Manager**




**ADC Total Unadjusted Error vs Temperature**



## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_J$ = 25°C. $V_{PWR}$ = $V_{IN\_SNS}$ = 12V, $V_{DD33}$, $V_{DD25}$, REFP and REFM pins fl unless otherwise indicated. $C_{VDD33}$ = 100nF, $C_{VDD25}$ = 100nF and $C_{REF}$ = 100nF. (Note 2)**

was just +

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **Sense Input Current Characteristics (Note 11)** | | | | | | | |
| $I_{IN\_VSENSE}$ | Input Current | $V_{SENSEPn}$ and $V_{SENSEMn}$ Inputs | ● | | | ±15 | µA |
| | Differential Input Current | $V_{SENSEPn}$ and $V_{SENSEMn}$ Inputs, $V_{IN\_DIFF}$ = 6V | ● | | | ±30 | µA |
| $I_{IN\_ISENSE}$ | Input Current | $V_{SENSEPn}$ and $V_{SENSEMn}$ Inputs | ● | | | ±3 | µA |
| | Differential Input Current | $V_{SENSEPn}$ and $V_{SENSEMn}$ Inputs, $\|V_{IN\_DIFF}\|$ = 170mV | ● | | +/- 0.5 | ±5 | µA |
| **DAC Output Ch s** | | | | | | | |
| $N\_V_{DAC}$ | Resolution | | | | 10 | | |
| $V_{FS\_VDAC}$ | Full-Scale Output Voltage (Programmable) | DAC Code = 0x3FF, DAC Polarity = 1, Buffer Gain Setting_0 | ● | 1.3 | 1.38 | 1.44 | V |
| | | DAC Code = 0x3FF, DAC Polarity = 1, Buffer Gain Setting_1 | ● | 2.5 | 2.65 | 2.77 | V |
| $INL\_V_{DAC}$ | Integral Nonlinearity | (Note 7) | ● | | | ±2 | LSB |
| $DNL\_V_{DAC}$ | Differential Nonlinearity | (Note 7) | ● | | | ±2.4 | LSB |
| $V_{OS\_VDAC}$ | Offset Voltage | (Note 7) | ● | | | ±12 | mV |
| $V_{DAC}$ | Load Regulation | $V_{DACn}$ = 2.65V, $I_{VDACn}$ Sourcing = 2mA | | | 100 | | ppm/mA |
| | | $V_{DACn}$ = 0.1V, $I_{VDACn}$ Sinking = 2mA | | | 100 | | ppm/mA |
| | PSRR | DC: 3.13V ≤ $V_{DD33}$ ≤ 3.47V, $V_{PWR}$ = $V_{DD33}$ | | | 60 | | dB |
| | Leakage Current | $V_{DACn}$ Hi-Z, 0V ≤ $V_{DACn}$ ≤ 6V | ● | | | ±100 | nA |
| | Short-Circuit Current Low | $V_{DACn}$ Shorted to GND | ● | –12 | | –4 | mA |
| | Short-Circuit Current High | $V_{DACn}$ Shorted to $V_{DD33}$ | ● | 4 | | 12 | mA |
| $C_{OUT}$ | Output Capacitance | $V_{DACn}$ Hi-Z | | | 10 | | pF |
| $t_{S\_VDAC}$ | DAC Output Update Rate | Fast Servo Mode | | | 250 500 | | µs |
| **Voltage Supervisor Characteristics** | | | | | | | |
| $V_{IN\_VS}$ | Input Voltage Range (Programmable) | $V_{IN\_VS}$ = ($V_{SENSEPn}$ – $V_{SENSEMn}$), Low Resolution Mode | ● | 0 | | | |
| | | $V_{IN\_VS}$ = ($V_{SENSEPn}$ – $V_{SENSEMn}$), High Resolution Mode | ● | 0 | | 3.8 | V |
| | | Single-Ended Voltage: $V_{SENSEMn}$ | ● | –0.1 | | 0.1 | V |
| $N\_VS$ | Voltage Sensing Resolution | 0V to 3.8V Range: High Resolution Mode | | | 4 | | mV/LSB |
| | | 0V to 6V Range: Low Resolution Mode | | | 8 | | mV/LSB |
| $TUE\_VS$ | Total Unadjusted Error | 2V ≤ $V_{IN\_VS}$ ≤ 6V, Low Resolution Mode | ● | | | ±1.25 | % of Reading |
| | | 1.5V < $V_{IN\_VS}$ ≤ 3.8V, High Resolution Mode | ● | | | ±1.0 | % of Reading |
| | | 0.8V ≤ $V_{IN\_VS}$ ≤ 1.5V, High Resolution Mode | ● | | | ±1.5 | % of Reading |
| $t_{S\_VS}$ | Update Period | | | | 12.21 | | µs |
| **Current Supervisor Characteristics** | | | | | | | |
| $V_{IN\_CS}$ | Current Sense Input Range | Single-Ended Voltage: $I_{SENSEPn}$, $I_{SENSEMn}$ | ● | –0.1 | | 6 | V |
| | | Differential Voltage: $V_{IN\_CS}$ = ($I_{SENSEPn}$ – $I_{SENSEMn}$) | ● | –170 | | 170 | mV |
| $N\_CS$ | Current Sense Resolution | IOUT_OC_FAULT_LIMIT • IOUT_CAL_GAIN<br>IOUT_UC_FAULT_LIMIT • IOUT_CAL_GAIN | | | 400 | | µV/LSB |
| $TUE\_CS$ | Total Unadjusted Error | 50mV ≤ $\|V_{IN\_CS}\|$ ≤ 170mV | ● | | | ±3 | % of Reading |
| | | $\|V_{IN\_CS}\|$ < 50mV | ● | | | ±1.5 | mV |
| $V_{OS\_CS}$ | Offset Error | $V_{IN\_CS}$ = 0.8mV | ● | | | ±600 | µV |
| $t_{S\_CS}$ | Update Period | | | | 12.21 | | µs |

Add

Increased Limit was +/- 0.5

Increased from 250

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_J$ = 25°C. $V_{PWR}$ = $V_{IN\_SNS}$ = 12V, $V_{DD33}$, $V_{DD25}$, REFP and REFM pins floating, unless otherwise indicated. $C_{VDD33}$ = 100nF, $C_{VDD25}$ = 100nF and $C_{REF}$ = 100nF. (Note 2)**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **$V_{IN\_SNS}$ Input Characteristics** | | | | | | | |
| $V_{IN\_SNS}$ | $V_{IN\_SNS}$ Input Voltage Range | | ● | 0 | | 15 | V |
| $R_{VIN\_SNS}$ | $V_{IN\_SNS}$ Input Resistance | | ● | 70 | 90 | 110 | kΩ |
| $TUE_{VIN\_SNS}$ | VIN_ON, VIN_OFF Threshold Total Unadjusted Error | 3V ≤ $V_{IN\_SNS}$ ≤ 8V | ● | | | ±2.0 | % of Reading |
| | | $V_{IN\_SNS}$ > 8V | ● | | | ±1.0 | % of Reading |
| | READ_VIN Total Unadjusted Error | 3V ≤ $V_{IN\_SNS}$ ≤ 8V | ● | | | ±1.5 | % of Reading |
| | | $V_{IN\_SNS}$ > 8V | ● | | | ±1.0 | % of Reading |
| **DAC Soft-Connect Comparator Characteristics** | | | | | | | |
| $V_{OS\_CMP}$ | Offset Voltage | $V_{DACP}$*n* = 0.2V | ● | | ±1 | ±18 | mV |
| | | $V_{DACP}$*n* = 1.3V | ● | | ±2 | ±26 | mV |
| | | $V_{DACP}$*n* = 2.65V | ● | | ±3 | ±52 | mV |
| **External Temperature Sensor Characteristics (READ_TEMPERATURE_1)** | | | | | | | |
| $t_{CONV\_TSENSE}$ | Conversion Time | For One Channel, (Total Latency For All Channels Is 4 • 66ms) | | | 66 | | ms |
| $I_{TSENSE\_HI}$ | $T_{SENSE}$ High Level Current | | ● | –90 | –64 | –40 | µA |
| $I_{TSENSE\_LOW}$ | $T_{SENSE}$ Low Level Current | | ● | –5.5 | –4 | –2.5 | µA |
| TUE_TS | Total Unadjusted Error | Ideal Diode Assumed | ● | | | ±3 | °C |
| N_TS | Maximum Ideality Factor | READ_TEMPERATURE_1 = 175°C<br>MFR_TEMP1_GAIN = 1/N_TS | | | | 1.10 | |
| **Internal Temperature Sensor Characteristics (READ_TEMPERATURE_2)** | | | | | | | |
| TUE_TS2 | Total Unadjusted Error | | | | ±1 | | °C |
| **$V_{OUT}$ Enable Output ($V_{OUT\_EN[3:0]}$) Characteristics** | | | | | | | |
| $V_{VOUT\_EN}$*n* | Output High Voltage | $I_{VOUT\_EN}$*n* = –5µA, $V_{DD33}$ = 3.13V | ● | 10 | 13 | 14.7 | V |
| $I_{VOUT\_EN}$*n* | Output Sourcing Current | $V_{VOUT\_EN}$*n* Pull-Up Enabled, $V_{VOUT\_EN}$*n* = 1V | ● | –5 | –7 | –9 | µA |
| | Output Sinking Current | Strong Pull-Down Enabled, $V_{VOUT\_EN}$*n* = 0.4V | ● | 3 | 5 | 8 | mA |
| | | Weak Pull-Down Enabled, $V_{VOUT\_EN}$*n* = 0.4V | ● | 33 | 50 | 65 | µA |
| | Output Leakage Current | Internal Pull-Up Disabled, 0V ≤ $V_{VOUT\_EN}$*n* ≤ 15V | ● | | | ±1 | µA |
| $V_{VOUT\_VALID}$ | Minimum $V_{DD33}$ when $V_{OUT\_EN}$*n* Valid | $V_{VOUT\_EN}$*n* ≤ 0.4V | ● | | | 1.1 | V |
| **General Purpose Output (AUXFAULTB) Characteristics** | | | | | | | |
| $V_{AUXFAULTB}$ | Output High Voltage | $I_{AUXFAULTB}$ = –5µA, $V_{DD33}$ = 3.13V | ● | 10 | | 14.7 | V |
| $I_{AUXFAULTB}$ | Output Sourcing Current | AUXFAULTB Pull-Up Enabled, $V_{AUXFAULTB}$ = 1V | ● | –5 | –7 | –9 | µA |
| | Output Sinking Current | Strong Pull-Down Enabled, $V_{AUXFAULTB}$ = 0.4V | ● | 3 | 5 | 8 | mA |
| | Output Leakage Current | Internal Pull-Up Disabled, 0V ≤ $V_{AUXFAULTB}$ ≤ 15V | ● | | | ±1 | µA |
| **EEPROM Characteristics** | | | | | | | |
| Endurance | (Note 8) | 0°C < $T_J$ < 85°C During EEPROM Write Operations | ● | 10,000 | | | Cycles |
| Retention | (Note 8) | $T_J$ < 105°C | ● | 10 | | | Years |
| $t_{MASS\_WRITE}$ | Mass Write Operation Time (Note 9) | STORE_USER_ALL, 0°C < $T_J$ < 85°C During EEPROM Write Operations | ● | | 440 | 4100 | ms |

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## ELECTRICAL CHARACTERISTICS

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| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $t_{SU,STO}$ | Stop Condition Setup Time (Note 10) | | ● | 600 | | | ns |
| $t_{HD,DAT}$ | Data Hold Time (LTC2974 Receiving Data) (Note 10) | | ● | 0 | | | ns |
| | Data Hold Time (LTC2974 Transmitting Data) (Note 10) | | ● | 300 | | 900 | ns |
| $t_{SU,DAT}$ | Data Setup Time (Note 10) | | ● | 100 | | | ns |
| $t_{SP}$ | Pulse Width of Spike Suppressed (Note 10) | | | | 98 | | ns |
| $t_{TIMEOUT\_BUS}$ | Time Allowed to Complete any PMBus Command After Which Time SDA Will Be Released and Command Terminated | Mfr_config_all_longer_pmbus_timeout = 0<br>Mfr_config_all_longer_pmbus_timeout = 1 | ●<br>● | | 25<br>200 | 35<br>280 | ms<br>ms |
| **Additional Digital Timing Characteristics** | | | | | | | |
| $t_{OFF\_MIN}$ | Minimum Off Time for Any Channel | | | | 100 | | ms |

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** All currents into device pins are positive. All currents out of device pins are negative. All voltages are referenced to GND unless otherwise specified. If power is supplied to the chip via the $V_{DD33}$ pin only, connect $V_{PWR}$ and $V_{DD33}$ pins together.

**Note 3:** The ADC total unadjusted error includes all error sources. First, a two-point analog trim is performed to achieve a flat reference voltage ($V_{REF}$) over temperature. This results in minimal temperature coefficient, but the absolute voltage can still vary. To compensate for this, a high-resolution, drift-free, and noiseless digital trim is applied at the output of the ADC, resulting in a very high accuracy measurement.

**Note 4:** Hysteresis in the output voltage is created by package stress that differs depending on whether IC was previously at a higher or lower temperature. Output voltage is always measured at 25°C, but the IC is cycled to 105°C or –40°C before successive measurements. Hysteresis is roughly proportional to the square of the temperature change.

**Note 5:** The current sense resolution is determined by the L11 format, the value of IOUT_CAL_GAIN, and the magnitude of the current being measured. See Table 2 for details.

**Note 6:** The nominal time between successive ADC conversions (latency of the ADC) for any given channel is $t_{UPDATE\_ADC}$.

**Note 7:** Nonlinearity is defined from the first code that is greater than or equal to the maximum offset specification to full-scale code, 1023.

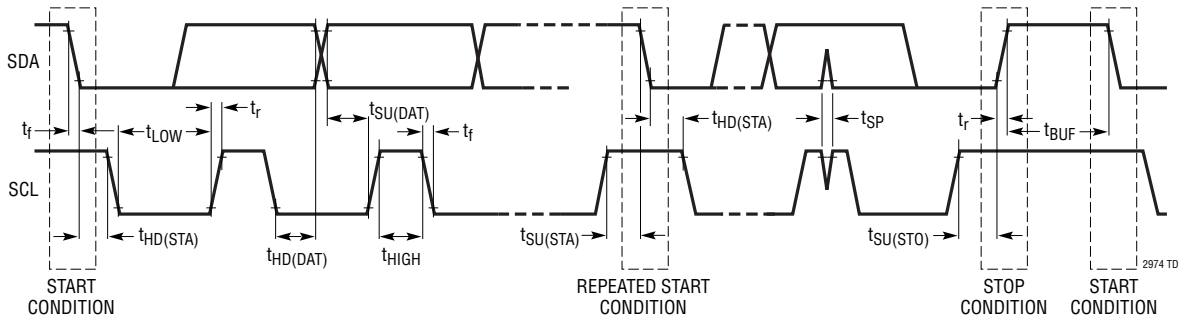
**Note 8:** EEPROM endurance and retention are guaranteed by design, characterization and correlation with statistical process controls. The minimum retention specification applies for devices whose EEPROM has been cycled less than the minimum endurance specification.

**Note 9:** Add 74 will not acknowledge any PMBus commands, except for MFR_COMMON, when a STORE_USER_ALL command is being executed. See also OPERATION section.

**Note 10:** Maximum capacitive load, $C_B$, for SCL and SDA is 400pF. Data and clock risetime ($t_r$) and falltime ($t_f$) are: (20 + 0.1• $C_B$) (ns) < $t_r$ < 300ns and (20 + 0.1 • $C_B$) (ns) < $t_f$ < 300ns. $C_B$ = capacitance of one bus line in pF. SCL and SDA external pull-up voltage, $V_{IO}$, is 3.13V < $V_{IO}$ < 3.6V.

**Note 11:** $V_{SENSE}$ and $I_{SENSE}$ input currents are characterized by input current and input differential current. Input current is defined as current into a single device pin (see Note 2). Input differential current is defined as ($I^+ – I^–$) where $I^+$ is the current into the positive device pin and $I^–$ is the current into the negative device pin.

## PMBUS TIMING DIAGRAM



# OPERATION

## LTC2974 OPERATION OVERVIEW

The LTC2974 is a PMBus programmable power supply controller, monitor, sequencer and voltage and current supervisor that can perform the following operations:

- Accept PMBus compatible programming commands.
- Provide DC/DC converter input voltage, output voltage, output current, output temperature, and internal junction temperature readback through the PMBus interface.
- Control the output of DC/DC converters that set the output voltage with a trim pin or DC/DC converters that set the output voltage using an external resistor feedback network.
- Sequence the startup of DC/DC converters via PMBus programming and the CONTROL input pins. The LTC 2974 supports time-based sequencing and tracking sequencing. Cascade sequence on with time based sequence off is also supported.
- Trim the DC/DC converter output voltage (typically in 0.02% steps), in closed-loop servo operating mode, autonomously or through PMBus programming.
- Margin the DC/DC converter output voltage to PMBus programmed limits.
- Trim or margin the DC/DC converter output voltage with direct access to the margin DAC.
- Supervise the DC/DC converter input voltage, output voltage, load current and the inductor temperatures for overvalue/undervalue conditions with respect to PMBus programmed limits and generate appropriate faults and warnings.
- Accurately handle inductor self-heating transients using a proprietary algorithm. These self-heating effects are combined with external temperature sensor readings to improve accuracy of current supervisors and ADC current measurement.
- Respond to a fault condition by continuing operation indefinitely, latching-off after a programmable deglitch period, latching-off immediately or sequencing off after TOFF_DELAY. Use retry mode to automatically recover from a latched-off condition. With retry enabled, MFR_RETRY_COUNT programs the number of retries (0 to 6 or infinite) for all pages.
- Optionally stop trimming the DC/DC converter output voltage after it reaches the initial margin or nominal target. Optionally allow servo to resume if target drifts outside of $V_{OUT}$ warning limits.
- Store command register contents to EEPROM with CRC and ECC through PMBus programming.
- Restore EEPROM contents through PMBus programming or when $V_{DD33}$ is applied on power-up.
- Report the DC/DC converter output voltage status through the power good output.
- Generate interrupt requests by asserting the ALERTB pin in response to supported PMBus faults and warnings.
- Coordinate system wide fault responses for all DC/DC converters connected to the LTC2974 FAULTB0 and FAULTB1 pins.
- Synchronize sequencing delays or shutdown for multiple devices using the SHARE_CLK pin.
- Software and hardware write protect the command registers.
- Disable the input voltage to the supervised DC/DC converters in response to output OV, UV, OC and UC faults.
- Log telemetry and status data to EEPROM in response to a faulted-off condition.
- Supervise an external microcontroller's activity for a stalled condition with a programmable watchdog timer and reset it if necessary.
- Prevent a DC/DC converter from re-entering the on state after a power cycle until a programmable interval (MFR_RESTART_DELAY) has elapsed and its output has decayed below a programmable threshold voltage (MFR_VOUT_DISCHARGE_THRESHOLD).
- Record minimum and maximum observed values of input voltage, output voltages, output currents and output temperatures.
- Access user EEPROM data directly, without altering RAM space (Mfr_ee_unlock, Mfr_ee_erase, and Mfr_ee_data). Facilitates in-house bulk programming.
- . Accommodate multiple hosts with Command Plus

Add

# PMBUS COMMAND SUMMARY

**Summary Table**

| COMMAND NAME | CMD CODE | DESCRIPTION | TYPE | PAGED | DATA FORMAT | UNITS | EEPROM | DEFAULT VALUE: FLOAT HEX | REF PAGE |
|---|---|---|---|---|---|---|---|---|---|
| USER_DATA_03 | 0xB3 | Scratchpad location. | R/W Word | Y | Reg | | Y | 0x0000 | 84 |
| USER_DATA_04 | 0xB4 | Scratchpad location. | R/W Word | N | Reg | | Y | 0x0000 | 84 |
| MFR_LTC_RESERVED_1 | 0xB5 | Manufacturer reserved. | R/W Word | Y | Reg | | Y | NA | 84 |
| MFR_INFO | 0xB6 | Manufacturer specific information. | R Word | N | Reg | | | NA | 83 |
| MFR_T_SELF_HEAT | 0xB8 | Calculated temperature rise due to self-heating of output current sense device above value measured by external temperature sensor. | R Word | Y | L11 | °C | | NA | 52 |
| MFR_IOUT_CAL_GAIN_TAU_INV | 0xB9 | Inverse of time constant for Mfr_t_self_heat changes scaled by 4 • $t_{CONV\_SENSE}$. | R/W Word | Y | L11 | | Y | 0.0 0x8000 | 52 |
| MFR_IOUT_CAL_GAIN_THETA | 0xBA | Thermal resistance from inductor core to point measured by external temperature sensor. | R/W Word | Y | L11 | °C/W | Y | 0.0 0x8000 | 52 |
| MFR_READ_IOUT | 0xBB | Alternate data format for READ_IOUT. One LSB = 2.5mA. | R Word | Y | CF | 2.5mA | | NA | 70 |
| MFR_LTC_RESERVED_2 | 0xBC | Manufacturer reserved. | R/W Word | Y | Reg | | | NA | 84 |
| MFR_EE_UNLOCK | 0xBD | Unlock user EEPROM for access by MFR_EE_ERASE and MFR_EE_DATA commands. | R/W Byte | N | Reg | | | NA | 44 |
| MFR_EE_ERASE | 0xBE | Initialize user EEPROM for bulk programming by MFR_EE_DATA. | R/W Byte | N | Reg | | | NA | 44 |
| MFR_EE_DATA | 0xBF | Data transferred to and from EEPROM using sequential PMBus word reads or writes. Supports bulk programming. | R/W Word | N | Reg | | | NA | 44 |
| MFR_COMMAND_PLUS | 0xC8 | Alternate access to block read and other data. Commands for all additional hosts. | R/W Word | N | Reg | | | | 29 |
| MFR_DATA_PLUS0 | 0xC9 | Alternate access to block read and other data. Data for additional host 0. | R/W Word | N | Reg | | | | 29 |
| MFR_DATA_PLUS1 | 0xCA | Alternate access to block read and other data. Data for additional host 1. | R/W Word | N | Reg | | | | 29 |
| MFR_CONFIG_LTC2974 | 0xD0 | Configuration bits that are channel specific. | R/W Word | Y | Reg | | Y | 0x0080 | 34 |
| MFR_CONFIG_ALL_LTC2974 | 0xD1 | Configuration bits that are common to all pages. | R/W Word | N | Reg | | Y | 0x0F7B | 34 |
| MFR_FAULTB0_PROPAGATE | 0xD2 | Configuration that determines if a channel's faulted off state is propagated to the FAULTB0 pin. | R/W Byte | Y | Reg | | Y | 0x00 | 63 |
| MFR_FAULTB1_PROPAGATE | 0xD3 | Configuration that determines if a channel's faulted off state is propagated to the FAULTB1 pin. | R/W Byte | Y | Reg | | Y | 0x00 | 63 |
| MFR_PWRGD_EN | 0xD4 | Configuration that maps WDI/RESETB status and individual channel power good to the PWRGD pin. | R/W Word | N | Reg | | Y | 0x0000 | 56 |
| MFR_FAULTB0_RESPONSE | 0xD5 | Action to be taken by the device when the FAULTB0 pin is asserted low. | R/W Byte | N | Reg | | Y | 0x00 | 63 |
| MFR_FAULTB1_RESPONSE | 0xD6 | Action to be taken by the device when the FAULTB1 pin is asserted low. | R/W Byte | N | Reg | | Y | 0x00 | 63 |

Add

# PMBUS COMMAND SUMMARY

**Summary Table**

| COMMAND NAME | CMD CODE | DESCRIPTION | TYPE | PAGED | DATA FORMAT | UNITS | EEPROM | DEFAULT VALUE: FLOAT HEX | REF PAGE |
|---|---|---|---|---|---|---|---|---|---|
| MFR_IOUT_PEAK | 0xD7 | Maximum measured value of READ_IOUT. | R Word | Y | L11 | A | | NA | 70 |
| MFR_IOUT_MIN | 0xD8 | Minimum measured value of READ_IOUT. | R Word | Y | L11 | A | | NA | 70 |
| MFR_CONFIG2_LTC2974 | 0xD9 | Configuration bits that are channel specific | R/W Byte | N | Reg | | Y | 0x00 | 34 |
| MFR_CONFIG3_LTC2974 | 0xDA | Configuration bits that are channel specific | R/W Byte | N | Reg | | Y | 0x00 | 34 |
| MFR_RETRY_DELAY | 0xDB | Retry interval during FAULT retry mode. | R/W Word | N | L11 | ms | Y | 200 0xF320 | 58 |
| MFR_RESTART_DELAY | 0xDC | Delay from actual CONTROL active edge to virtual CONTROL active edge. | R/W Word | N | L11 | ms | Y | 400 0xFB20 | 55 |
| MFR_VOUT_PEAK | 0xDD | Maximum measured value of READ_VOUT. | R Word | Y | L16 | V | | NA | 70 |
| MFR_VIN_PEAK | 0xDE | Maximum measured value of READ_VIN. | R Word | N | L11 | V | | NA | 70 |
| MFR_TEMPERATURE_1_PEAK | 0xDF | Maximum measured value of READ_ TEMPERATURE_1. | R Word | Y | L11 | °C | | NA | 70 |
| MFR_DAC | 0xE0 | The code of the 10-bit DAC. | R/W Word | Y | Reg | | | 0x0000 | 48 |
| MFR_POWERGOOD_ ASSERTION_DELAY | 0xE1 | Power-good output assertion delay. | R/W Word | N | L11 | ms | Y | 100 0xEB20 | 56 |
| MFR_WATCHDOG_T_FIRST | 0xE2 | First watchdog timer interval. | R/W Word | N | L11 | ms | Y | 0 0x8000 | 56 |
| MFR_WATCHDOG_T | 0xE3 | Watchdog timer interval. | R/W Word | N | L11 | ms | Y | 0 0x8000 | 56 |
| MFR_PAGE_FF_MASK | 0xE4 | Configuration defining which channels respond to global page commands (PAGE=0xFF). | R/W Byte | N | Reg | | Y | 0x0F | 29 |
| MFR_PADS | 0xE5 | Current state of selected digital I/O pads. | R/W Word | N | Reg | | | NA | 65 |
| MFR_I2C_BASE_ADDRESS | 0xE6 | Base value of the $I^2C$/SMBus address byte. | R/W Byte | N | Reg | | Y | 0x5C | 0x0215 |
| MFR_SPECIAL_ID | 0xE7 | Manufacturer code for identifying the LTC2974. | R Word | N | Reg | | Y | ~~0x0214~~ | 83 |
| MFR_SPECIAL_LOT | 0xE8 | Customer dependent codes that identify the factory programmed user configuration stored in EEPROM. Contact factory for default value. | R Byte | Y | Reg | | Y | NA | 83 |
| MFR_VOUT_DISCHARGE_ THRESHOLD | 0xE9 | Coefficient used to multiply VOUT_ COMMAND in order to determine $V_{OUT}$ off threshold voltage. | R/W Word | Y | L11 | | Y | 2.0 0xC200 | 48 |
| MFR_FAULT_LOG_STORE | 0xEA | Command a transfer of the fault log from RAM to EEPROM. | Send Byte | N | | | | NA | 74 |
| MFR_FAULT_LOG_RESTORE | 0xEB | Command a transfer of the fault log previously stored in EEPROM back to RAM. | Send Byte | N | | | | NA | 74 |
| MFR_FAULT_LOG_CLEAR | 0xEC | Initialize the EEPROM block reserved for fault logging and clear any previous fault logging locks. | Send Byte | N | | | | NA | 74 |
| MFR_FAULT_LOG_STATUS | 0xED | Fault logging status. | R Byte | N | Reg | | Y | NA | 74 |

# PMBUS COMMAND DESCRIPTION

The following example illustrates configuring an LTC2974 with one master channel and three slaves.

Master channel 0

TON_DELAY = Ton_delay_master

TON_RISE = Ton_rise_master

TOFF_DELAY = Toff_delay_master

Mfr_track_en_chan0 = 0

Slave channel *n*

TON_DELAY = Ton_delay_slave

TON_RISE = Ton_delay_master + Ton_rise_slave

TOFF_DELAY = Toff_delay_master + T_off_delay_slave

Mfr_track_en_chan0 = 1

Where:

Ton_delay_master – Ton_delay_slave > RUN to TRACK setup time

Toff_delay_slave > time for master supply to fall.

The system response to a control pin toggle is illustrated in Figure 18.

The system response to a UV fault on a slave channel is illustrated in Figure 19.

### *MFR_CONFIG_ALL_LTC2974*

This command is used to configure parameters that are common to all channels on the IC. They may be set or reviewed from any PAGE setting.

**MFR_CONFIG_ALL_LTC2974 Data Contents**

| BIT(S) | SYMBOL | OPERATION |
|---|---|---|
| b[15:12] | Reserved | Don't care. Always returns 0. |
| b[11] | Mfr_config_all_pwrgd_off_uses_uv | Selects PWRGD de-assertion source for all channels.<br>0: PWRGD is de-asserted based on $V_{OUT}$ being below or equal to POWER_GOOD_OFF. This option uses the ADC. Response time is approximately 100ms to 200ms.<br>1: PWRGD is de-asserted based on $V_{OUT}$ being below or equal to VOUT_UV_LIMIT. This option uses the high speed supervisor. Response time is approximately 12µs. |
| b[10] | ~~Mfr_config_all_fast_fault_log~~<br>Reserved | ~~Controls number of ADC readings completed before transferring fault log memory to EEPROM.~~<br>~~0: All ADC telemetry values will be updated before transferring fault log to EEPROM. Slower.~~<br>~~1: Telemetry values will be transferred from fault log to EEPROM within 24ms after detecting fault. Faster.~~ |
| b[9] | Mfr_config_all_control3_pol | Selects active polarity of CONTROL3 pin<br>0: Active low (pull pin low to start unit).<br>1: Active high (pull pin high to start unit). |
| b[8] | Mfr_config_all_control2_pol | Selects active polarity of CONTROL2 pin<br>0: Active low (pull pin low to start unit).<br>1: Active high (pull pin high to start unit). |