1. Electro-Static Discharge (ESD) Test Results

1.1 Test Description

The HBM ESD testing was performed on a THERMOFISHER Mk.2 using the Human Body Module per JESD22-A114. This test is performed for classification only. **Class 1A >±250V, Class 1B >±500V, Class 1C >±1000V, Class 2 >±2000V, Class 3A >±4000V and Class 3B >±8000V. A copy of the circuit is shown below:**

1.2 Test Circuit & Condition

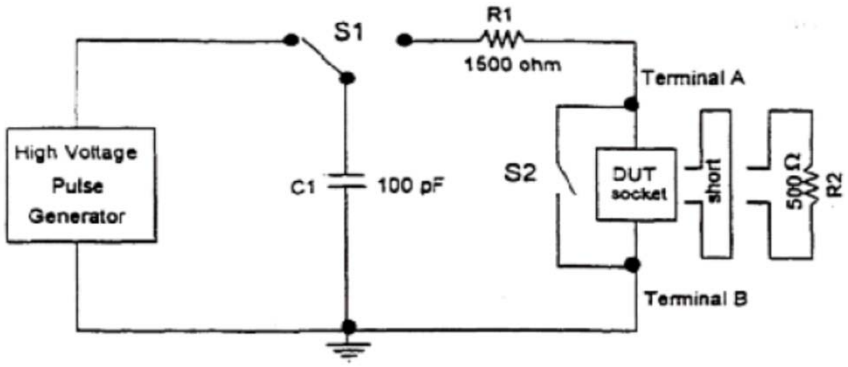


Figure 1 — Typical equivalent HBM ESD circuit

NOTE 1 The performance of any simulator is influenced by its parasitic capacitance and inductance.

NOTE 2 Precautions must be taken in tester design to avoid recharge transients and multiple pulses.

NOTE 3 R2, used for initial equipment qualification and requalification as specified in 3.1, shall be a low inductance, 4000 V, 500 Ω resistor with +/-1% tolerance.

NOTE 4 Stacking of DUT socket adaptors (piggybacking) is allowed only if the waveforms can be verified to meet the specifications in Table 1.

NOTE 5 Reversal of terminals A and B to achieve dual polarity is not permitted.

NOTE 6 S2 shall be closed at least 10 milliseconds after the pulse delivery period to ensure the DUT socket is not left in a charged state.

NOTE 7 R1, 1500 Ω +/- 1%.

NOTE 8 C1, 100 pF +/- 10% (effective capacitance).

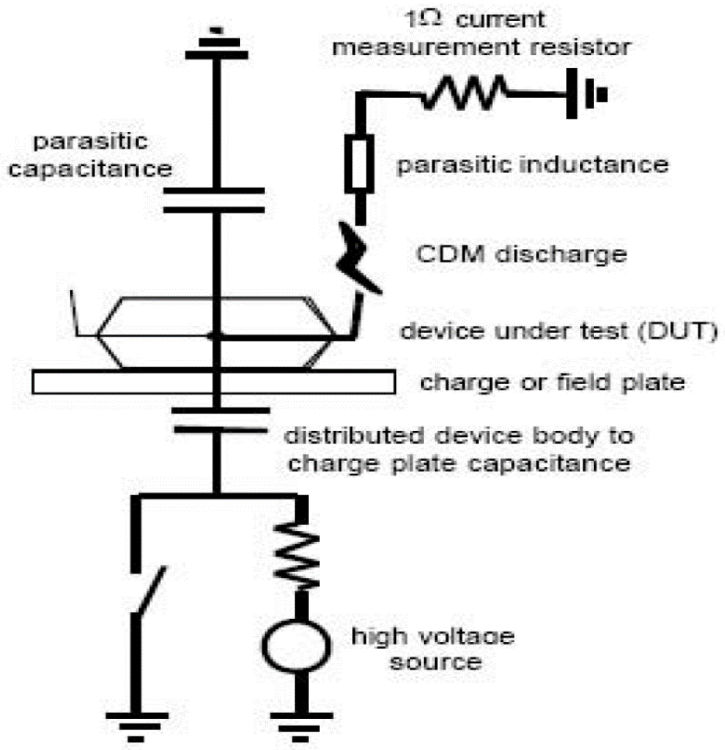
1.3 ESD Data

Device	Model	S/S	Pins	Voltage Passed	Voltage Failed
LTC6813	HBM Class 1C	3	All Pins	>±1000V	

1.7 Test Description

The Charged Device Model (CDM) ESD testing was performed on a THERMOFISHER RCDM system per ESDA ESD STM5.3.1-1999 / AEC-Q100-011-Rev-B. This test is performed for information only. A copy of the circuit is shown below:

1.8 Test Circuit & Condition



(b) Field induced charge CDM

1.9 ESD Data

Device	Model	S/S	Pins	Voltage Passed	Voltage Failed
LTC6813	CDM	3	All Pins	>±750V	

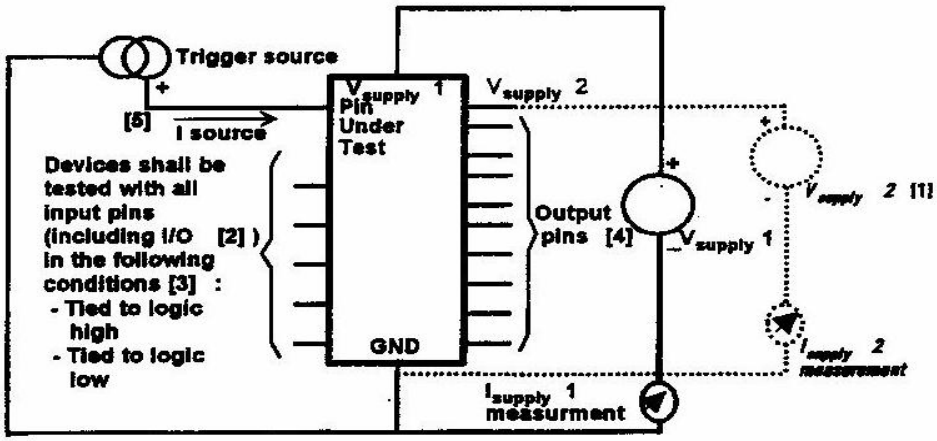
4. Latch-Up Test Results

4.1 Test Description

Latchup Testing was performed at +25°C and +125°C using the LTX Integrated Circuit Test system. The Power Supply pins are biased to the appropriate Datasheet specifications and the individual non-Power Supply pins are tested incrementally while the current is monitored until failure occurs.

4.2 Test Circuit & Condtion

4.2.1 Test Circuit 1

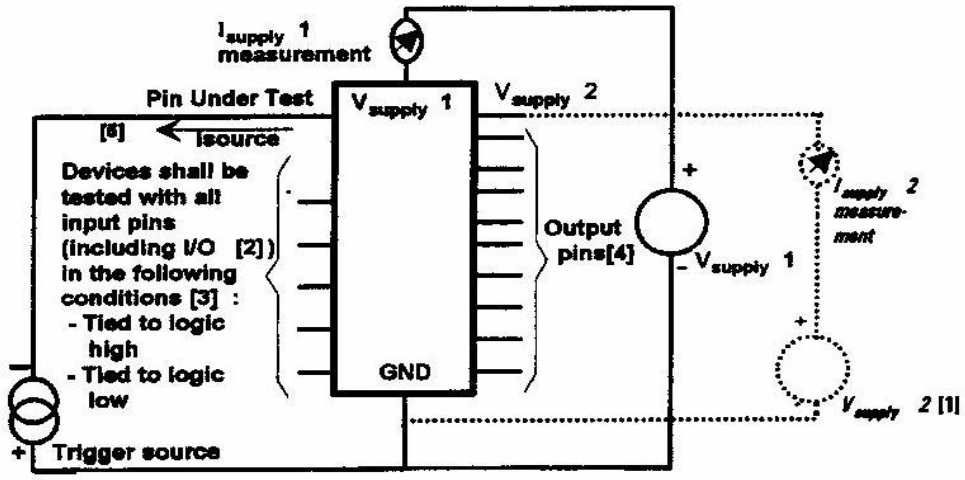


1. DUT biasing shall include additional $V_{supplies}$ as required.
2. DUT shall be preconditioned so that all I/O pins are placed in a valid state per 4.1. I/O pins in the output state shall be open circuit.
3. Logic high and logic low shall be per the device specification. When logic levels are used in respect to a non-digital device, it means the maximum high or minimum low voltage that can be supplied to the pin per the device specifications, unless these conditions violate device setup condition requirements.
4. Output pins shall be open circuit except when latch-up tested.
5. The trigger test condition is defined in figure 2 and table 1.

NOTE: Dynamic devices may have timing signals applied per 4.2.3.

Figure 5 - The equivalent circuit for positive input/output I-test latch-up testing

4.2.2 Test Circuit 2



1. DUT biasing shall include additional Vsupplies as required.
2. DUT shall be preconditioned so that all I/O pins are placed in a valid state per 4.1. I/O pins in the output state shall be open circuit.
3. Logic high and logic low shall be per the device specification. When logic levels are used with respect to a non-digital device, it means the maximum high or minimum low voltage that can be supplied to the pin per the device specification, unless these conditions violate the device setup condition requirements.
4. Output pins shall be open circuit except when latch-up tested.
5. The trigger test condition is defined in figure 3 and table 1.

NOTE: Dynamic devices may have timing signals applied per 4.2.3.

Figure 6 - The equivalent circuit for negative input/output I-test latch-up testing

4.3 Latch-Up Data

Device	Mode	Current	Temp	S/S	Results
LTC6813	CKT1 & CKT2	>±200mA	+25°C	5	PASS
	CKT1 & CKT2	>±100mA	+125°C	5	PASS