Product/Process Change Notice - PCN 21_0015 Rev. -

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This notice is to inform you of a change that will be made to certain ADI products (see Appendix A) that you may have purchased in the last 2 years. **Any inquiries or requests with this PCN (additional data or samples) must be sent to ADI within 30 days of publication date.** ADI contact information is listed below.

PCN Title: AD9082 Die Revision and Data Sheet Change

Publication Date: 01-Feb-2021

Effectivity Date: 12-Feb-2021 *(the earliest date that a customer could expect to receive changed material)*

Revision Description:
Initial Release.

Description Of Change:

A die revision (R2) and Thermal Interface Material (TIM) change has been completed for the AD9082 resulting in multiple improvements in performance and added functions. A summary of the changes are as follows:

Die Rev and Thermal Interface Material (TIM) Changes:

1. JESD204C maximum lane rate increased to 24.75Gbps. R2 is backwards compatible with R1R revision modes of operation, with the API version 1.0.7 or higher.

2. Added Receive Path (ADC) JESD user modes. Refer to the Device User Guide, UG-1578.

3. Added Slew rate detector to Tx PA protection feature. Refer to the Device User Guide, UG-1578.

4. Sub-class 1 robustness improvement. Refer to attached Revision History document.

4. Improved package thermal conductivity characteristics. (Table 13, AD9082 Rev B data sheet).

5. Added Temperature Monitoring Unit (TMU) functionality. Refer to the Device User Guide, UG-1578.

Data sheet Changes:

1. SPI clock rate increased to 33MHz.

2. Increased storage temperature range to -65C to +150C. (Table 18, AD9082 Rev B data sheet)

3. Added ordering part number AD9082BBPCZ-2D2AC (DAC1 and DAC3 disabled at start up).

4. Added maximum Rx input power (Table 12, AD9082 Rev B data sheet).

5. Added min/max limits to A/C specs. Refer to the AD9082, Rev B data sheet and attached Revision History Document.

6. Absolute maximum Tj decreased from 125C to 120C due to a typographical error. Note that maximum specified operating range remains at 120C. (Table 12, AD9082 Rev B data sheet).

Device Revision Identifiers:

1. ChipID register 0x006 read back value changed from 0x2 (R1R) to 0x3 (R2). Refer to attached Revision History document.

2. Applicable date codes: 2043 or later and API version 1.0.7 or higher should be used.

Reason For Change:

Upgrade the JESD204C lane rate to support up to a maximum 24.75Gbps.

Impact of the change (positive or negative) on fit, form, function & reliability:

No Change to fit, form, or reliability. Improved functionality. API usage requires upgrading to version 1.0.7 or later versions.

Product Identification *(this section will describe how to identify the changed material)*

Date codes of 2043 or later. ChipID register 0x006 rad back value = 0x3

Summary of Supporting Information:

Qualification has been performed per Industry Standard Test Methods. See attached Qualification Results Summary.

Supporting Documents

Attachment 1: Type: Datasheet Specification Comparison

ADI_PCN_21_0015_Rev_-_AD9082_Revision_History_for R3 Jan2021.pdf

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Attachment 2: Type: Qualification Results Summary

ADI_PCN_21_0015_Rev_-_AD9082 Qualification Results Summary.pdf

For questions on this PCN, please send an email to the regional contacts below or contact your local ADI sales representatives.			
Americas: PCN_Americas@analog.com	**Europe:** PCN_Europe@analog.com	**Japan:** PCN_Japan@analog.com	**Rest of Asia:** PCN_ROA@analog.com

Appendix A - Affected ADI Models				
Added Parts On This Revision - Product Family / Model Number (2)				
AD9082 / AD9082BBPZ-4D2AC	AD9082 / AD9082BBPZRL-4D2AC			

Appendix B - Revision History			
Rev	**Publish Date**	**Effectivity Date**	**Rev Description**
Rev. -	01-Feb-2021	12-Feb-2021	Initial Release.