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RAQ Issue 205: How Do You Amplify AC Signals with Large DC Offsets Using an Indirect Current-Mode In-Amp?

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Question:

How do I eliminate the need for additional gain stages while supporting applications where large differential offset voltages exist?

Answer:

This can be accomplished by designing an AC coupling and gaining solution in one stage using a micropower, rail-to-rail indirect current-mode instrumentation amplifier. This article will outline the design benefits and provide a step-by-step design guide.

Introduction

In applications such as electromagnetic flow (EM flow) meters and biopotential measurements, small differential signals are in series with much larger differential offsets. These offsets typically limit the gain that the circuit can take in the front-end design, which in turn impacts the overall dynamic range. The gain limitation is even more challenging when lower supply voltages are used—for example, in battery-powered signal chains. One solution to address this large differential offset issue is to use an AC-coupled measurement signal chain. A typical AC-coupled signal chain would include a low gain instrumentation amplifier, followed by a high-pass filter and additional gain stages (see "Amplifying AC Signals with Large DC Offsets for Low Power Designs"). In most applications, it is preferable to get as much gain as possible at the first stage as this helps in improving the referred to input (RTI) noise of the following gain stages in the signal chain. This article will assist with the design and the implementation of an indirect current-mode instrumentation amplifier (in-amp) architecture, which will enable high gain, and AC coupling all in one stage. The design will feature the AD8237, a micropower, zero-drift instrumentation amplifier that has a wide common mode and differential input range. Other examples of the indirect current-mode architecture include the AD8420. The main benefits of such an indirect current feedback in-amp are:

- It is a low power architecture
- There is no diamond plot limitation like with other typical architectures such as in-amps composed of two or three op amps

- Good gain drift performance can be achieved from external resistor matching
- High CMRR can be achieved without relying on resistor matching
- High impedance reference pin

The circuit in Figure 1 provides the overall schematic where the AD8237 indirect current-mode in-amp is chosen. However, to accomplish high gain and AC coupling all in one stage, an integrator circuit has to be implemented in a feedback loop with the AD8237. This solution allows more gain than instrumentation amplifier solutions composed of two or three op amps, which cancel the offset after gain has been applied. For the proposed architecture, the offset correction happens prior to the gain phase that allows the in-amp to have a large gain. Both architectures will be presented in the appendix. The ADA4505 op amp is used in the feedback loop as the integrator circuit. The output of the AD8237 is sensed by the integrator input and drives the reference pin of the AD8237 to force the output of the AD8237 to V_{MID}, which is set on the +input of the ADA4505. Even though the integrator circuit provides a low-pass filter function, in this situation, due to its use in the feedback loop, the overall circuit will have a high-pass filter transfer function. Thanks to this behavior, not only will it ultimately block any DC offsets prior to gain that will allow increasing the gain further than other solutions, but also it is even more helpful with low supply voltages and large offsets since the headroom left to work with is limited. The integrator circuit also forces the output of the AD8237 at a chosen voltage via a reference pin. Indeed, the integrator is forcing the reference pin relative to the FB pin of the AD8237 to be equal and opposite to the differential voltage of the inputs.

Design Specifications Example

For low power applications, a single supply is usually available, which is usually somewhere between 1.8 V and 3.6 V. The design choices for the circuit shown in Figure 1 depend on the input signal and offset amplitude range and frequency. Table 1 lists example design specifications for the circuit in Figure 1.

The design choices for this circuit were made while using a low bandwidth mode for the AD8237, allowing for gain flexibility and better stability.

Table 1. Key Design Specifications for Circuit in Figure 1

Sensor V_{OFFSET} Max Amplitude	Sensor V_{SIGNAL} Max Amplitude	Sensor V_{SIGNAL} Min/Max Frequency	Sensor Common Mode (V_{CM})	Supplies V_{DD}/V_{SS}	Supply Current Max	V_{MID} Output Common Mode
±1 V	±6 mV	20 Hz/220 Hz	1.65 V	+3.3 V/0 V	200 µA	1.65 V

Design Description

The circuit in Figure 1 is composed of the AD8237, a micropower, rail-to-rail instrumentation amplifier, and the ADA4505, a zero input crossover distortion op amp. Both can be powered from a minimum 3.3 V supply, V_{DD}.

This circuit can output a voltage, V_{OUT}, which represents the amplification of the AC signal, V_{SIGNAL}, presented at the input while removing any DC offset voltages, V_{OFFSET}. A V_{MID} voltage is generated to set both the positive input of the ADA4505 and the AD8237 gain stage output common mode to mid-supply. The V_{MID} is generated with a voltage divider (R1, R2) and buffered by another ADA4505. The AD8237 comes in a mini small outline package (MSOP) and the ADA4505 comes in a compact wafer-level chip scale package (WLCSP).

Design Considerations

1. The positive input of the ADA4505-2 (1/2), V_{MID}, will set the value of V_{REF} (Ref pin of AD8237) and consequently, the output, V_{OUT}. To ensure the maximum output swing between the two supply rails, most instrumentation amplifiers' optimal value is at mid-supply ($+V_{DD}/2$) due to the common-mode input voltage vs. output range or diamond plot. A diamond plot tool to help with this will be presented in the design simulations section.
2. When considering the total supply current for the circuit, the choice of resistor values R1 and R2 also matters. The resistor choice is a trade-off between noise and power dissipation. In the case of this circuit, it is better to choose larger resistor values to minimize additional supply current. Additional supply current added for this resistor divider would be:

$$I_1 = \frac{V_{DD}}{R1 + R2}$$

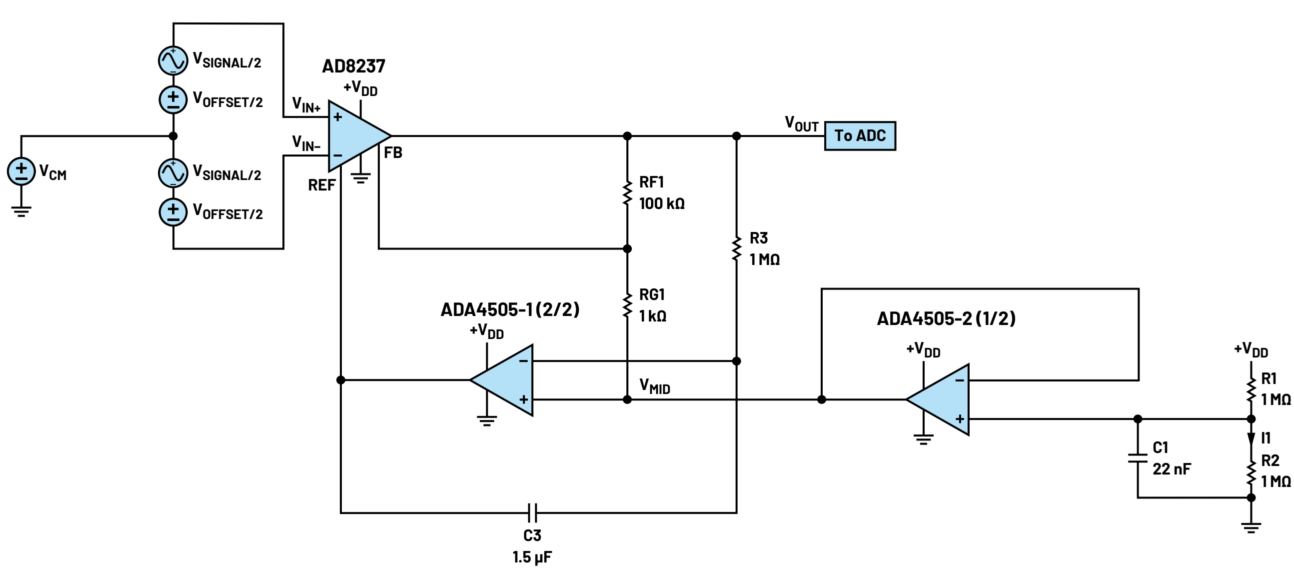

Figure 1. AC-coupled signal conditioning circuit with indirect current-mode architecture.

- In the case of the resistor divider (R1, R2), an additional capacitor C1 can be added to bandlimit the noise as well as reduce any 50 Hz/60 Hz or other interference on V_{DD}. The larger the capacitor, the better the noise filtering; however, it will take V_{MID} longer to settle at power-up. The estimated time it takes to settle within 1%:

$$t_{SETTLE}\ V_{MID} = 5 \times \frac{R1 \times R2 \times C1}{R1 + R2}$$

3. When choosing passive component values (resistors and capacitors), the tolerances should be considered. In the case of the resistor divider (R1, R2), the target V_{MID} value can shift, which would influence the output swing ranges V_{OUT} of the AD8237 and ADA4505.

   From the circuit in Figure 1, the transfer function will have two cutoff frequencies that are the result of a high-pass filter coming from the ADA4505 integrator circuit in feedback and a low-pass filter response due to the AD8237 bandwidth. Some gain error can be introduced, which relates to the cutoff frequency of the integrator (ADA4505) in combination with the AD8237 bandwidth. Thus, it is important that the high pass cutoff frequency and the low pass cutoff frequency respect a certain span. Depending on how close cutoff frequencies are to each other, the percentage gain error might change.

4. If the application requires the use of high impedance sensors, buffers such as the ADA4505 could be used in front of the AD8237 inputs to provide higher input impedance and lower input bias current, as a buffer will convert a high impedance input into a low impedance output. The AD8237 input bias current is 1 nA maximum over temperature.

Design Procedure

1. Voltage divider for setting V_{MID}:

Using section 2 of Design Considerations, for the circuit in Figure 1, the values for the peripheral components are set to R1 = R2 = 1 MΩ to keep the supply current contribution around 1 µA.

$$I_1 = \frac{3.3\ \text{V}}{1\ \text{M}\Omega + 1\ \text{M}\Omega} = 1.65\ \mu\text{A}$$

Output of the resistor divider prior to the ADA4505:

$$V_{MID} = V_{DD} \times \frac{R2}{R1 + R2} = 3.3 \times \frac{1\ \text{M}\Omega}{1\ \text{M}\Omega + 1\ \text{M}\Omega} = 1.65\ \text{V}$$

Assuming tolerance for R1 and R2 is 5% and taking into account the ADA4505 offset:

$$V_{MID} = 1.65\ \text{V} \pm 82\ \text{mV}$$

To remove AC power supply interference and noise from resistors, set C1 so the cutoff frequency is at least less than the minimum V_{SIGNAL} frequency of 20 Hz.

Note that the capacitor value can be larger if it is needed to further bandlimit the noise.

$$20\ \text{Hz} < \frac{1}{2 \times \pi \times C1 \times \dfrac{R1R2}{R1 + R2}}$$

$$\frac{1}{20\ \text{Hz} \times 2\ \pi \times \dfrac{1\ \text{M}\Omega \times 1\ \text{M}\Omega}{1\ \text{M}\Omega + 1\ \text{M}\Omega}} < C1$$

$$15.9\ \text{nF} < C1$$

In this case, C1 is set to 22 nF, which provides a frequency of:

$$\frac{1}{22\ \text{nF} \times 2\ \pi \times \dfrac{1\ \text{M}\Omega \times 1\ \text{M}\Omega}{1\ \text{M}\Omega + 1\ \text{M}\Omega}} = 14.5\ \text{Hz}$$

2. Instrumentation amplifier (AD8237) gain value V_{SIGNAL}:

Consider that the range span of EM flow sensors output typically is a peak-to-peak signal amplitude going from ±75 µV to ±6 mV. For the circuit in Figure 1, the amplitude peak-to-peak signal amplitude range will be set to V_{SIGNAL} = 6 mV peak with a frequency of 30 Hz.

Then, consider the AD8237 output swing range limits to the supply rails. These values can be found in the data sheet from "Output Swing." Let's use the case R_L = 10 kΩ swing case at +25°C to be conservative:

$$0.05\ \text{V} < V_{OUT} < V_{DD} - 0.05\ \text{V}$$

For 3.3 V supply:

$$0.05\ \text{V} < V_{OUT} < 3.25\ \text{V}$$

Since the output is fully differential, the output will swing with respect to V_{MID} will be, worse case:

For positive input signals ($V_{MID_{MAX}}$ = 1.732 V):

$$1.732\ \text{V} \leq V_{OUT} \leq 3.25\ \text{V}$$

$$+SwingRange_{AD8237} = 3.25\ \text{V} - 1.732\ \text{V} = 1.518\ \text{V}$$

For negative input signals ($V_{MID_{MAX}}$ = 1.568 V):

$$0.05\ \text{V} \leq V_{OUT} \leq 1.568\ \text{V}$$

$$-SwingRange_{AD8237} = 1.568\ \text{V} - 0.5\ \text{V} = 1.518\ \text{V}$$

Now to set the gain, add up the total expected differential input signals and use the lower of the positive and negative swing ranges to set the max swing range:

$$Max\ Gain_{AD8237} = \frac{Max\ Swing\ Range_{AD8237}}{V_{SIGNAL}}$$

$$Max\ Gain_{AD8237} = \frac{1.518\ \text{V}}{6\ \text{mV}}$$

$$Max\ Gain_{AD8237} = 253\ \text{V/V}$$

Considering the output voltage range limits, the AD8237 gain should be less than 253. To leave some margin for DC errors/others, the gain value for the circuit in Figure 1 should be less than the maximum possible value. There is also a trade-off between the gain and the settling time: the higher the gain, the slower the time constant of the filter. Owing to those comments, the AD8237 gain is set to 101.

Note the benefit of design considerations, Step 1, in terms of maximization of the swing value.

From the data sheet, the associated formula for the gain is:

$$Gain = 1 + \frac{R_{G1}}{R_{F1}}$$

The AD8237 data sheet provides suggested resistor values for gain selection. For the selected gain of 101, the values of these resistors should be R_{F1} = 1 kΩ and R_{G1} = 100 kΩ.

3. In-amp (AD8237) bandwidth:

From the data sheet, the cutoff frequency value is

$$f_{3dB_{8237}} = \frac{GBW}{Gain}$$

$$f_{3dB_{8237}} = \frac{200\ \text{kHz}}{101\ \text{V/V}} = 1980\ \text{Hz}$$

If the design specification requires a certain minimum attenuation for the maximum signal frequency, this can be easily checked for a given filter cutoff frequency.

$$Attenuation = 20\ log_{10}\ \sqrt{\left(\frac{1}{1+\left(\frac{V_{SIGNAL\_max}{f0}\_freq^2}{f_{3dB_{8237}}{}^2}\right)}\right)}$$

$$Attenuation = 20\ log_{10}\ \sqrt{\left(\frac{1}{1+\left(\frac{220\ \text{Hz}^2}{1980\ \text{Hz}^2}\right)}\right)} = -0.05\ \text{dB}$$

4. Setting the high-pass filter cutoff frequency:

A high value high-pass filter cutoff frequency set by the integrator can get too close to the cutoff frequency of the low-pass filter set by the AD8237 bandwidth as explained in the design considerations section. This will introduce some gain error from the gain established previously.

Assuming ±5% tolerance for R3 and C3, the fastest time constant should be less than V_{SIGNAL} minimum frequency:

$$f_{3dB_{Integrator}} = \frac{Gain}{2\ \pi \times 0.95 \times R3 \times 0.95 \times C3} < 20\ \text{Hz}$$

The resistor R3 will have a constant value of 1 MΩ to minimize the current through this resistor into the op amp.

$$C3 > \frac{101\ \text{V/V}}{2\ \pi \times (0.9 \times 0.9 \times 1\ \text{M}\Omega \times 20\ \text{Hz})}$$

$$C3 > 0.99\ \mu\text{F}$$

Taking the nearest standard capacitor value to have approximately a cutoff frequency of 20 Hz, let's set C3 = 1.5 µF, so, the updated cutoff frequency is:

$$f_{3dB_{Integrator}} = \frac{101}{2\ \pi\ (1\ \text{M}\Omega \times 1.5\ \mu\text{F})} = 10.71\ \text{Hz}$$

If the design specification requires a certain minimum attenuation for the minimum signal frequency, this can be easily checked for a given filter cutoff frequency. See an example for this circuit:

$$Attenuation = 20\ log_{10}\ \sqrt{\left(\frac{1}{1+\left(\frac{f_{3dB_{Integrator}}{}^2}{V_{SIGNAL\_min}{f0}\_freq^2}\right)}\right)}$$

$$Attenuation = 20\ log_{10}\ \sqrt{\left(\frac{1}{1+\left(\frac{10.71^2\ \text{Hz}^2}{20^2\ \text{Hz}^2}\right)}\right)} = -1.09\ \text{dB}$$

5. Offset voltage:

Both signals V_{OFFSET} and V_{CM} have limitations.

As expected, the DC offset can be larger than what we can usually find in most applications. In this situation, the voltage value must be $V_{OFFSET} \leq \pm V_{MID}$. If the DC offset is greater than this limit, the V_{REF} voltage value goes outside the voltage supply range of the ADA4505. The equation linked to the reference pin is set to: $V_{REF} = V_{MID} - V_{OFFSET}$. The V_{OFFSET} will be set at 1 V.

As for the common-mode voltage, it is directly linked to the V_{OFFSET} value as V_{CM} must be in the range:

$$0 < V_{CM} \pm V_{OFFSET}/2 < V_{DD}$$

If those limitations are not verified, the input values of the AD8237 are either over or under the supply ranges. The V_{CM} will be set at 1.65 V.

Design Simulations

To check the common-mode input range vs. output voltage or diamond plot for an instrumentation amplifier, you'll want to provide the supply voltage $+V_{DD}$, reference voltage, gain, common-mode swing, and differential input swing. The instrumentation amplifier diamond plot tool from Analog Devices helps to see if the input swing is within the operating range of the part. Take note that the output swing used for the tool uses the worst-case load conditions (smallest resistive load), so if you design to the tool limits, there would be additional margin for larger resistive loads. Looking at the results in Figure 2, the purple outline is the usable range of the AD8237 for the given supply voltage, output swing, input common-mode range, and reference voltage of the part. The red outline shows how much of this range you are using for the given common-mode and differential input mode swing. The goal is to keep the red outline within the purple outline. If certain conditions violate this, the tool will show the error and provide recommendations. It is important to note that implementing the integrator circuit in the feedback loop is not possible in this interface. However, a workaround for this is to configure the diamond plot input signal as if the V_{OFFSET} and V_{CM} voltage of the circuit (in Figure 1) were added in. Hence, using the interval (0.65 V to 2.65 V) as the DC offset is removed and is not gained up. It also showcases that the common-mode voltage could be higher as there is still some room for the output to swing. To further understand what is happening inside the instrumentation amplifier, the **Internal Circuitry** tab will show the voltages of internal nodes.

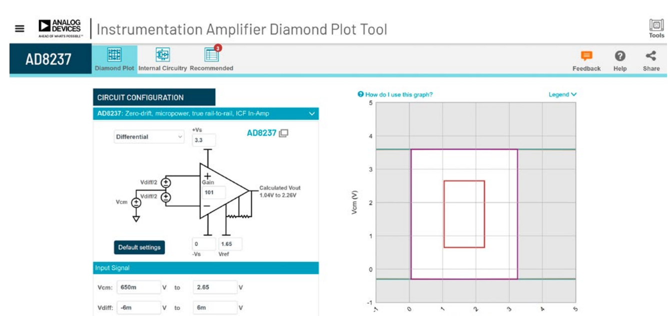

Figure 2. An AD8237 plot tool example.

LTspice® is an excellent simulation tool to check against the design procedure calculations made earlier including other specifications of interest such as the noise performance in the signal band of interest. The LTspice schematic is shown in Figure 3. The first simulation (Figure 4 and Figure 5) is a transient simulation with a DC offset of 1 V and an input signal of ±6 mV at 30 Hz. Figure 4 shows the signal at different stages in the circuit. Figure 5 is a zoomed in version of Figure 4 once the circuit has settled and the integrator capacitor is charged to the final value. The blue curve is the output of the integrator or reference voltage pin of the AD8237. The red curve is the V_{MID} value designed to $V_{DD}/2$ and the green curve is the final 30 Hz output signal gained, V_{OUT}.

Table 2 shows a comparison of the design goal vs. simulation results for the transient simulation. For the maximum and minimum V_{OUT} value, the expected values come from: $V_{OUT} = V_{MID} \pm V_{SIGNAL} \times 101$, which in our situation gives us the expected values equal to 2.256 V and 1.044 V. The V_{REF} value expected is equal to $V_{MID} - V_{OFFSET}$, which in our situation, gives us an expected value of 0.65 V. As for V_{MID}, we calculated it to be the mid-supply voltage, which is in our case, 1.65 V.

The results obtained in the transient analysis compared with the expectations are quite similar in terms of voltage output. However, 17 seconds are needed for the simulation to settle and for the output to get to its final value, due to the large integrator capacitor and the large DC offset implemented. This settling time comes from the fact that the simulation starts at time 0 s, and the capacitor needs time to charge to the final value.

Table 2. Design Goal vs. Simulation Transient Analysis

Parameter	Design Goal	Simulation
$V_{OUT_{MAX}}$	2.256 V	2.224 V
$V_{OUT_{MIN}}$	1.044 V	1.077 V
V_{MID}	1.65 V	1.65 V
V_{REF}	0.65 V	≈ 0.65 V

The next simulation in Figure 6 shows the frequency response of the circuit in Figure 3 with a DC offset of 1 V and an input signal of ±6 mV at 30 Hz. Cursors 1 and 2 from Figure 6 were placed at the –3 dB point for the high-pass and low-pass filters, respectively. Table 3 shows a comparison of design goals vs. simulation results.

Table 3. Design Goal vs. Simulation AC Analysis

Parameter	Design Goal	Simulation
High-Pass $f_{3dB_{ADA4505}}$	10.71 Hz	10.70 Hz
Low-Pass $f_{3dB_{8237}}$	1980 Hz	2138 Hz
20 Log (Gain)	40.08 dB	40.08 dB

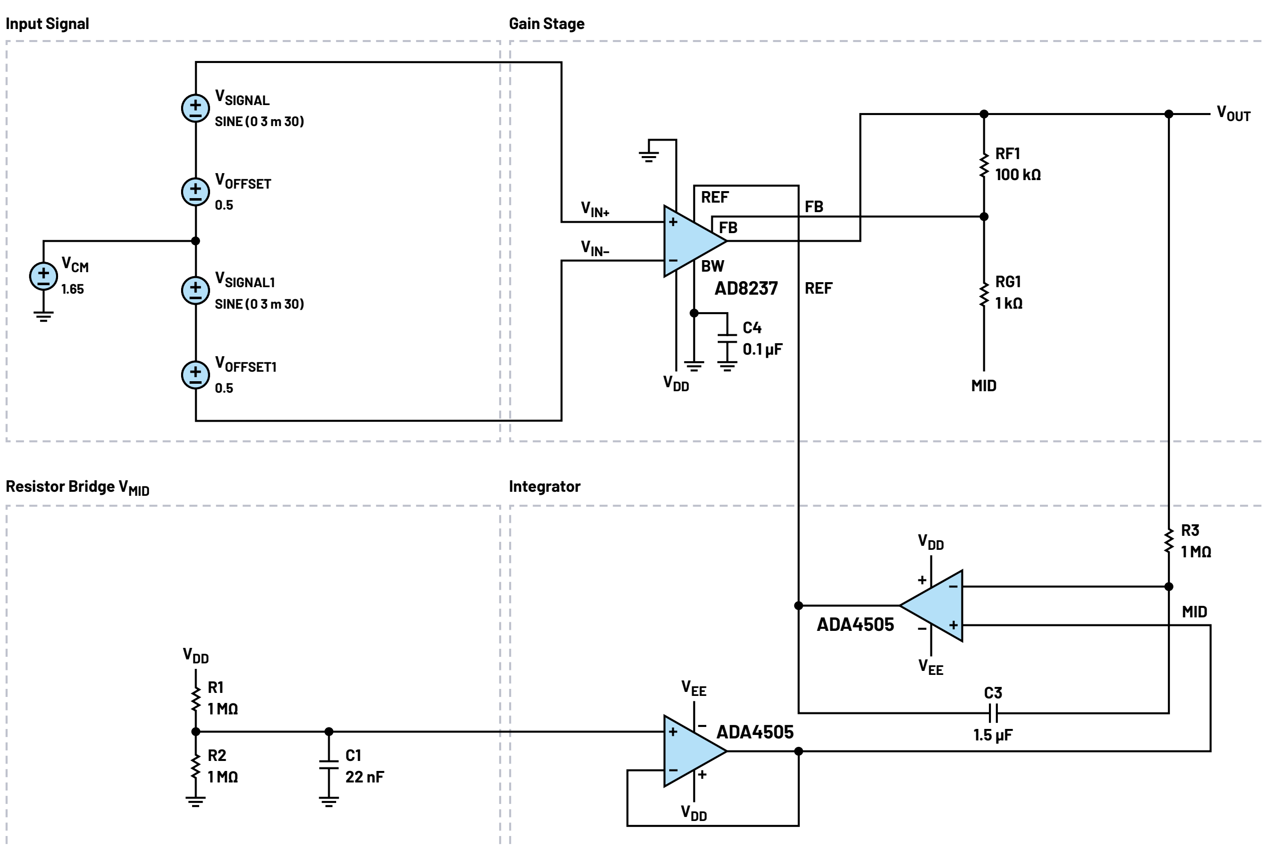

Figure 3. An LTspice schematic.

The next simulation in Figure 7 shows the voltage noise density vs. frequency RTI for the circuit in Figure 3. This is done by dividing the output noise by the total gain of the solution (101). For the band-pass filter function, we need to choose the integration frequency interval to compute total noise.

For the upper frequency, we will use the sensor maximum frequency value established earlier, which is 220 Hz. For the lower frequency, we will also use the sensor minimal frequency value established at 20 Hz. In this situation, the noise resulting will be from the integration from 20 Hz to 220 Hz.

The measured noise will actually be higher due to the band-pass filter cutoff frequencies. The LTspice simulation results assume a post processing brick wall filter to have a sharp roll-off at 20 Hz and 220 Hz.

The command line in LTspice is then set to be .noise V(V_{OUT}) V1 dec 100 20 220. Then hold the control key and left click on the waveform name (V(ONOISE)/101). The rms noise can easily be converted to peak-to-peak noise using the equation:

$$Noise\ \text{p-p} = 6.6 \times Noise\ \text{rms}$$

$$Noise\ \text{p-p} = 6.6 \times 1.3469\ \mu\text{V rms} = 8.88954\ \mu\text{V p-p}$$

A quick check of the AD8237 noise and ADA4505 noise determined that the AD8237 is the dominant noise source.

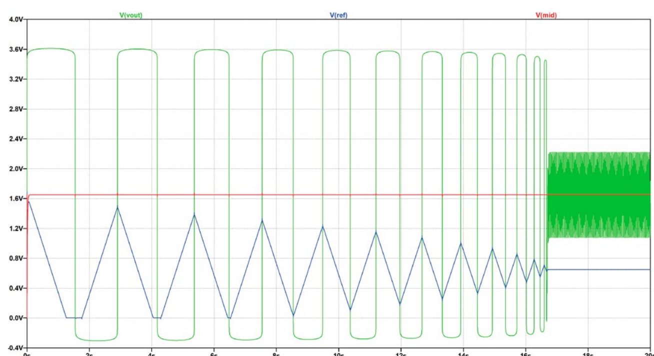

Figure 4. Transient simulation results.

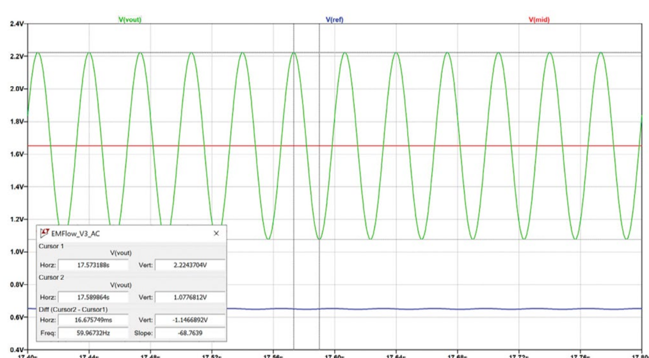

Figure 5. Transient simulation results zoomed in.

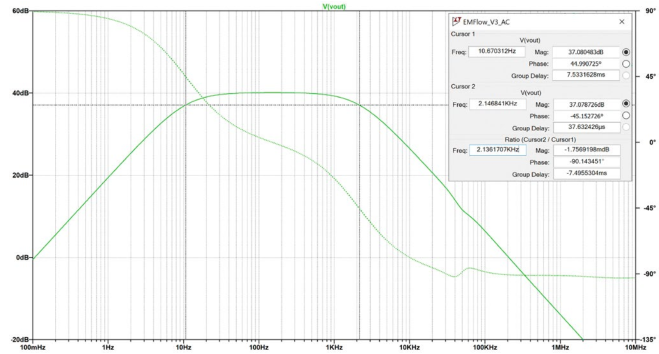

Figure 6. AC simulation results.

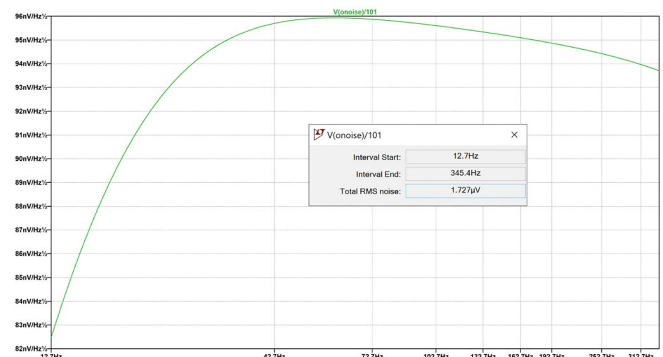

Figure 7. Total noise integrated over the equivalent noise bandwidth results.

Measured Results

To highlight the previous results, hardware testing is possible as both the AD8237 and ADA4505 offer test boards. The soldering of each component can be done from the test boards' schematics. When using both test boards at the same time, a trace on the AD8237 board may need to be cut to connect the V_{MID} voltage to the R_G resistors.

To ensure a better understanding, the values of components were set and taken from the design procedure section same as with the design simulation. To simulate the EM flow meters or biopotential measurement sensors, different measurement equipment was used such as a voltage calibrator and an arbitrary waveform generator.

For this test, the inputs signals were set with a DC offset, V_{OFFSET}, of 1 V, a common-mode voltage of 1.65 V, and an input signal, V_{SIGNAL}, of ±6 mV at 30 Hz.

Looking at the results shown in Figure 8, the output voltage V_{OUT} (yellow curve) performance has a small voltage off from the expected values but is still in line with expectations.

Table 4 shows a summary of design goals vs. measured results.

Table 4. Design Goals vs. Measured Results

Parameter	Design Goal	Measured
V_{OFFSET}	1 V	1.01 V
V_{SIGNAL}	6 mV peak	5.2 mV peak
$V_{OUT_{MIN}}$	1.044 V	1.13 V
$V_{OUT_{MAX}}$	2.256 V	2.19 V
V_{REF}	0.65 V	0.64 V

The differences in the design goal vs. simulation results can have different origins.

- The resistors used had a 5% error tolerance, meaning the V_{MID} value could have been shifted.
- The bench setup may have limitations that can result in minor deviations as shown by the measured simulations, V_{OFFSET} and V_{SIGNAL}.

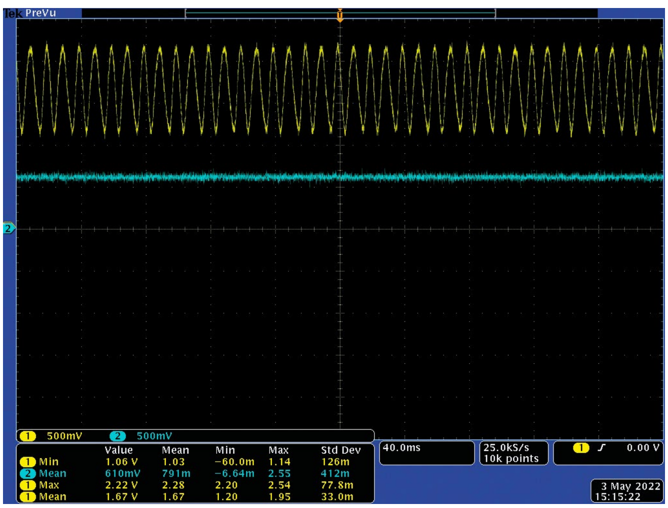

Figure 8. An oscilloscope screenshot with the yellow curve corresponding to V_{OUT} and the blue curve V_{REF}.

Design Devices

Table 5. In-Amp

Part Number	Package Size (MSOP)	I_{BIAS} (nA) Max	V_{OS} (µV) Max	Gain Min/ Max (kHz) typ	0.1 Hz to 10 Hz Noise (µV p-p) typ	V_{NOISE} (nV/√Hz) typ	I_Q/ Amp (µA) typ	+Vs Min/ Max (V)
AD8237	3.20 mm × 5.15 mm	1	75	1/1000	1.5	68	115	1.8/5.5

Table 6. Op Amp

Part Number	Package Size (WLCSP)	I_{BIAS} (pA) Max	V_{OS} (mV) Max	GBP (kHz) typ	0.1 Hz to 10 Hz Noise (µV p-p) typ	V_{NOISE} (nV/√Hz) typ	I_Q/ Amp (µA) typ	+Vs Span Min/ Max (V)
ADA4505	1.42 mm × 1.42 mm	2	3	50	2.95	65	7	1.8/5

Conclusion

A common requirement when capturing signals from sensors such as EM flow in field transmitters or electrodes in biopotential applications, the signal of interest, is usually sitting on much larger DC offsets. To make it easier to extract the relevant information from these sensors, one solution is to implement an AC-coupled measurement signal chain. The aim is to remove the DC offsets while amplifying the AC signals. The instrumentation amplifier AD8237 provides the gain and the AC is coupled all in one stage by incorporating an integrator circuit in the feedback loop. By removing the DC offset at the input stage, this circuit allows maximum signal gain to be applied at the very input of the measurement signal chain, which minimizes the input referred noise of the overall measurement solution.

References

LTspice

LTspice is a high performance SPICE III simulator, schematic capture, and waveform viewer with enhancements and models for easing the simulation of switching regulator, linear, and signal chain circuits.

Instrumentation Amplifier Diamond Plot Tool

The diamond plot tool is a web application that generates a configuration-specific output voltage range vs. input common-mode voltage graph, also known as the diamond plot, for ADI instrumentation amplifiers.

Appendix

In Figure 9 and Figure 10, the indirect current-mode instrumentation amplifier and the three op amp instrumentation are displayed. The indirect current-mode instrumentation amplifier allows more gain than instrumentation amplifier solutions composed of two or three op amps, which cancel the offset after gain has been applied. For the proposed architecture, the offset correction happens prior to the gain phase, which allows the in-amp to have a large gain. Here is a description of both architectures.

For Figure 9, the indirect current-mode instrumentation amplifier is based on a one-stage configuration. The input voltages are applied to the first G_{M1} cell, while the G_{M2} cell is in the feedback loop. The internal integrator Amplifier A forces a replica of V_{IN1} at V_{IN2}. The integrator is used to drive the reference pin that is prior to the gain. The gain is set by the external resistors RFB and RG and equal to:

$$1 + \frac{R_{FB}}{R_G}$$

The three op amps architecture in Figure 10 is based on a two-stage configuration. The first two op amps U1 and U2, R_{GAIN} resistor, R2 resistors, and R1 resistors form noninverting amplifiers and are considered as the input stage. It provides unity common-mode gain and the differential gain is set by the resistor R_{GAIN} and equal to:

$$1 + \frac{2 \times R1}{R_{GAIN}}$$

The last op amp, U3, and the R3 resistors form a differential amplifier that forms the output stage of the instrumentation amplifier. It provides unity differential-mode gain and common-mode rejection. The injection point of the reference for this architecture is at the second stage after the first gain stage has been applied.

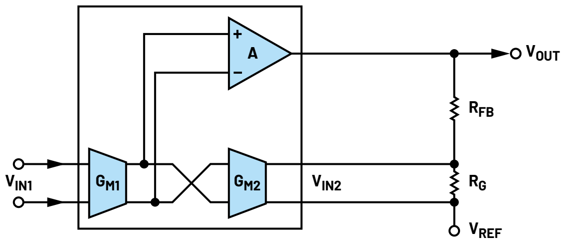

Figure 9. Indirect current-mode instrumentation amplifier architecture of the AD8237.

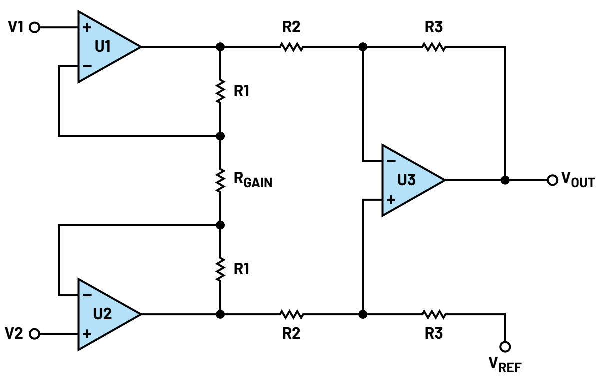

Figure 10. Three op amp instrumentation amplifiers.

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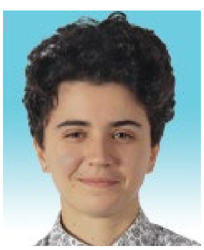
Aine McCarthy, Lead Systems Applications Engineer, Automotive Group

Tim Green, Senior Analog Applications Engineer, Scientific Instruments (SCI) Group



About the Author

Marie-Eve Carre holds a master's degree in electronics engineering from CPE Lyon, School of Engineering in Lyon, France. Marie-Eve first joined Analog Devices in 2020 as an applications engineering co-op before returning to France to finish her master's degree. She returned to ADI in 2022 and is currently supporting the Precision Signal Chain Application Group with a focus on low power signal chains.