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RAQ Issue 224: Parasitic Oscillation in Hot Swaps

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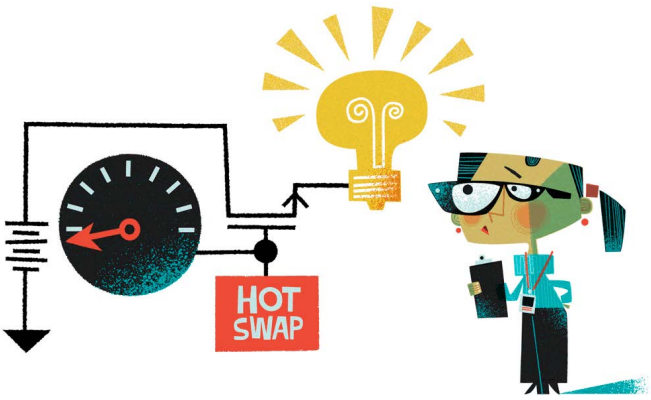
Question

I used a 10 Ω gate resistor in my schematic like the data sheet says, but still see ringing during start-up. Why is my hot swap circuit oscillating?



Answer

Hot swap parts that use high-side, N-channel MOSFET switches can oscillate during startup and current limit. While this is not a new issue, data sheets often lack detailed information on the solution. Simply adding a small gate resistor as an easy fix without understanding the underlying principles can result in a layout prone to oscillation. This article aims to explain the theory of parasitic oscillation and provide guidance on correctly implementing the solution.

Introduction

Hot swap, surge stopper, eFuse, and ideal diode controllers that use high-side N-channel MOSFETs (NFETs) can suffer from oscillation during startup and voltage/current regulation. Data sheets typically mention this issue briefly, along with the recommended fix of adding a small gate resistor. However, without a clear understanding of the root cause of oscillations, designers may position the gate resistor poorly in the layout, making the circuit susceptible to oscillation. This article will discuss the theory behind parasitic oscillation and may prevent a board revision.

Initially, adding gate resistance may seem redundant, as the resistance looking into the NFET's gate is infinite. Users may omit the part with no consequence and question whether the gate resistor was necessary. However, the 10 Ω gate resistor serves as a preventative measure to suppress ringing on the gate node. The gate node possesses the components of a tank circuit, starting from the gate trace itself. A long PCB trace introduces parasitic inductance and distributed capacitance to a nearby ground plane, creating a high frequency path to the ground. Power FETs that are optimized for high safe operating area (SOA) have nanofarads of gate capacitance, which is further exacerbated when additional FETs are connected in parallel for increased current handling. Zener diodes used to clamp a FET's V_{GS} also contribute parasitic capacitance (although C_{ISS} from a power FET dominates).

Figure 1 shows a generic PowerPath™ controller with parasitics drawn in.

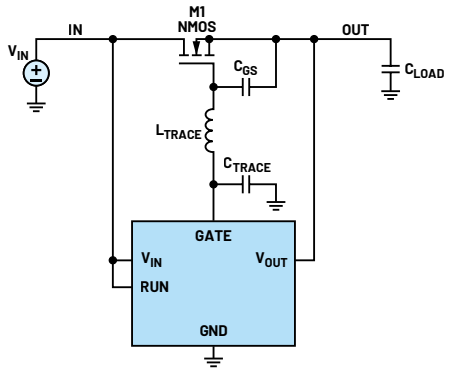


Figure 1. A generic PowerPath controller.

When the circuit is rotated (see Figure 2), its resemblance to a Colpitts oscillator becomes evident (see Figure 3). It's a tank circuit with added gain, capable of generating sustained oscillations. This configuration is found in PowerPath controllers that utilize N-channel FETs.

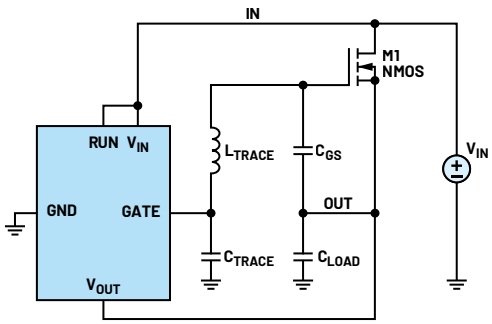


Figure 2. A rotated PowerPath controller.

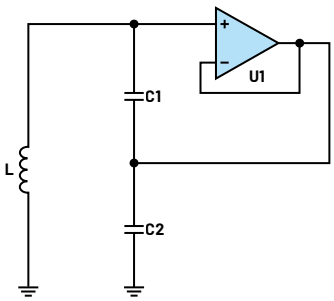


Figure 3. A Colpitts oscillator.

A Colpitts oscillator uses a buffer to provide positive feedback through a capacitive divider. In the PowerPath controller, this is realized by the FET. Since it is in a common-drain/source-follower configuration, it will act as an AC buffer with improved performance at higher drain currents. The signal at the top of the capacitive divider is injected into the middle of the divider, causing the signal at the top of the divider to rise (and the process repeats).

Oscillations may occur in scenarios where the FET is not fully enhanced:

1. During initial startup, when the gate voltage ramps up and the output capacitor is charged.

2. When current is being regulated (if the controller uses active current limiting).

3. When voltage is being regulated (as seen in surge stoppers).

To validate the concept of the switch FET being in a Colpitts oscillator topology, a basic circuit was constructed without a gate driver IC (see Figure 5). The FET's C_{GS} (not shown as a discrete component in Figure 4) and C2 form the divider.

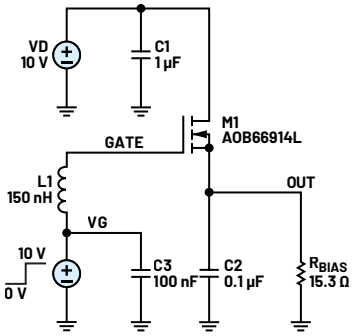


Figure 4. Test circuit of NFET as a Colpitts oscillator.

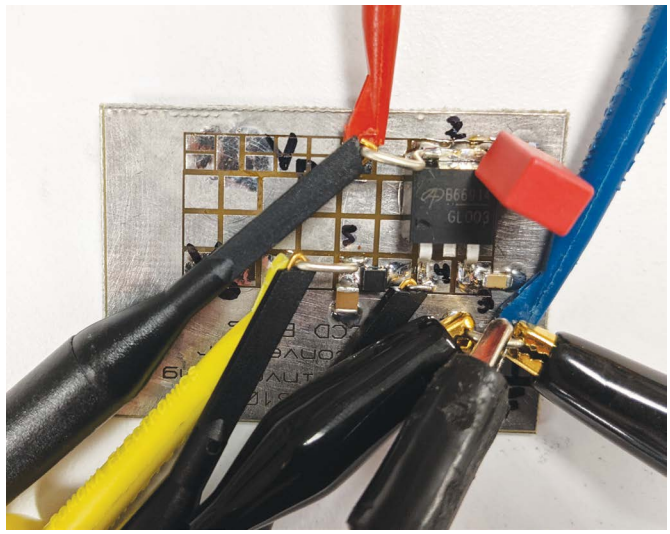
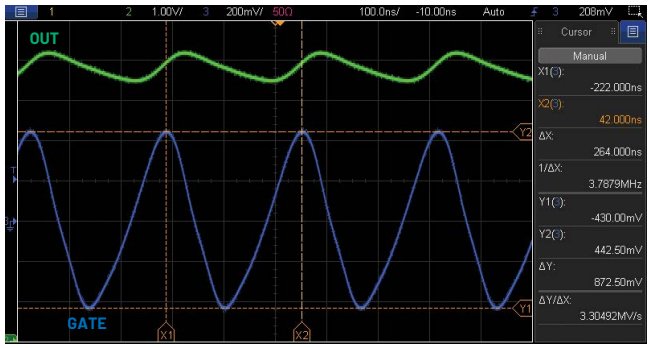


Figure 5. Prototype of a circuit.



P2: OUT (1 V/Div, DC-Coupled)
P3: GATE (200 mV/Div, AC-Coupled)

Figure 6. Scope capture showing oscillations when applying DC.

Oscillation is observed in Figure 6, which supports that a high-side, NFET switch is in a Colpitts topology.

Now let's move to a hot swap controller and see if it can be modified to induce oscillations. A demo board is used to start into a capacitive load. During startup, the gate voltage ramps up with a set dV/dt, which the output follows. From the equation, $I_{INRUSH} = C_{LOAD} \times dV/dt$, the inrush current into the output capacitor is controlled by dV/dt. To increase the FET's transconductance (g_m), the inrush is set to a relatively high value of 3 A.

Test setup (see Figure 7):

- UV and OV functions are disabled.
- C_{TRACE} represents the trace capacitance and is a discrete 10 nF ceramic capacitor.
- L_{TRACE} is a discrete 150 nH inductor placed between the LT4260's GATE pin and the NFET's gate, representing trace inductance.
- A 2 mΩ sense resistor will limit the foldback current limit to 10A.
- A 68 nF gate capacitor extends startup time to tens of milliseconds, during which the FET is susceptible to oscillations.
- An output capacitance of 15 mF will draw amps of inrush during startup, increasing the FET's g_m.
- A 12 Ω load provides additional current for the FET's g_m.

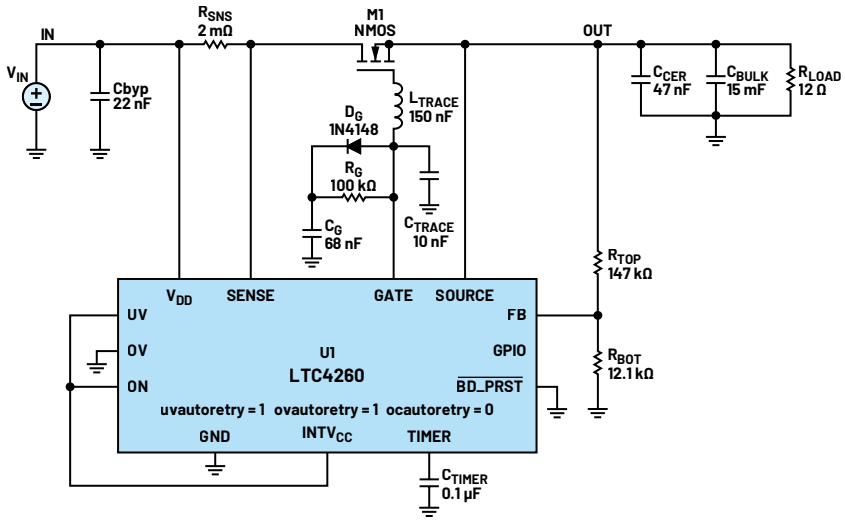


Figure 7. Simplified test circuit.

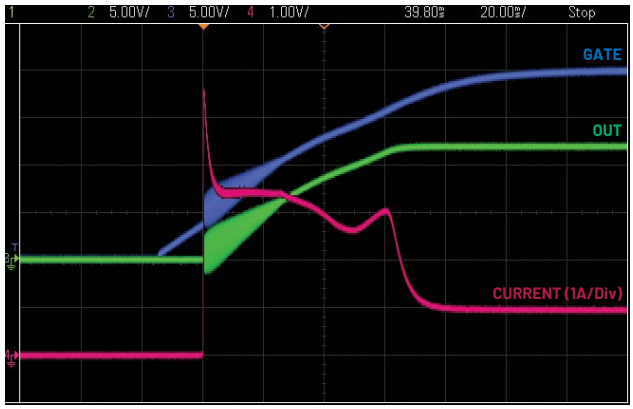


Figure 8. Scope capture of decaying oscillations during startup.

Looking at the waveforms in Figure 8, once the gate voltage ramps up to the FET's threshold voltage, the GATE and OUT waveforms exhibit ringing. This ringing is caused by the sudden step in the GATE waveform, resulting in an overshoot in the inrush current. The ringing eventually subsides.

To push the transient ring into continuous oscillation, the gain of the FET must be increased. By raising the V_{IN} from 12 V to 18 V, both the load current and g_m increase. This amplifies the positive feedback enough to maintain oscillation, as depicted in the scope capture shown in Figure 9.

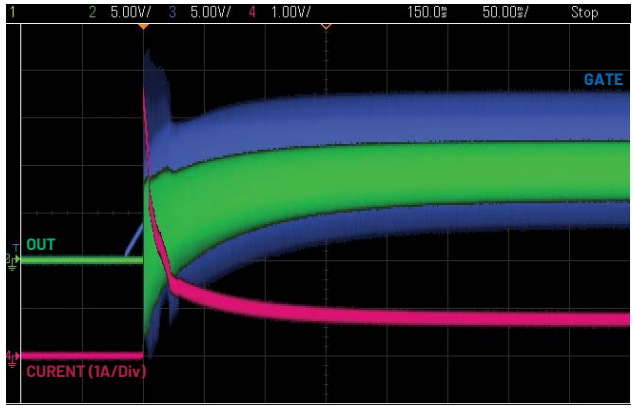


Figure 9. Scope capture of continuous oscillations from increasing V_{IN}.

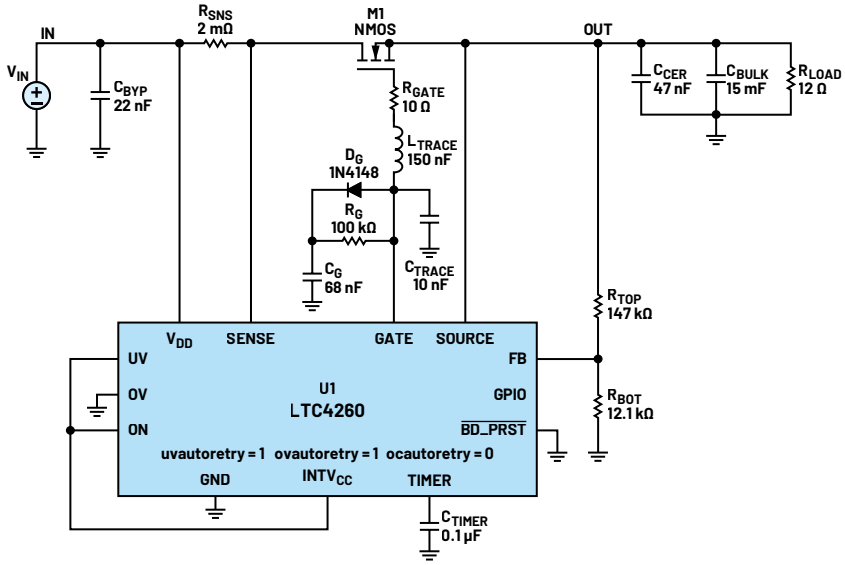


Figure 10. Demo board test circuit with gate resistor added.

Now that the issue has been replicated, let's implement the well-known fix: a 10 Ω gate resistor is placed in series with the inductor (see Figure 10). This addition effectively halts the oscillations, resulting in a clean startup (see Figure 11).

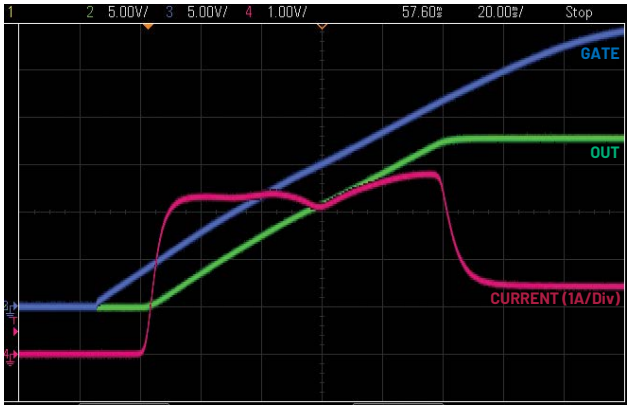


Figure 11. Scope capture of oscillation-free startup after adding a gate resistor.

Returning to the basic NFET Colpitts oscillator, the damping effect of R_{GATE} can be observed by introducing a switchable gate resistor (see Figure 12). When stepped from 0 Ω to 10 Ω, the oscillations are damped, as shown in Figure 13.

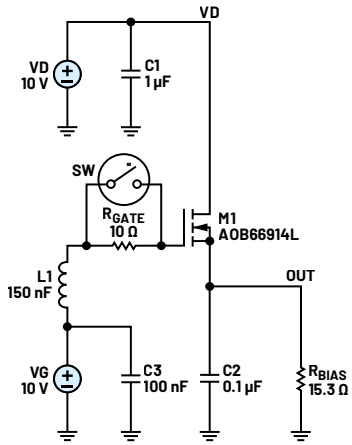
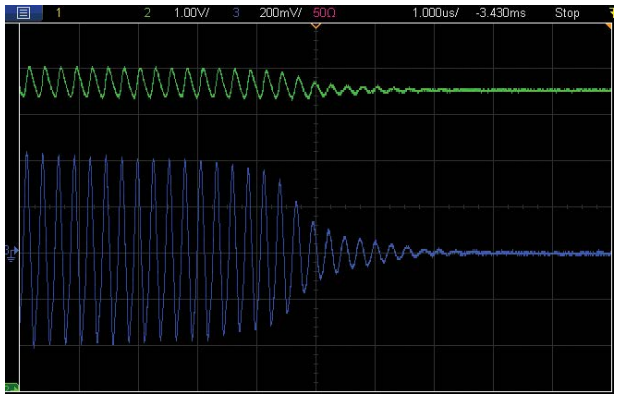


Figure 12. Basic NFET Colpitts oscillator, with switchable R_{GATE} added.



P2: OUT (1 V/Div, DC-Coupled)
P3: GATE (200 mV/Div, AC-Coupled)

Figure 13. Scope capture showing oscillations die off as R_{GATE} is stepped.

Conclusion

This article has covered the theory of parasitic FET oscillation, validated the Colpitts model through experimentation on the bench, replicated the issue on a demo board, and resolved the issue with the well-known solution. Placing a 10 Ω gate resistor as close as possible to the FET's gate pin separates the parasitic inductance of the PCB trace from the input capacitance of the FET. This eliminates the potential for gate ringing or oscillations and can spare the user hours of troubleshooting and a board respin, all at the cost of a single surface-mount resistor.

About the Author

Aaron Shapiro joined Analog Devices in 2019, working on hot swap products. He earned his B.S.E.E. degree from California State University Sacramento, focusing on analog electronics.