RAQ's

Rarely Asked Questions

Strange stories from the call logs of Analog Devices

Oversampling and Undersampling

Q. Why do many modern ADCs have a signal bandwidth much greater than their maximum sampling frequency? Doesn't sampling theory require the signal frequency to be limited to half the sampling frequency? Wouldn't it save power if their input stages had less bandwidth?

A. This has indeed become a common feature in sampling ADCs designed in the last decade or so. The increased bandwidth rarely has much effect on an ADC's power consumption, though, as its input stage usually consists of switched capacitor sampling circuitry. In ADCs that have input buffers, the power consumption of these amplifiers will be roughly proportional to their bandwidth, but as modern amplifier processes continue to evolve, each successive generation delivers more bandwidth for less power.

Sampling Theory[1] states that if a complex signal (made up of components at several different frequencies) is sampled with a sampling clock frequency of less than twice the maximum frequency present in the signal, a phenomenon known as *aliasing* will occur. Sampling with a clock frequency low enough to cause aliasing is known as *undersampling*.

In the early days of sampled data systems the input signal was almost always a baseband signal, with a frequency ranging from dc (or near dc if it was ac coupled) to a cut-off frequency which was usually defined by a low-pass filter (LPF). In such systems aliasing can prevent proper operation and may be a serious problem.

But if the total bandwidth of the signal is less than half the sampling frequency, then aliasing is not a problem—provided the relationship between the sampling frequency and the range of signal frequencies is correctly defined. Today many sampled data systems work with signals of high frequency, but relatively narrow bandwidth (for example the intermediate frequencies (IFs) of digital radios), and lower frequency clocks. The ADCs for these systems must have wide signal bandwidths but do not need high maximum clock frequencies.

As we saw in an earlier RAQ[2] it is possible to improve the resolution of a sampled data system by increasing the sampling clock rate—the procedure is known as *oversampling*. If the signal bandwidth is small, even though the signal frequency is high, we can build a high-performance system using the ADCs you describe in your question and a clock frequency much higher than the signal bandwidth but much lower than the signal's center frequency. Such a system is simultaneously undersampling and oversampling, unlikely though this may seem at first sight.

[1]Often called the Nyquist, or Nyquist-Shannon, Sampling Theory after Harry Nyquist and Claude Shannon who were among the first to develop its theoretical basis.
[2]RAQ 13 - "It may be Greek to you, but sigma delta converters are not really hard to understand."

To Learn More About Sampling ADCs
http://dn.hotims.com/27763-101

Contributing Writer James Bryant has been a European Applications Manager with Analog Devices since 1982. He holds a degree in Physics and Philosophy from the University of Leeds. He is also C.Eng., Eur. Eng., MIEE, and an FBIS. In addition to his passion for engineering, James is a radio ham and holds the call sign G4CLF.

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