

Input Magic—Differential Signals Allow Input Swing to Exceed Supply Voltage

Q: My ADC has a 1.8-V power supply. How can it have a 2-V p-p input range?



A: The latest generation of low-power, high-speed ADCs—manufactured on fine-line silicon processes—run on low-voltage supplies. ADC designers face a tradeoff between making the input range bigger to get better signal-to-noise ratio (larger signals provide higher SNR), and making the input range smaller to ease the drive requirements. Over the years we've seen ADCs with 5-V supplies and 4-V p-p input ranges, and 3-V supplies with 2-V p-p input ranges, but these didn't raise any eyebrows. Over the past few years, however, we've seen a host of ADCs with 1.8-V supplies and 2-V p-p input ranges. These raise some seemingly reasonable questions: How can the ADC have a 2-V p-p input voltage range while running on 1.8-V supplies? Doesn't this require the signal to exceed the supply rails?

The overlooked detail, of course, is that the analog input signal to most high-speed ADCs is differential. Transmitted as complementary single-ended signal pairs on the V_{IN+} and V_{IN-} pins, the differential input signal $V_{INDIFF} = V_{IN+} - V_{IN-}$. The single-ended components, centered within the supply rails, swing only half the amplitude of the differential signal, with a typical common-mode voltage of $V_{SUPPLY}/2$.

Differential signals are advantageous because they provide good common-mode rejection and inherent cancellation of even-order distortion (This is only true if you have perfect amplitude and phase matching, but that's another story.). An often overlooked advantage of differential signals, however, is that the amplitude of a differential signal can have twice the amplitude as a single-ended signal within a given supply range. As ADC designs move to even lower supply voltages, the headroom for the input signal will continue to be squeezed, and the differential signal will occupy more of the available supply range. In dc-coupled applications, the common-mode voltage of these low-voltage ADCs presents an interface challenge to the drive amplifiers, but for many applications the signal can be ac-coupled to the ADC, so this will not be an issue.

References

Analog Dialogue

Ardizzoni, John and Jonathan Pearson, [“Rules of the Road” for High-Speed Differential ADC Drivers](#), Analog Dialogue, Volume 43, Number 2, 2009

Application Notes

[AN-1026: High Speed Differential ADC Driver Design Considerations](#)

RAQs

[Driving Miss ADC](#)

Technical Documentation

[Using Op Amps with Data Converters](#)

[Interfacing to Data Converters](#)

Tutorials

[MT-075: Differential Drivers for High Speed ADCs Overview](#)

[MT-074: Differential Drivers for Precision ADCs](#)

Webcasts

[The Latest on Driving ADCs Differentially: Part 2](#)

[The Latest on Driving ADCs Differentially: Part 1](#)

