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AnalogDialogue

StudentZone—ADALM2000 Activity: Digital-to-Analog Conversion

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R-2R Resistor Ladder Digital-to-Analog Converter (DAC)

Objective

The objective of this exercise is to explore the concepts of digital-to-analog conversion making use of the CMOS inverter as reference switches for a resistor ladder divider (used in DAC).

Background

We will explore the simple CMOS inverter logic gate as a pair of switches. The digital I/O signals of the ADALM2000 module can be configured as standard CMOS dividers with a 3.3 V supply (push-pull mode). In the simplest form, a CMOS output consists of one PMOS device, M1, and one NMOS device, M2. Generally, the CMOS fabrication process is designed such that the threshold voltage, V_{TH}, of the NMOS and PMOS devices is roughly equal—that is, complementary. The designer of the inverter then adjusts the width-to-length ratio, W/L, of the NMOS and PMOS devices such that their respective transconductance, and thus their R_{ON}, is also equal. Only one of the two transistors is ever on at the same time, connecting the output to either V_{DD} or V_{SS}. We can consider these two voltages to be the reference for the DAC.

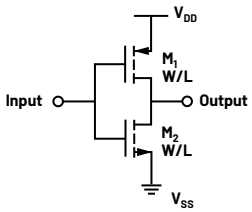


Figure 1. CMOS output driver.

When used in what is referred to as "voltage mode," the legs of the R-2R resistor ladder, shown in Figure 2, are alternately driven to one of the two reference voltage levels based on the digital code (D0-7). Digital 0 is for V_{REF}– and Digital 1 is for V_{REF}+. Depending on the digital input code V_{LADDER} (in Figure 2) will be some fraction of the difference between the two reference levels. The negative of the two reference voltages (V_{REF}–) is often ground (V_{SS}). The positive reference voltage (V_{REF}+) in our case here will be the positive supply (V_{DD}) for the CMOS driver.

Materials

- ADALM2000 Active Learning Module
- Solderless breadboard
- Jumper wires
- Nine 20 kΩ resistors
- Nine 10 kΩ resistors
- One OP27 amplifier

Directions

Build the 8-bit resistor ladder circuit shown in Figure 2, preferably on your solderless breadboard. The number of resistors normally supplied in the Analog Parts Kit (ADALP2000) is not sufficient to build the full 8-bit ladder. It is best to use 1% resistors for this project if you have access to them.

Connect the eight digital outputs designated by the blue boxes, and the scope channel and AWG output designated by the green boxes to the resistor ladder circuit as shown. Remember to connect power to the op amp supply pins.

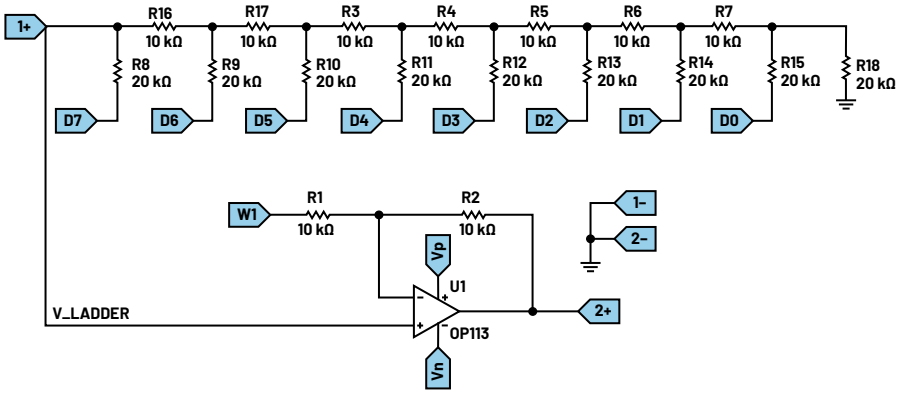


Figure 2. R-2R resistor ladder circuit.

Hardware Setup

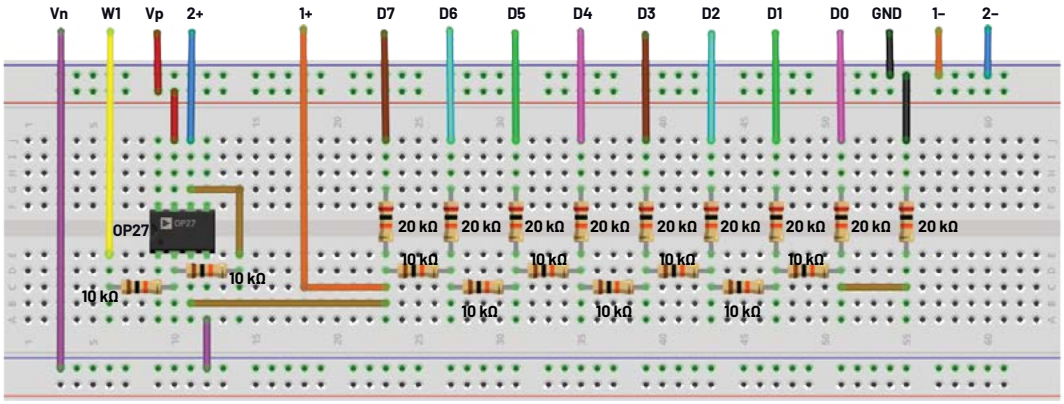


Figure 3. R-2R resistor ladder circuit breadboard connections.

Procedure

With both R1 and R2 installed, set AWG1 to a DC voltage equal to the V_{REF}+ of the DAC, which will be the 3.3 V supply voltage of the CMOS digital outputs. This will produce a bipolar output voltage that will swing from –3.3 V to +3.3 V. Disconnect AWG1 and remove resistor R1 for a unipolar output voltage that will swing from 0 V to 3.3 V. Start the Scopy software. Open the **Pattern Generator** screen. Select and group DIO0 to DIO7. Now edit the parameters. Set the pattern to **Binary Counter.** The output should be PP (for push-pull). Set the frequency for 256 kHz. You should see something that looks like the screen shown in Figure 4. Lastly, hit the **Run** button.

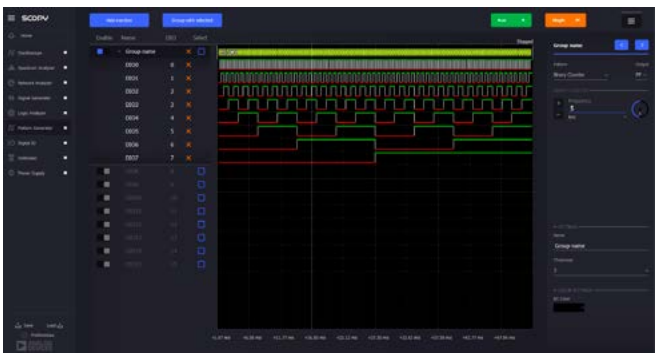


Figure 4. The Pattern Generator screen.

Open the **Scope** screen, turn Channel 2 on, and set the time base for 200 µs/div. Be sure to hit the green **Run** button. You may also need to adjust the vertical range for the channel (1 V/div is a good starting point). You should see, as shown in Figure 4, the voltage ramp up from 0 V to 3.3 V. The period of the ramp should be 1 ms.

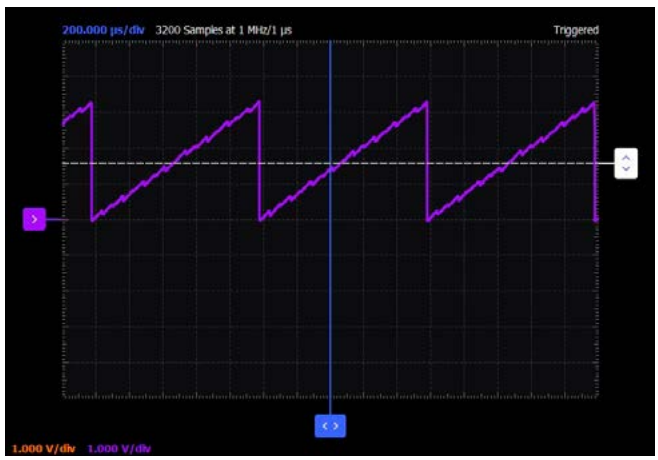


Figure 5. The Scope screen.

Change the digital pattern. Try the **Random** pattern and open the FFT window on the scope. You can also load custom patterns by making a plain text .csv file with a column of numbers ranging from 0 to 255 (for the 8-bit wide bus). Load your custom pattern and see what happens.

Here are some premade waveform files you can try: sine, triangle, Gaussian pulse, etc.: waveforms_pg.

AD5626 12-Bit *nano*DAC

Background

The AD5626 is a voltage output DAC that can operate from a single 5 V supply. It contains the DAC, input shift registers and latches, reference, and a rail to-rail output amplifier that can swing to either rail and is set to a range of 0 V to 4.095 V for a 1 mV per-bit resolution. This part features a serial interface that is high speed, 3-wire, and DSP compatible with data in (SDIN), clock (SCLK), and load strobe ($\overline{\text{LDAC}}$). There is also a chip-select pin for connecting multiple DACs. The CLR input sets the output to zero scale at power-on or upon user demand.

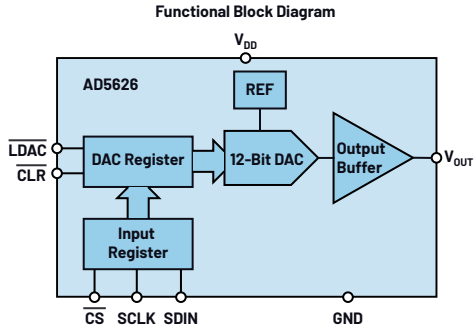


Figure 6. A functional block diagram of the AD5626.

The AD5626 has a separate serial input register from the 1-bit DAC register, and it allows preloading of a new data value into the serial register without disturbing the present DAC output voltage. The loaded value can be transferred to the DAC register by strobing the LDAC pin.

Unipolar Output Operation

This mode of operation is the basic mode for the AD5626. You can verify the good functionality of the AD5626 according to the unipolar code table of the DAC.

Table 1. Unipolar Code Table of the AD5626

Hexadecimal Number in DAC Register	Decimal Number in DAC Register	Analog Output Voltage (V)
FFF	4095	4.095
801	2049	2.049
800	2048	2.048
7FF	2047	2.047
000	0	0

Materials

- ADALM2000 Active Learning Module
- Solderless breadboard
- Jumper wires
- One AD5626 12-bit *nano*DAC®
- One 2.2 kΩ resistor
- One 0.001 µF capacitor
- One 0.1 µF capacitor
- One 10 µF capacitor

Hardware Setup

Connect the pins of the AD5626 as shown in Figure 7.

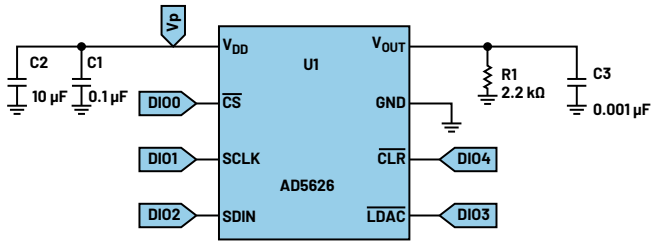


Figure 7. Connections for unipolar operation of the AD5626.

Procedure

Open Scopy and enable the positive power supply to 5 V. In the **Pattern Generator**, you should configure the DAC input signals according to the timing diagram of the AD5626 presented in the data sheet. Start by configuring SPI signals. Create a group channel with DIO0, DIO1, and DIO2. If the connections were done as shown in Figure 7, then DIO1 is the clock signal, DIO2 is the data signal, and DIO0 is the $\overline{\text{CS}}$ signal. Make sure that the digital channels are in the right order when grouped as SPI (see Figure 10). It is specified in the data sheet that the clock width for both high and low states should be at least 30 ns. From this, you can compute the clock period and therefore maximum frequency. Set the clock frequency to 1 MHz. Set **CLK Polarity** and **CLK Phase** to 1.

As the AD5626 is a 12-bit DAC, the data sent through SPI should be at least 12 bits long. Set the number of bytes per frame to 2, and it will send 16 bits when the conversion is initiated. In the **Data** textbox, you can enter the value to be sent to the DAC. The signals of the SPI group channel should resemble the timing diagram of the AD5626 DAC.

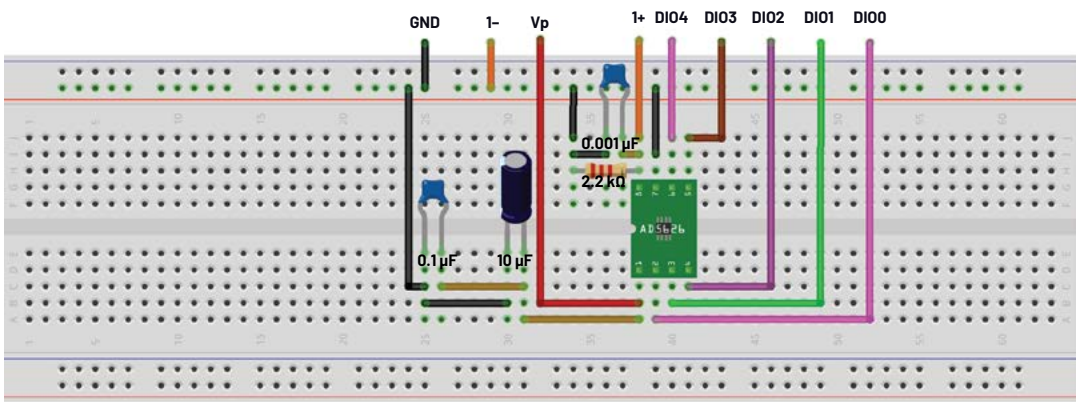


Figure 8. AD5626 breadboard connections.

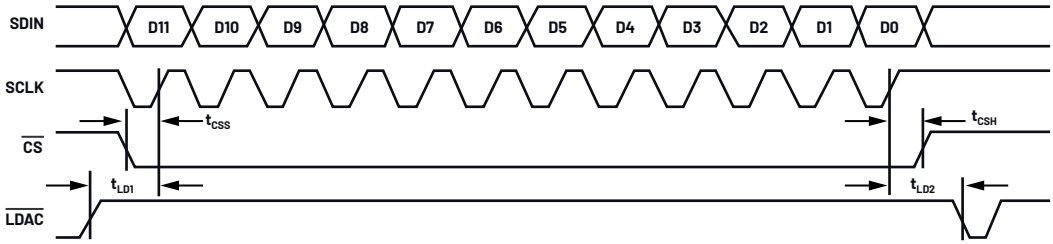


Figure 9. AD5626 SPI timing diagram.

Now you should configure /LDAC and /CLR signals. From the data sheet, we know that the shift register contents are updated on the rising edge of /LDAC if /CLR is high. Set the pattern of DIO4 (/CLR) as "Number" and enter the value 1. The /LDAC signal (DIO3) should have a rising edge before $\overline{CS}$ falling edge and should be high, as long as bits are transmitted serially. In order to fulfill the previously stated conditions, the DIO3 signal can be set at 13 kHz frequency and 160° phase. All the input signals needed for AD5626 digital-to-analog conversion are presented in Figure 9.

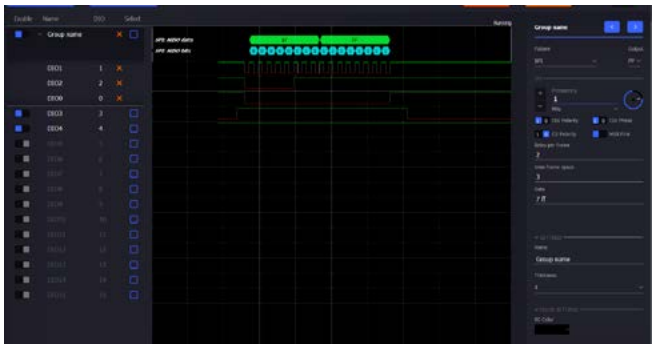


Figure 10. Pattern Generator signals setup.

The last step is to open **Oscilloscope** in Scopy and connect Channel 1 to the output of the AD5626. Enable Channel 1 measurements and enter a value in the "Data" area of SPI. In Figure 11 you can see the output voltage if the data sent through SPI is 7FF.

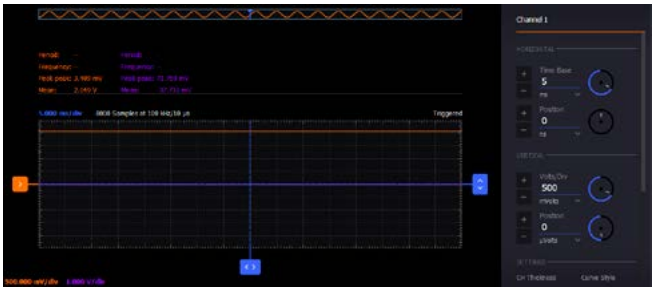
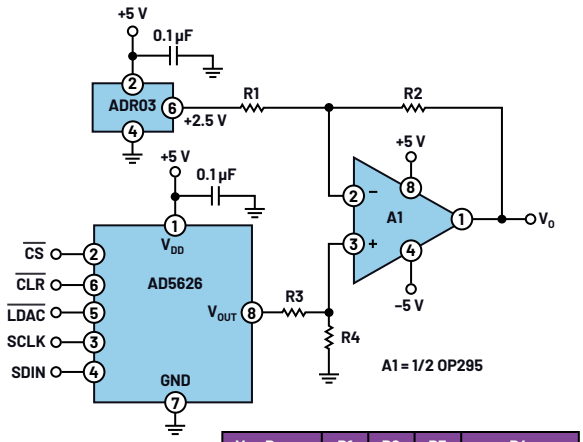


Figure 11. AD5626 output voltage for 7FF input.

Bipolar Output Operation

Although the AD5626 has been designed for single-supply operation, bipolar operation is achievable using the circuit illustrated in Figure 12.



V_{OUT} Range	R1	R2	R3	R4
±2.5 V	10 kΩ	10 kΩ	10 kΩ	15 kΩ + 274 Ω
±5 V	10 kΩ	20 kΩ	10 kΩ	43.2 kΩ + 499 Ω

Figure 12. Bipolar output operation without trim (circuit suggested in the data sheet).

This circuit can be used for applications that do not require high accuracy. The output voltage is coded in offset binary and is given by:

$$V_O = 1\ \text{mV} \times Digital\ Code \times \left(\frac{R4}{(R3 + R4)}\right)$$

$$\times \left(1 + \frac{R2}{R1}\right) - 2.5 \times \left(\frac{R2}{R1}\right)$$

For the ±5 V output range and the circuit values shown in the table in Figure 12, the transfer equation becomes:

$$V_O = 2.44\ \text{mV} \times Digital\ Code - 5\ \text{V}$$

Materials

- ADALM2000 Active Learning Module
- Solderless breadboard
- Jumper wires
- One AD5626 12-bit *nano*DAC
- One OP484 operational amplifier
- One 0.1 µF capacitor
- One 1 kΩ resistor
- One 20 kΩ resistor
- Two 10 kΩ resistors
- One 47 kΩ resistor
- One 470 kΩ resistor

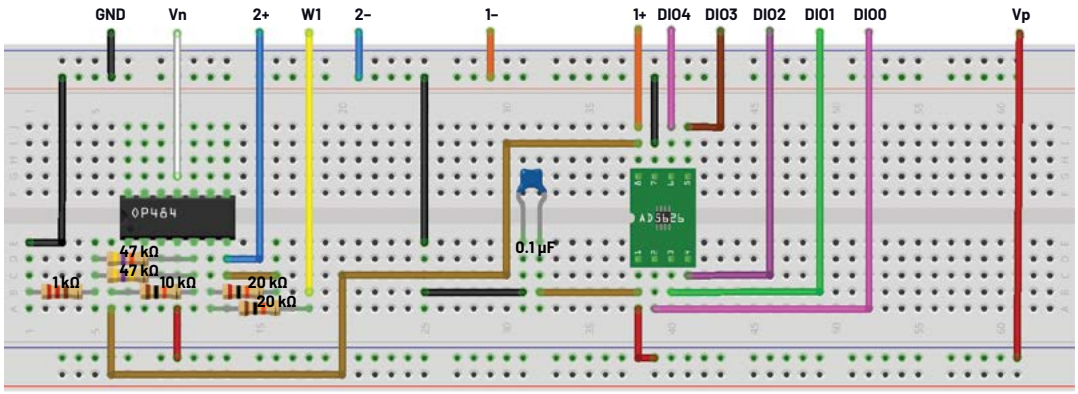


Figure 13. AD5626 bipolar output operation breadboard connections.

Hardware Setup

Build the circuit presented in Figure 12 on your solderless breadboard.

Procedure

You can configure the DAC for unipolar output operation as described in Figure 7. For the voltage reference, use Channel 1 of the **Signal Generator** set for constant 2.5 V. On the second channel of the oscilloscope, visualize the voltage at the output of the op amp. You can visualize both voltages for unipolar operation and bipolar operation at the same time on the oscilloscope.

Figure 14. Unipolar and bipolar output voltages for 000 input.

Figure 15. Unipolar and bipolar output voltages for 800 input.

Figure 16. Unipolar and bipolar output voltages for FFF input.

Question:

1. Using Ohm's law and the formula for resistors in parallel, what is the output voltage of the R-2R DAC when inputs D7 and D6 are connected to each combination of ground and 3.3 V? Please present the results as a table.

You can find the answer at the StudentZone blog.

About the Author

Andreea Pop has been a system design/architecture engineer at Analog Devices since 2019. She graduated from the integrated circuits and systems master's program and has a B.Eng. in electronics and telecommunications, both from Technical University of Cluj-Napoca. She can be reached at andreea.pop@analog.com.

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Antoniu Miclaus is a system applications engineer at Analog Devices, where he works on ADI academic programs, as well as embedded software for Circuits from the Lab®, QA automation, and process management. He started working at ADI in February 2017 in Cluj-Napoca, Romania. He is currently an M.Sc. student in the software engineering master's program at Babes-Bolyai University and he has a B.Eng. in electronics and telecommunications from Technical University of Cluj-Napoca. He can be reached at antoniu.miclaus@analog.com.

About the Author

Doug Mercer received his B.S.E.E. degree from Rensselaer Polytechnic Institute (RPI) in 1977. Since joining Analog Devices in 1977, he has contributed directly or indirectly to more than 30 data converter products and he holds 13 patents. He was appointed to the position of ADI Fellow in 1995. In 2009, he transitioned from full-time work and has continued consulting at ADI as a Fellow Emeritus contributing to the Active Learning Program. In 2016, he was named engineer in residence within the ECSE department at RPI. He can be reached at doug.mercer@analog.com.