

StudentZone— ADALM2000 Activity: Tuned Amplifier Stages

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Objective

The objective of this lab activity is to study the characteristics of tuned amplifiers.

Background

Many communications system requirements exceed the high frequency limits of op amps. In cases such as these, discrete tuned amplifiers are often used. Discrete amplifiers are typically tuned using LC (parallel inductor-capacitor) resonant circuits in place of the collector (or drain) resistors. One such circuit is shown in Figure 1.

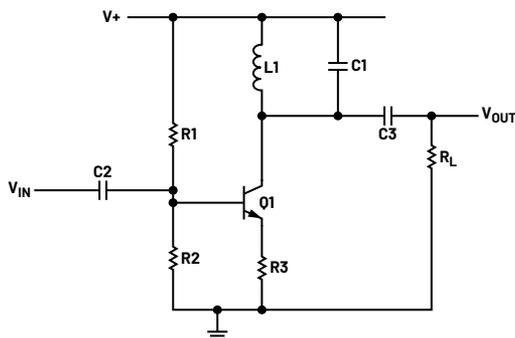


Figure 1. A common emitter amplifier with resonant output load.

The parallel LC (resonant tank) circuit determines the frequency response of the amplifier. There is a frequency at which $X_L = X_C$. This frequency, called the resonant frequency F_R , is calculated using:

$$F_R = \frac{1}{2\pi\sqrt{LC}} \quad (1)$$

As we learned in the lab on inductor self-resonance¹, it is important to take this built-in capacitance into account when designing tuned amplifiers. In an ideal resonant circuit, inductor current lags the capacitor current by 180° and the net circuit current is zero. As a result, the impedance of a parallel resonant circuit is extremely high at F_R . The common emitter amplifier voltage gain reaches its maximum value when the collector load impedance is maximum—that is, operated at F_R .

When the input frequency (F_{IN}) is lower than F_R , the circuit impedance decreases from its maximum value and is inductive. When F_{IN} is higher than F_R , the circuit impedance drops again but is capacitive. When operated at F_R , the impedance of the tank circuit reaches its maximum value. As a result, the gain of the tuned common emitter amplifier² is also at its maximum value.

Prelab Simulations

Build a simulation schematic of the tuned amplifier as shown in Figure 1. Calculate values for bias resistors, R1 and R2, such that with emitter resistor R3 set to $100\ \Omega$, the collector current in NPN transistor Q1 is approximately 5 mA. Assume the circuit is powered from a 10 V power supply. Be sure to keep the sum of R1 and R2 (total resistance) as high as practical to maintain the input impedance of the amplifier stage as high as possible. Set input and output AC coupling capacitors C2 and C3 to $0.1\ \mu\text{F}$. Calculate a value for C1 such that the resonant frequency, with L1 set equal to $100\ \mu\text{H}$, will be close to 500 kHz. Perform a small signal AC sweep of the input and plot the amplitude and phase seen at the output. Save these results to compare with the measurements you take on the actual circuit and to include with your lab report. You may also want to create simulation schematics for the circuits shown in figures 3 and 4 as well.

Materials

- ▶ ADALM2000 Active Learning Module
- ▶ Solderless breadboard and jumper wire kit
- ▶ One 2N3904 NPN transistor
- ▶ One 100 μH inductor (various other value inductors)
- ▶ Two 0.1 μF capacitors
- ▶ One 100 Ω resistor
- ▶ Other resistors and capacitors as needed

Directions

Build the circuit shown in Figure 2 on your solderless breadboard. Based on your prelab simulations, choose values for bias resistors R1 and R2 from your parts kit such that with the 100 Ω emitter resistor, R3, the collector current in NPN transistor Q1 is between 5 mA and 10 mA. Assume the circuit is powered from the +5 V and -5 V power supplies (10 V total). Be sure to keep the sum of R1 and R2 (total resistance) as high as practical to maintain the input impedance of the amplifier stage as high as possible. Again, based on your simulations, calculate a value for C1 such that the resonant frequency with the 100 μH L1 will be close to 500 kHz. Choose a standard capacitor value from the ones supplied in your parts kit or combine two in series or parallel to come as close as possible to your calculated value. Calculate a new resonant frequency based on the final value you ended up with for C1. You may want to include the effect of the parasitic winding capacitance you might have measured in the lab on inductor self-resonance.¹

The peak gain of this tuned amplifier can be very high. We will need to slightly attenuate the output signal of AWG1 by choosing a value for R_s that is 2 to 3 times larger than the parallel combination of R1 and R2 (the input resistance of the amplifier). The value of the output load, R_L , also determines the amplifier maximum gain. For the initial measurements leave R_L out of the circuit. The approximate 1 M Ω input resistance of the scope channel will serve as R_L .

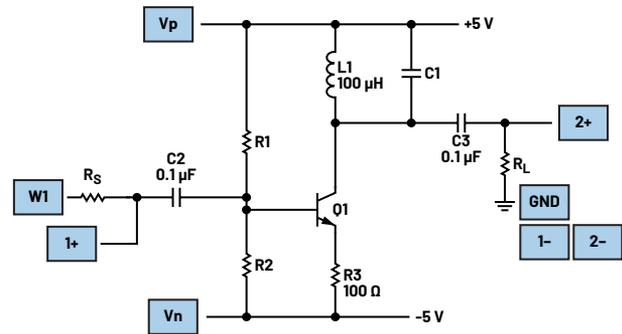


Figure 2. A common emitter tuned amplifier.

Hardware Setup

The green squares indicate where to connect the ADALM2000 module AWG, scope channels, and power supplies. Be sure to turn on the power supplies only after you double-check your wiring. Breadboard connections are presented in Figure 3.

Procedure

Open the network analyzer software instrument from the main Scopy window. Configure the sweep to start at 10 kHz and stop at 10 MHz. Set the amplitude to 200 mV and the offset to 0 V. Under the Bode scale set the magnitude top to 60 dB and range to 80 dB. Set the phase top to 180° and range to 360°. Under scope channels, click on use Channel 1 as reference. Set the number of steps to 100.

Run a single-frequency sweep. You should see amplitude and phase vs. frequency plots that look very similar to your simulation results. Once you have determined that the maximum gain of the amplifier occurs near 500 kHz, then you can reduce the frequency sweep range to start at 100 kHz and stop at 1 MHz. Be sure to export all the frequency sweep data to a .csv file for further analysis in either Excel or MATLAB®. A Scopy plot example is presented in Figure 4.

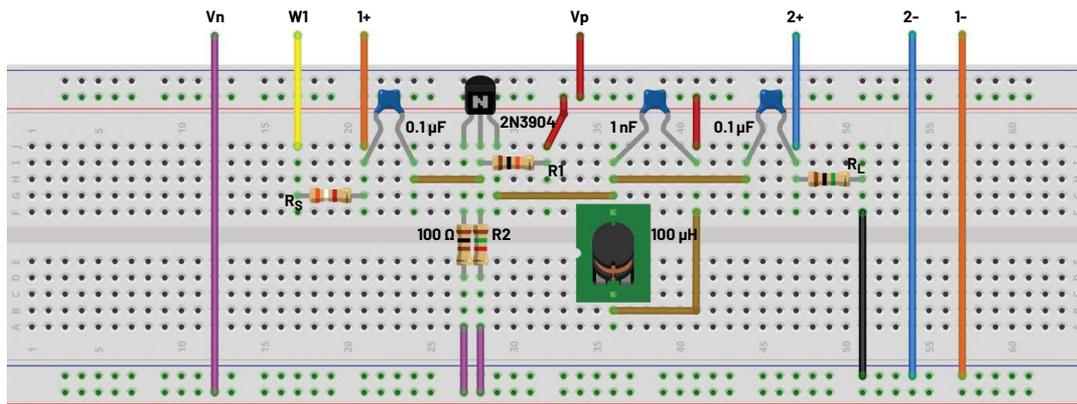


Figure 3. Common emitter tuned amplifier breadboard connections.

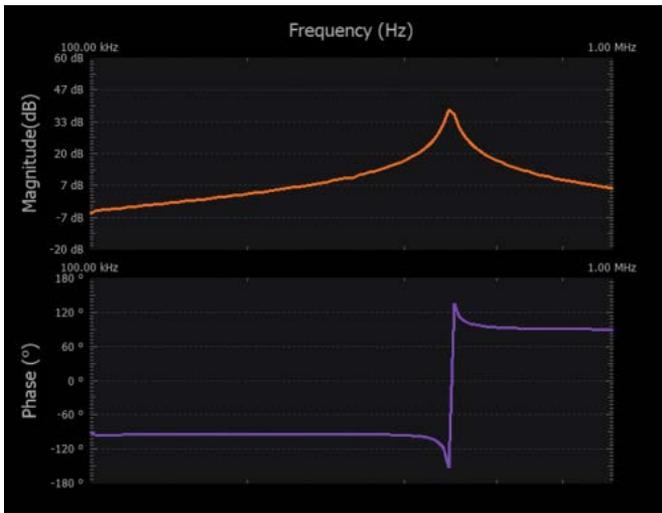


Figure 4. A common emitter tuned amplifier with R_L is 1 M Ω .

Now add the load resistor, R_L , in the circuit. Start with 100 k Ω and run a new sweep. Note the maximum gain and the frequency. Compare this to the result you got with just the scope input as the load. Try successively lower values for R_L such as 10 k Ω and 1 k Ω , etc. Note and compare your measurements.

Frequency Multipliers

Frequency multipliers or harmonic generators are a special class of amplifiers that are biased at 3 to 10 times below normal cutoff bias. They are used to generate an output frequency that is a multiple (harmonic) of a lower input frequency.

The tuned amplifier circuit of Figure 2 can operate as a frequency multiplier. If an input signal, such as a square wave or pulse that contains a large enough harmonic, has a frequency of 167 kHz, which is 1/3 of the 500 kHz resonant frequency of the output tank, the output signal would contain mostly 500 kHz where the gain is highest, or three times the input frequency. The fundamental frequency and other harmonics of the input will be greatly reduced by the tuned nature of the circuit. The fifth harmonic (frequency quintupler) is normally as high in multiplication as is practical, because harmonics of an input signal higher than the fifth are generally very weak, and the multiplied output diminishes to a very weak signal.

Directions

Calculate new values for the input bias resistor dividers, R1 and R2, such that transistor Q1 is nominally cut off ($I_c = 0$) with no input signal applied. Sine waves generally do not contain any harmonics, so set AWG1 to produce a square wave signal at 1/3 the resonant frequency you measured in the earlier tests. To generate large harmonics set the symmetry to 20% (pulse high for 20% of the period). You will need to increase the amplitude of the input pulse to greater than 2 V or remove the input attenuation source resistor R_s .

Procedure

Frequency multipliers are operated by the pulses of collector current produced by a Class C amplifier. Although the collector current flows in pulses, the alternating collector voltage is sinusoidal because of the action of the tank circuit. Use one of the scope channels to monitor the collector current pulses by measuring the voltage across emitter resistor R3. A Scopy plot example is presented in Figure 5.



Figure 5. Channel 2 measuring the voltage across emitter resistor R3.

Improved Tuned Amplifier Stage

The following circuit, shown in Figure 6 is a more versatile tuned amplifier stage using an NPN differential pair³ with an LC resonant output load.

Materials

- ▶ ADALM2000 Active Learning Module
- ▶ Solderless breadboard and jumper wire kit
- ▶ One 2N3904 NPN transistor
- ▶ One SSM2212 NPN matched transistor pair
- ▶ One 100 μH inductor (various other value inductors)
- ▶ Two 0.1 μF capacitors (marked 104)
- ▶ One 100 Ω resistor
- ▶ Two 1 $\text{k}\Omega$ resistors
- ▶ Two 2.2 $\text{k}\Omega$ resistors
- ▶ Other resistors and capacitors as needed

Directions

Build the circuit shown in Figure 6 on your solderless breadboard. Use the SSM2212 matched transistor pair for Q1 and Q2. Choose values for bias resistors R1 and R2 from your parts kit such that with the 100 Ω emitter resistor, R3, the collector current in NPN transistor Q3 is between 5 mA and 10 mA. Note in this case the R1, R2 resistor divider is powered from ground and -5 V power supply. Use the same combination of L1 and C1 as in the previous amplifier stage.

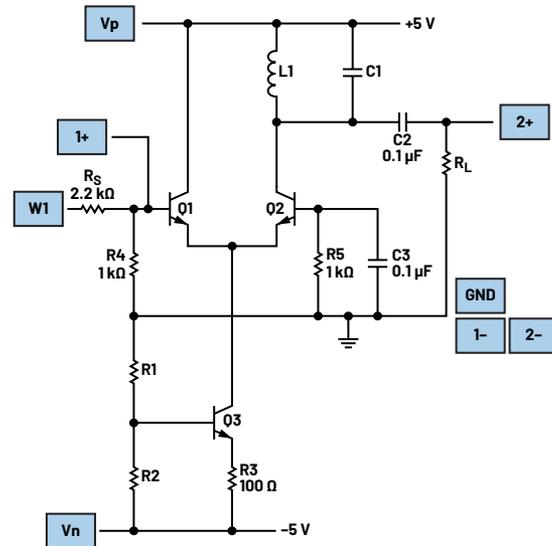


Figure 6. A differential amplifier stage with single-ended resonant output load.

Hardware Setup

The green squares indicate where to connect the ADALM2000 module AWG, scope channels, and power supplies. Be sure to turn on the power supplies only after you double-check your wiring. Breadboard connections are presented in Figure 7.

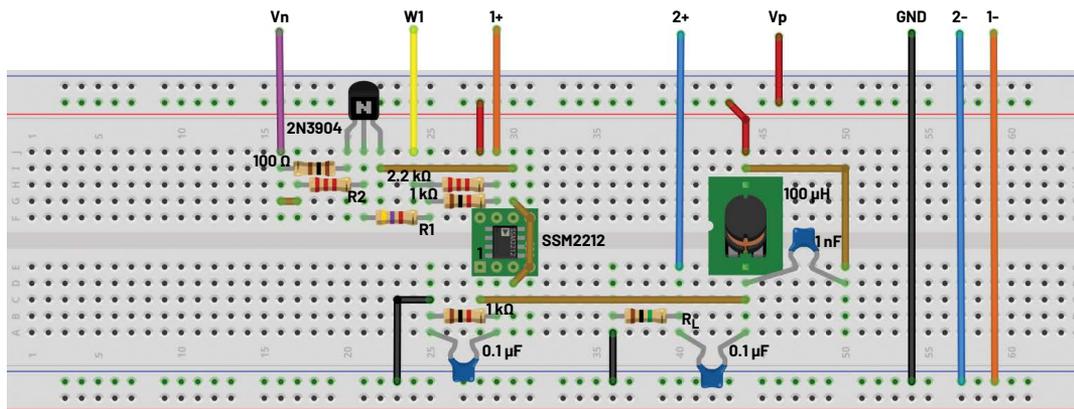


Figure 7. A differential amplifier stage with single-ended resonant output load breadboard connection.

Procedure

Open the network analyzer software instrument from the main Scopy window. Configure the sweep to start at 10 kHz and stop at 10 MHz. Set the amplitude to 200 mV and the offset to 0 V. Under the Bode scale set the magnitude top to 50 dB and range to 80 dB. Set the phase top to 180° and range to 360°. Under scope channels click on use Channel 1 as reference. Set the number of steps to 500.

As in the first experiment, run a single-frequency sweep. Once you have determined that the maximum gain of the amplifier occurs near 500 kHz then you can reduce the frequency sweep range to start at 100 kHz and stop at 1 MHz. Be sure to export the data to a .csv file for further analysis in either Excel or MATLAB. A Scopy plot example is presented in Figure 8.

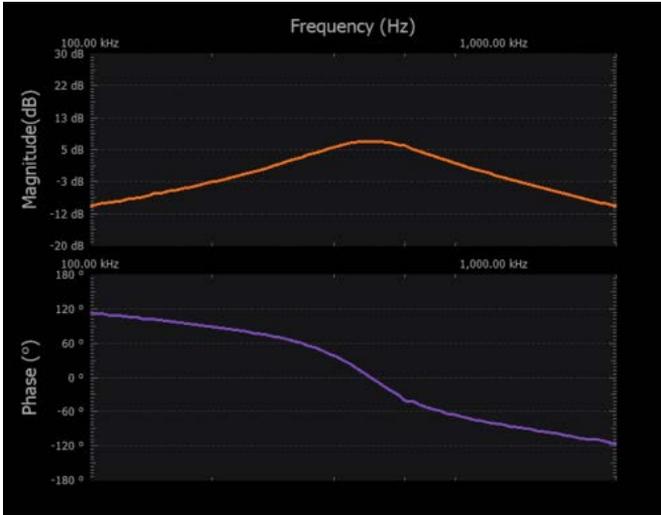


Figure 8. An improved tuned amplifier with R_L is 1 M Ω .

As before, add the load resistor, R_L , in the circuit. Start with 100 k Ω and run a new sweep. Note the maximum gain and the frequency. Compare this to the result you got with just the scope input as the load. Try successively lower values for R_L such as 10 k Ω and 1 k Ω , etc. Note and compare your measurements. They should be similar to the results you got in the first experiment.

Bonus Experiment

Amplitude modulation may be applied to the output frequency by capacitor coupling a modulating (audio frequency) signal from AWG 2 to either the base or emitter of current source transistor Q3.

Adding a 2-Pole High-Pass Filter Input Stage

It is sometimes desirable to include a simple active high-pass filter to the input of the single transistor tuned amplifier stage. The filter circuit shown in Figure 9 provides a 2-pole filter with unity gain. This filter is convenient to place in a larger circuit because it contains few components and does not occupy much space.

The active high-pass transistor circuit is quite straightforward, using just a total of four resistors, two capacitors, and the same single transistor. The operating conditions for the transistor are set up in the normal way. As in Figure 1, R1 and R2 are used to set up the bias point for the base of the transistor. The resistor R3 is the emitter resistor and sets the current for the transistor.

The filter components are included in negative feedback from the emitter of the transistor to the input. The components that form the active filter network consist of C2, C3, R4, and the combination of R1 and R2 in parallel, assuming that the input resistance to the base of the transistor is very high and can be ignored.

$$C2 = 2 \times C3 \quad (2)$$

$$R4 = \frac{(R2 \times R1)}{(R2 + R1)} \quad (3)$$

This is for values where the effect of the transistor itself within the high-pass filter circuit can be ignored, that is:

$$R3(\beta + 1) \gg \frac{(R2 \times R1)}{(R2 + R1)} \quad (4)$$

$$F_0 = \frac{1.414}{(4\pi R4 C2)} \quad (5)$$

Where:

β = the forward current gain of the transistor

F_0 = the cutoff frequency of the high-pass filter

π = equal to 3.14159

The equations for determining the component values provide a Butterworth response, which provides maximum flatness within the pass band at the expense of achieving the ultimate roll off as quickly as possible. This has been chosen because this form of filter suits most applications, and the mathematics works out easily.

Materials

- ▶ ADALM2000 Active Learning Module
- ▶ Solderless breadboard and jumper wire kit
- ▶ One 2N3904 NPN transistor
- ▶ One 100 μ H inductor (various other value inductors)
- ▶ One 0.1 μ F capacitor
- ▶ One 100 Ω resistor
- ▶ Other resistors and capacitors as needed

Directions

Build the circuit shown in Figure 9 on your solderless breadboard. Use the same values for bias resistors R1 and R2 that you used in Experiment 1 (Figure 2). Use the same combination of L1 and C1 as in the previous amplifier stage. Using the formula above for the high-pass cut off frequency F_0 , calculate values for C2, C3, and R4 that results in a frequency more than two octaves below the resonance frequency of L1 and C1. For example, if F_R is equal to 500 kHz then base your calculations on F_0 equal to 125 kHz.

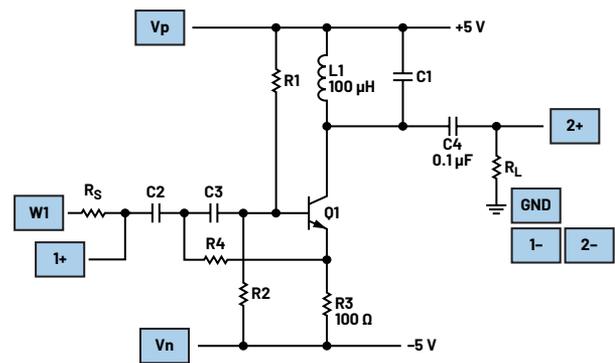


Figure 9. Adding a 2-pole high-pass input filter to the tuned amplifier.

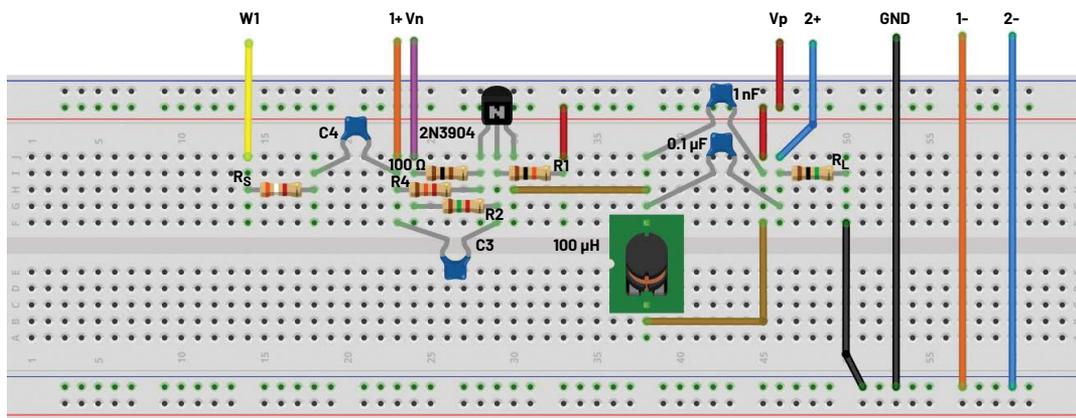


Figure 10. A breadboard connection.

Hardware Setup

The green squares indicate where to connect the ADALM2000 module AWG, scope channels, and power supplies. Be sure to turn on the power supplies only after you double-check your wiring (Figure 10).

Procedure

Open the network analyzer software instrument from the main Scopy window. Configure the sweep to start at 10 kHz and stop at 10 MHz. Set the amplitude to 200 mV and the offset to 0 V. Under the Bode scale set the magnitude top to 30 dB and range to 60 dB. Set the phase top to 180° and range to 360°. Under scope channels, click on use Channel 1 as reference. Set the number of steps to 100.

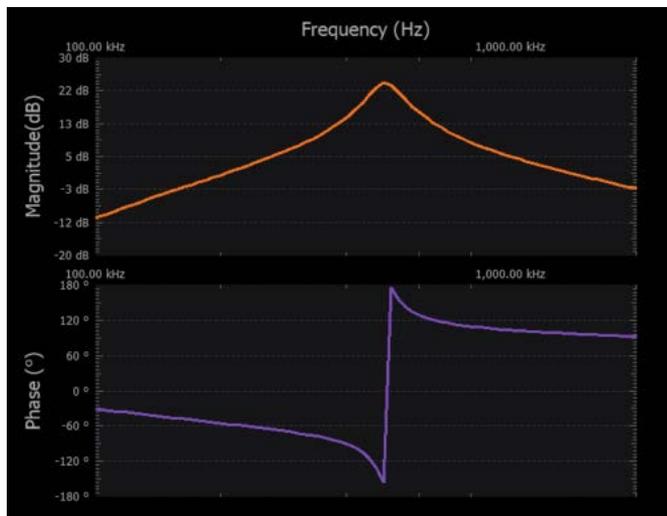


Figure 11. The result with R_1 is 1 M Ω .

As in the first experiment, run a single-frequency sweep with scope Channel 2 connected through coupling capacitor C4 to the collector of Q1. To measure the response of the high-pass input filter, connect scope Channel 2 through coupling capacitor C4 to the base of Q1. Be sure to export the data to a .csv file for further analysis in either Excel or MATLAB. Compare the response curves with what you measured for the circuit in Figure 2. Try different combinations of values for C2, C3, and R4 to see how the frequency response changes. A Scopy plot example is shown in Figure 11.

Questions

1. What are the components commonly used to tune amplifiers when op amps are not suitable for high frequency requirements?
2. What happens to the impedance of a parallel resonant circuit at its resonant frequency, and how does this affect the voltage gain of a common emitter amplifier?
3. What is the primary function of the high-pass filter mentioned in the text, and how does it affect the amplifier's input signal?

You can find the answers at the [StudentZone blog](#).

References

- ¹"Activity: Inductor Self Resonance." Analog Devices, Inc., June 2020.
- ²"ADALM2000 Activity: Common Emitter Amplifier." *Analog Dialogue*, Vo. 54, No. 2, June 2020.
- ³"ADALM2000 Activity: BJT Differential Pair." *Analog Dialogue*, Vo. 55, No. 2, June 2021.



About the Author

Antoniu Miclaus is a system applications engineer at Analog Devices, where he works on ADI academic programs, as well as embedded software for Circuits from the Lab[®], QA automation, and process management. He started working at ADI in February 2017 in Cluj-Napoca, Romania. He currently holds an M.Sc. degree in software engineering from the Babes-Bolyai University and a B.Eng. degree in electronics and telecommunications from the Technical University of Cluj-Napoca.