

AnalogDialogue

ADALM2000 Activity: Adjustable External Triggering Circuit

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Objective

The objective of this lab activity is to investigate a circuit to interface analog signals to the digital external trigger input(s) of the ADALM2000 module.

Background

The ADALM2000 scope module is most often triggered from one of its analog input channels. The module will display stable waveforms with the horizontal time scale (align zero-time point) based on whichever channel is selected as the trigger source. It is sometimes desirable to trigger the display (zero-time point reference) using a third signal from some other point in the circuit being tested. The ADALM2000 hardware provides two external digital inputs/outputs, T1 and T0, which can be selected as trigger inputs. Using these digital inputs, the displayed waveforms will align (set the zero-time point) with the rising edge of the applied signal. These are, however, digital inputs and only allow input voltages between 0 V and 5 V. They have a fixed threshold voltage. To use these external trigger inputs with analog input signals—that is, between -5 V and +5 V—a voltage comparator circuit is needed, along with an adjustable voltage source to set the trigger voltage level.

Materials

- ADALM2000 Active Learning Module
- Solderless breadboard
- Jumper wires
- One AD8561 comparator (or AD790 alternate with slightly different pinout)
- One 74HCO4 hex CMOS inverter (or CD4007, see Appendix)
- Three 1 kΩ resistors
- One 1 MΩ resistor
- One 10 kΩ potentiometer
- One 0.1 µF capacitor
- One 0.0047 µF capacitor

Directions

Build the circuit shown in Figure 1 on your solderless breadboard. The AD8561 analog comparator has noninverted (true) and inverted (complement) outputs. The input of the first inverter can be alternately connected to either the Pin 7 output,



Figure 1. An analog trigger circuit.



Figure 2. Analog trigger breadboard circuit.

for a rising edge, or the Pin 8 output, for a falling edge trigger. Start with it connected to Pin 7. The 74HCO4 hex inverter is suggested but a CD4069 hex inverter may be substituted, or the two inverters can be built using the CD4007 transistor array (see Appendix).

The AD8561 has a very high bandwidth and will respond to any high frequency noise that might be present on the input signal. This will cause its output(s) to switch back and forth multiple times very quickly if the input signal is near the threshold voltage (V_{TH}). This noise will cause the waveform to be displayed on the screen to jump or jitter back and forth and look unstable. Resistor R5 and capacitor C1 form a low-pass filter and are inserted between the two inverter stages to reduce these very fast switching spikes. The time constant of this filter would be adjusted based on the nature of the signal being used as the external trigger.

Hardware Setup

Waveform generator AWG1 should be set up as a triangle wave with an 8 V amplitude peak-to-peak and, an 0 V offset, and a frequency of 5 kHz. Set the horizontal and vertical scales of the scope to display at least one complete cycle of the input triangle waveform. Turn on the power supplies only after double checking your circuit connections.

Procedure

To start, set the scope trigger source to Channel 1, rising edge, with the level set to 0 V. You should see the rising edge of the triangle wave on Channel 1 centered on the zero-time point along the horizontal axis. The rising edge of the digital output of the second inverter on Channel 2 should occur at different times along the horizontal axis depending on the setting of the potentiometer, R3. Adjust R3

up and down from one end of its range to the other and observe where the rising edge of the pulse on Channel 2 occurs with respect to the voltage (vertical axis) of the triangle wave at that time point.



Figure 3. A scope shot at oscilloscope Channel 1's rising edge trigger on a different potentiometer value.

Now switch the scope trigger source to External 1 (T1 input) and repeat the sweep of R3 from one end of its range to the other. You should be able to align the zero-time point anywhere along the rising edge.



Figure 4. A scope shot at the oscilloscope external trigger's rising edge on a different potentiometer value.

Now move the input of the first inverter to Pin 8 of the AD8561. The zero-time point should now align with the falling edge of the input triangle wave. Again, repeat the sweep of R3 to confirm that you can align the zero-time point anywhere along the falling edge.

Question:

1. What methods, other than the RC filter, could be used to remove the noise jitter from the comparator?

You can find the answer at the StudentZone blog.

Appendix: Making an Inverter with the CD4007 Transistor Array

Figure 5 shows the schematic and pinout for the CD4007.



Figure 5. The CD4007 CMOS transistor array pinout.

As many as three individual inverters can be built from one CD4007 package. The simplest one to configure, as shown in Figure 6, is by connecting pins 8 and 13 together as the inverter output. Pin 6 will be the input. Be sure to connect Pin 14 V_{DD} to power and Pin 7 V_{SS} to ground.



Figure 6. An inverter circuit.

The second inverter is made by connecting Pin 2 to V_{DD} and Pin 4 to V_{SS} ; pins 1 and 5 are connected together as the output and with Pin 3 as the input. The third inverter is made by connecting Pin 11 to V_{DD} and Pin 9 to V_{SS} ; Pin 12 is the output and Pin 10 is the input.



About the Author

Antoniu Miclaus is a system applications engineer at Analog Devices, where he works on ADI academic programs, as well as embedded software for Circuits from the Lab[°], QA automation, and process management. He started working at ADI in February 2017 in Cluj-Napoca, Romania. He is currently an M.Sc. student in the software engineering master's program at Babes-Bolyai University and he has a B.Eng. in electronics and telecommunications from Technical University of Cluj-Napoca.



About the Author

Doug Mercer received his B.S.E.E. degree from Rensselaer Polytechnic Institute (RPI) in 1977. Since joining Analog Devices in 1977, he has contributed directly or indirectly to more than 30 data converter products and holds 13 patents. He was appointed to the position of ADI Fellow in 1995. In 2009, he transitioned from full-time work and has continued consulting at ADI as a fellow emeritus contributing to the Active Learning Program. In 2016, he was named engineer in residence within the ECSE department at RPI.



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