Vol 56, No 2—May 2022

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AnalogDialogue

# StudentZone—ADALM2000 Activity: Silicon Controlled Rectifiers (SCR)

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## Objective

The objective of this lab activity is to examine the structure and operation of the silicon controlled rectifier (SCR). SCRs are mainly used in devices where the control of high power, possibly at high voltage, is needed. The ability to switch large currents on and off makes the SCR suitable for use in medium to high voltage AC power control applications such as lamp dimming, regulators, and motor control. In addition, unintentional SCRs can form in integrated circuits and when these SCRs get triggered, they can lead to circuit malfunction or even reliability problems and damage.

## Background

SCRs are 4-layer solid-state current controlling devices with three terminals. They have anode and cathode terminals like a conventional diode and a third control terminal, referred to as the gate. SCRs are unidirectional devices: they conduct current only in one direction, like a diode or rectifier. SCRs are triggered only by currents going into the gate. The SCR combines the rectifying features of diodes and the on/off control features of transistors.

SCRs are generally used in power switching applications. In the normal off state, the device restricts current flow to the leakage current. When the gate-to-cathode current exceeds a certain threshold, the device turns on and conducts current. The SCR will remain in the on state even after gate current is removed as long as the current through the device exceeds the holding current. Once the current falls below the holding current for a period of time, the device will switch off. If the gate is pulsed and the current through the device is below the latching current, the device will remain in the off state.

Looking at Figure 1b, which shows the 4-layer structure of the SCR, we see the three terminals: one from the outer p-type layer called anode A, the second from the outer n-type layer called cathode K, and the third from the base of the lower NPN transistor section called gate G.

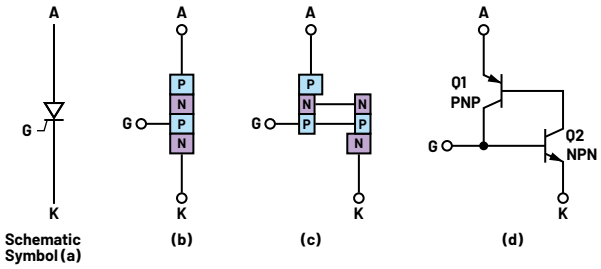


*Figure 1. SCR equivalent circuits.*

The SCR, as shown in Figure 1c, can be visualized as two separate transistors. The equivalent circuit of an SCR is composed of a PNP transistor and an NPN transistor interconnected, as shown in Figure 1d. We see that the collector of each transistor is connected to the base of the other, forming a positive feedback loop.

The SCR has two stable states. The first is the nonconducting off state. With the gate terminal open, let us first assume that no current is flowing into the base terminal of NPN transistor Q2. Given zero base current, the collector current of Q2 will also be zero. Given zero collector for Q2, we see that there should be zero current flowing out of the base of PNP transistor Q1. Given zero base current in Q1, we see that there should be zero collector current in Q1. This is consistent with our original assumption of zero current in the base of Q2. With zero collector current (and zero base current) in both Q1 and Q2, we can tell that there should be no emitter current in either transistor as well. This zero current off state is stable as long as any leakage current through Q1 or Q2 from emitter to collector is very small.

The second stable state is the conducting on state. We can transition or switch the SCR from the off state to the on state by injecting a small current into the gate terminal. Going through the same procedure around the loop we just did for the off state, we can see that as soon as a base current is supplied to Q2, a larger collector current ($\beta_{NPN}$ times the base current) will start to flow. This Q2 collector current becomes base current for Q1. This base current in Q1 produces

a larger collector current ($\beta_{PNP}$ times the base current) in Q1. The collector current of Q1 feeds back into the base of Q2 increasing its base current even more. Once this feedback loop of current is established, the initial gate current can be removed and the SCR will remain in the conducting on state for as long as the external circuit around the SCR supplies current through the SCR. The only way to turn off the SCR is for the current to drop below a critical "holding" current level.

An observation to note about this positive feedback loop is that it will hold the SCR on and remain in this latched state as long as the following is true:

$$\beta_{PNP} \times \beta_{NPN} = 1 \quad (1)$$

The voltage drop across the SCR from terminal A to K when the SCR is conducting is the sum of $Q1_{VBE}$ and $Q2_{VCESAT}$ in parallel with the sum of $Q2_{VBE}$ and $Q1_{VCESAT}$. We know that the β of BJT devices falls as the collector base junction is forward biased into the saturation region that is $V_{CE}$ less than $V_{BE}$. The $V_{CE}$ of the two transistors will drop until the positive feedback gain equation is satisfied and $\beta_{PNP} \times \beta_{NPN}$ is equal to 1.

It is also important to note that the β of BJT transistors is low for small values of collector current and from the above equation, the SCR will remain in the off state as long as the leakage current is so small that $\beta_{PNP} \times \beta_{NPN}$ is less than 1 at this low leakage current level.

The ADALP2000 Analog Parts Kit does not include an SCR but we can emulate one by building the equivalent circuit shown in Figure 1d from discrete PNP and NPN transistors.

## Materials

- ADALM2000 Active Learning Module
- Solderless breadboard
- Two 1 kΩ resistors
- Two 100 kΩ resistors
- One 0.1 µF capacitor
- One small signal NPN transistor (2N3904)
- One small signal PNP transistor (2N3906)

## Directions

Build the model of the equivalent circuit of an SCR as shown in Figure 2 on your solderless breadboard.

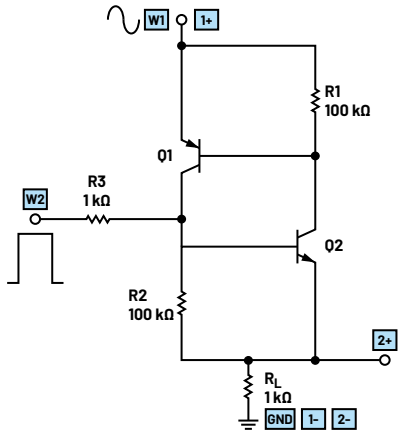


*Figure 2. Circuit to emulate an SCR.*

The two 100 kΩ resistors, R1 and R2, are placed across the respective $V_{BE}$ of each transistor to insure that any small leakage currents do not self trigger the simulated SCR. Resistor R3 converts the voltage pulse from AWG2 into a triggering current.

## Hardware Setup

The breadboard connections of the SCR are presented in Figure 3.

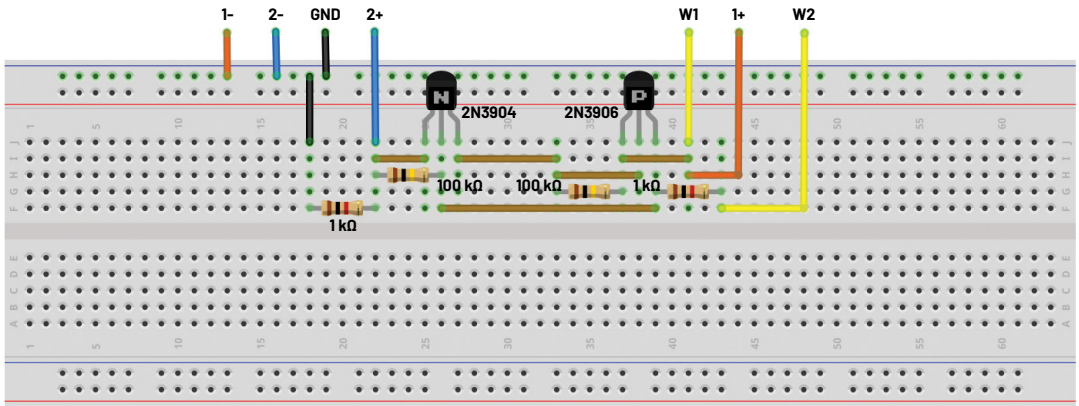


*Figure 3. Breadboard connections of circuit to emulate an SCR.*

## Procedure

AWG1 should be configured as a sine wave with an amplitude of 10 V peak-to-peak, zero offset, and a frequency of 100 Hz. AWG2 should be configured as a square wave with an amplitude of 800 mV peak-to-peak, 400 mV offset, and a frequency of 100 Hz. Be sure to run the two AWG channels synchronously.

Trigger the scope on Channel 1. While observing the input sine wave on Scope Channel 1 and the voltage across $R_L$ on Scope Channel 2, adjust the phase of AWG2 in steps from 180° to 360°. Depending on the phase setting of AWG2, you should see something that looks similar to the figures below. You will notice that the voltage across $R_L$ is zero, SCR in off state, until the trigger pulse from AWG2 occurs and the SCR remains in the on state until the input sine wave voltage crosses zero.

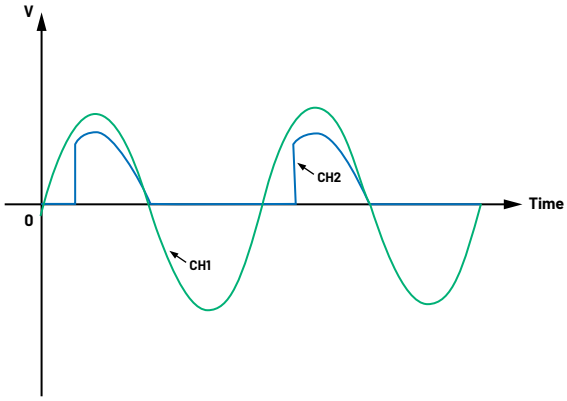


*Figure 4. Waveforms example.*

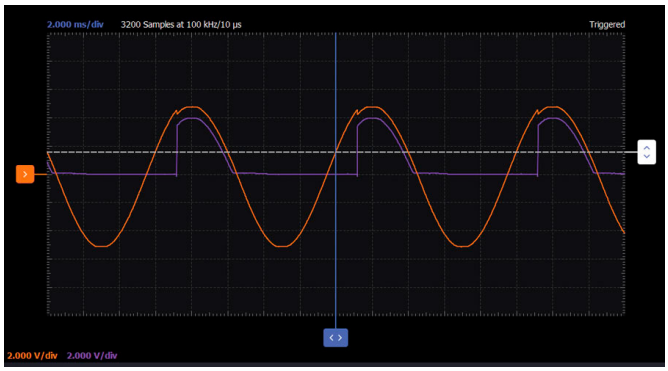


*Figure 5. Scopy waveforms example.*

Measure and report the voltage drop across the SCR when it is in the on state and conducting current.

Find the minimum pulse voltage (amplitude) above ground that will trigger the SCR by adjusting AWG2. Estimate the minimum trigger current based on this voltage, R3, and the $V_{BE}$ of Q2. Explain your result.

Try larger (1 MΩ) and smaller (10 kΩ) values for R1 and R2. How does this change the minimum trigger voltage?

Replace resistor R3 with a 0.1 µF capacitor. This coupling capacitor acts as a differentiator turning the square pulse of the AWG output into narrow positive and negative spikes of current on the rising and falling edges of the square wave. How does this affect when and how the SCR is triggered?

## Unintentional Parasitic SCRs in Integrated Circuits

We have explored applications for the SCR that intentionally make use of its characteristics. Unfortunately, unintentional SCRs can form in integrated circuits and if these parasitic SCRs get triggered they can cause circuit malfunction or even reliability issues and damage to the integrated circuit.

### Latch-Up

Latch-up is a potentially destructive situation in which a parasitic SCR is triggered, shorting the positive and negative supplies together. If current flow is not limited, electrical overstress will occur. The classic case of latch-up occurs in CMOS output devices, in which the driver transistors and wells form a 4-layer PNPN SCR structure when one of the two parasitic base-emitter junctions is momentarily forward biased during an overvoltage upset event. The SCR turns on and essentially causes a short between the $V_{DD}$ power supply and ground.

Since all these MOS devices are located close together on the monolithic die, with appropriate external excitation, the parasitic SCR devices may turn on, a behavior common with poorly designed CMOS circuits. Figure 6 illustrates a simplified cross section showing two transistors, one PMOS and one NMOS; these could be connected together as logic gates or as an analog amplifier or switch. The parasitic bipolar transistors responsible for latch-up behavior, Q1 (vertical PNP) and Q2 (lateral NPN) are as indicated.

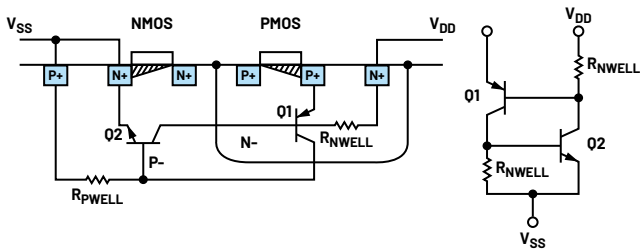


*Figure 6. Cross section of PMOS and NMOS devices, with parasitic transistors Q1 and Q2.*

Proper design methods to reduce the possibility of SCR formation include increasing the spacing between NMOS and PMOS devices and interposing highly doped regions between and around NWELLs and PWELLs. Both of these layout approaches attempt to lower the β of either the vertical PNP or the lateral NPN parasitic bipolar transistors to less than 1. Some of these methods also tend to lower the resistance of $R_{PWELL}$ and $R_{NWELL}$ which increases the minimum trigger current needed to turn on the SCR.

## Question:

1. How does the SCR differ from an ordinary rectifier diode?

You can find the answer at the StudentZone blog.

## About the Author

Doug Mercer received his B.S.E.E. degree from Rensselaer Polytechnic Institute (RPI) in 1977. Since joining Analog Devices in 1977, he has contributed directly or indirectly to more than 30 data converter products and holds 13 patents. He was appointed to the position of ADI Fellow in 1995. In 2009, he transitioned from full-time work and has continued consulting at ADI as a fellow emeritus contributing to the Active Learning Program. In 2016, he was named engineer in residence within the ECSE department at RPI.

## About the Author

Antoniu Miclaus is a system applications engineer at Analog Devices, where he works on ADI academic programs, as well as embedded software for Circuits from the Lab®, QA automation, and process management. He started working at Analog Devices in February 2017 in Cluj-Napoca, Romania. He is currently an M.Sc. student in the software engineering master's program at Babes-Bolyai University and he has a B.Eng. in electronics and telecommunications from Technical University of Cluj-Napoca.