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AnalogDialogue

StudentZone—ADALM2000 Activity: TTL Inverter and NAND Gate

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Objectives

A variety of digital logic circuit techniques have been in use since the 1960s when integrated logic gates were first produced. In this laboratory activity, the transistor-transistor logic (TTL) circuit inverter (not gate) and 2-input NAND gate configurations are examined.

Background

The schematic of a TTL inverter is shown in Figure 1. This circuit overcomes the limitations of the single transistor inverter circuit. The basic TTL inverter consists of three stages: a current steering input, a phase splitting stage, and an output driver stage.

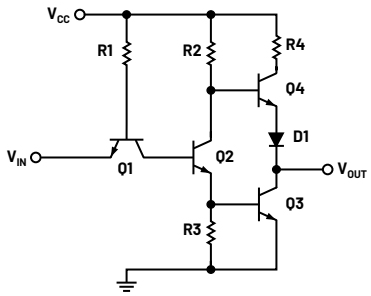


Figure 1. A TTL inverter.

The input stage transistor Q1 performs a current steering function. It can be thought of as a back-to-back diode arrangement. The transistor is operated in either forward or reverse mode to steer current to or from the second stage transistor's base, Q2. The forward current gain or β_F is much larger than the reverse β_R. It provides a higher discharge current to discharge the base when turning it off.

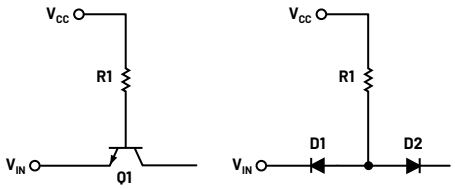


Figure 2. The equivalent circuit of the input current steering stage.

The second stage transistor, Q2 in Figure 1, uses a phase splitter to drive both halves of the pull-up and pull-down output stages. It allows the input condition to be produced in opposite phases so that the output transistors can be driven in antiphase. This allows Q3 to be on when Q4 is off and vice versa as shown in Figure 3.

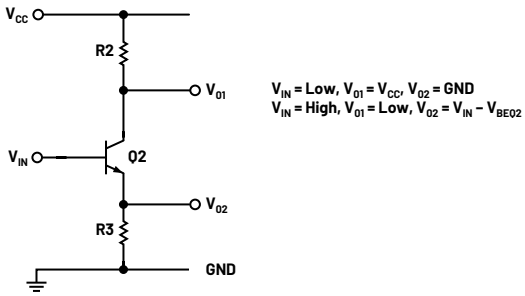


Figure 3. The phase splitting stage.

The output transistor pair, Q3 and Q4 along with diode D1, is referred to as a totem-pole output as shown in Figure 4. This output configuration provides the ability to both actively source or sink current and is useful for driving capacitive loads. Resistor R4 serves to limit the current available from V_{CC}. Under steady-state conditions, only one transistor is on at a time.

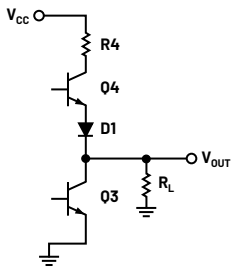


Figure 4. The output stage.

The diode, D1, serves to increase the effective turn on voltage of Q4, which allows it to be turned off before Q3 turns fully on. This helps prevent potentially large surge currents from flowing in the output stage during transitions between logic states. Resistor R4 also serves to limit the current that is allowed to flow in the output stage. The disadvantage is that the logic high voltage is reduced by an amount of the diode drop as shown in Figure 11.

Materials

- ADALM2000 Active Learning Module
- Solderless breadboard
- Jumper wires
- One 100 kΩ resistor
- One 2.2 kΩ resistor
- One 470 Ω resistor
- One 100 Ω resistor
- One small signal diode (1N914)
- Five small signal NPN transistors (2N3904 and/or SSM2212)

TTL Inverter

Directions

There are five 2N3904 NPN transistors supplied with the ADALP2000 analog parts kit. Older kits may contain one SSM2212 matched pair. The suggested breadboard layouts shown are for the SSM2212 connections. If you are using just the 2N3904 devices, change the layout as needed.

Construct the TTL inverter circuit as shown in Figure 5 on your solderless breadboard. If the SSM2212 NPN pair is used, it can replace only Q3 and Q4 (output stage) since it contains internal protection diodes across the base and emitter terminals to prevent them from being reverse biased.

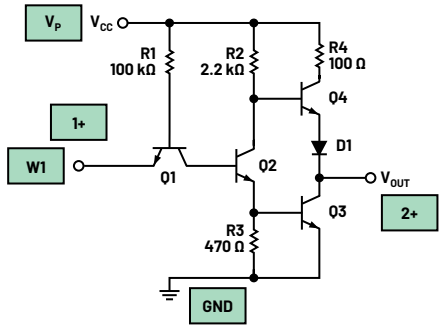


Figure 5. A TTL inverter.

Hardware Setup

Connect your circuit to the ADALM2000 input/output connector as indicated in Figure 5. It is best to ground the unused negative scope inputs when not being used.

The breadboard connections are shown in Figure 6.

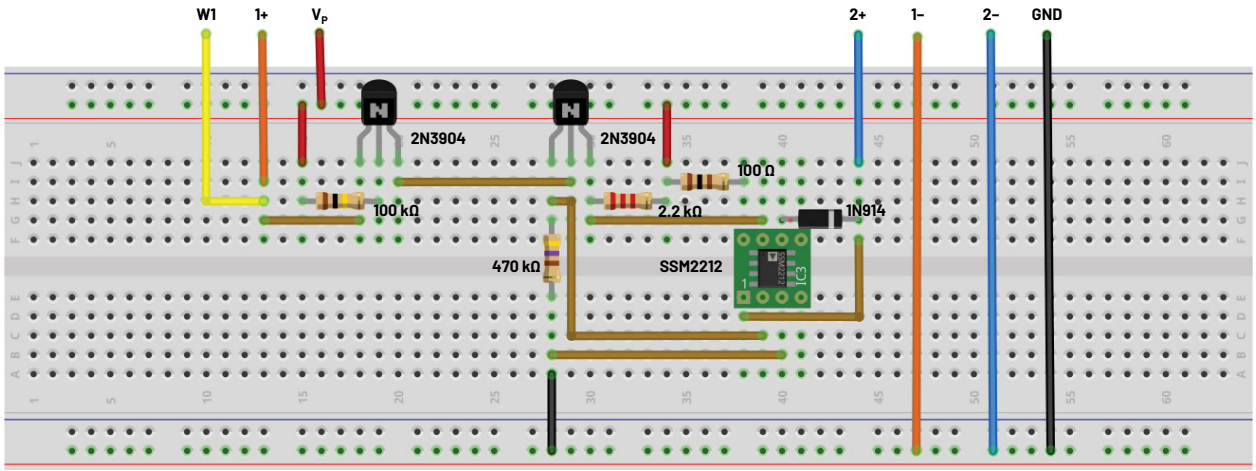


Figure 6. A TTL inverter breadboard circuit.

Procedure

Configure waveform generator, W1, with a 100 Hz triangle wave with 0 V offset and 6 V amplitude peak-to-peak values. Use the oscilloscope in the x-y mode to observe the voltage-transfer curve of the circuit.

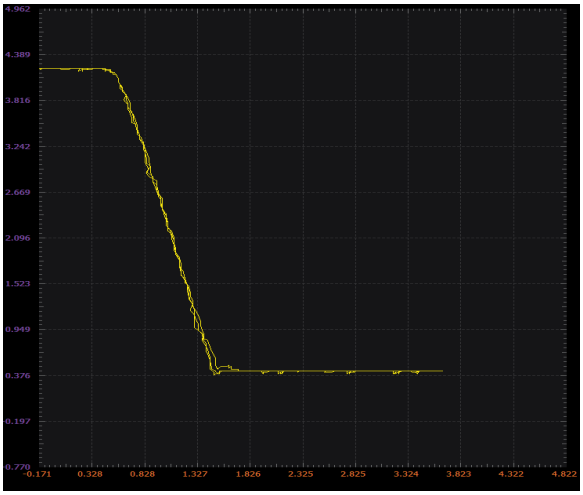


Figure 7. A TTL inverter transfer curve.

TTL NAND Gate

Directions

By adding another input to the TTL inverter, a TTL NAND gate can be made. Connect the TTL inverter circuit, which is shown in Figure 8.

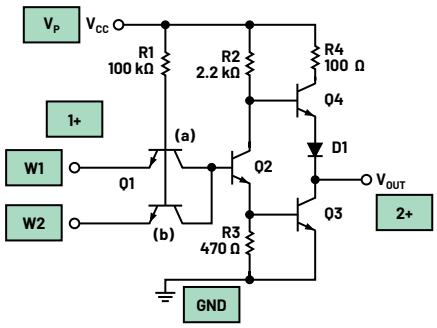


Figure 8. A TTL 2-input NAND gate.

Hardware Setup

Connect your circuit to the ADALM2000 I/O connector as indicated in Figure 8. It is best to ground the unused negative scope inputs when not being used.

The breadboard connections are shown in Figure 9.

Procedure

Configure waveform generator, W1, with a 100 Hz triangle wave with 0 V offset and 6 V amplitude peak-to-peak values, and W2 with a 100 Hz triangle wave with 0 V offset and 6 V amplitude peak-to-peak value and 90° phase.

Use the oscilloscope to observe the output of the circuit, Ch2.

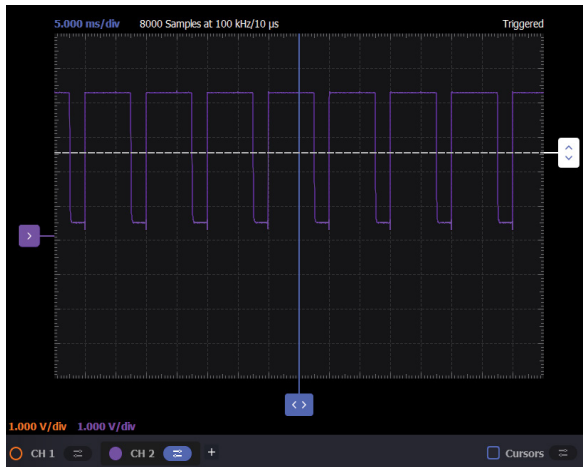


Figure 10. TTL NAND gate output waveform.

Measurements

Transfer Characteristic

The transfer characteristic of a TTL inverter can be deduced by applying a slowly ramping input voltage and determining the sequence of events that takes place with respect to changes in the states of conduction of each transistor and the critical points at which the onset of these changes happen. Consider the circuit input vs. output transfer characteristic curve shown in Figure 11.

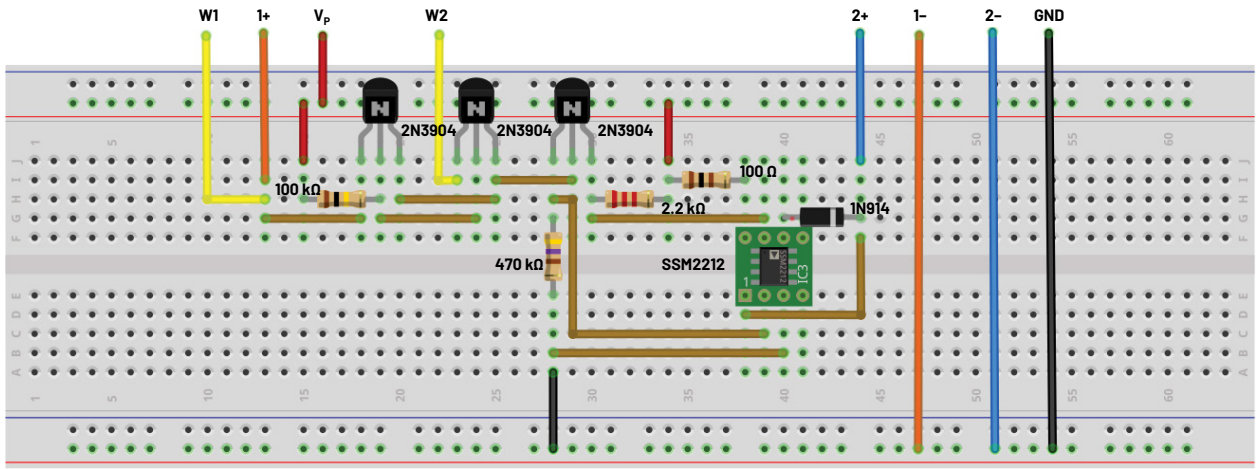


Figure 9. A TTL 2-input NAND gate breadboard circuit.

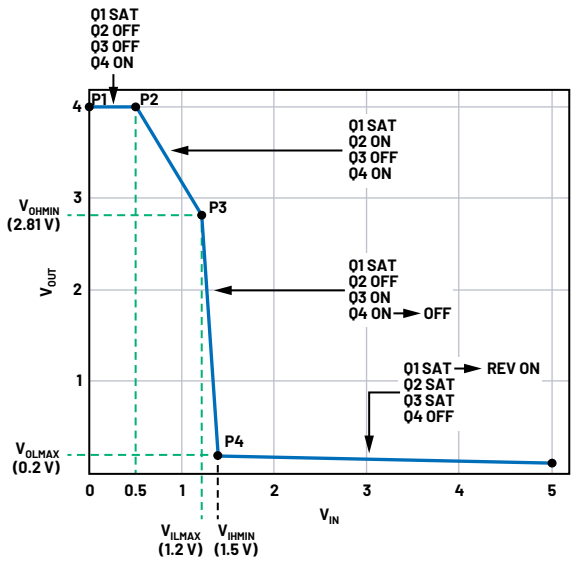


Figure 11. TTL inverter input vs. output transfer curve.

Break Point P1

With the input near 0 V and the base current supplied to Q1, this transistor can conduct in forward mode. Since the only source of collector current is the leakage of Q2, Q1 will be driven into saturation. This ensures that Q2 is off, which, in turn, means that Q3 is off. While there is no load present, there are leakage currents flowing in the output stage, which allow the transistor Q4 and the diode D1 to barely conduct in the on state.

$V_{OUT} = V_{CC} - V_{BE4} - V_{D1}$

$V_{OUT} = 5\ V - 0.6\ V - 0.6\ V = 3.8\ V$

Point P1: $V_{IN} = 0.5\ V$, $V_{OUT} = 3.8\ V$

Break Point P2

As the input voltage is slightly increased, the above state continues until, with Q1 on and in saturation, the voltage at the base of Q2 rises to the point of conduction. Then:

$V_{IN} = V_{BE2} - V_{CE1(SAT)} = 0.6\ V - 0.1\ V = 0.5\ V$

Point P2: $V_{IN} = 0.5\ V$, $V_{OUT} = 3.8\ V$

Break Point P3

As the input voltage is further increased, Q2 becomes more conductive, turning fully on. Base current to Q2 is supplied by the now forward biased base-collector junction of Q1, which is still in saturation. Eventually, Q3 reaches the point of conduction. This happens when:

$V_{IN} = V_{BE2} + V_{BE3} - V_{CE1(SAT)}$

$V_{IN} = 0.7\ V + 0.6\ V - 0.1\ V = 1.2\ V$

Note that with transistor Q3 just at turn on, $V_{BE3} = 0.6\ V$, which means that the current through R3 is 0.6 V/470 Ω = 1.27 mA. With operation in the linear active region, the collector current in Q2 is 0.97 mA × 1.27 mA = 1.23 mA.

The voltage drop across R2 is then $V_{R2} = 1.23\ mA \times 2.2\ k\Omega = 2.7\ V$.

Under this condition, the collector to emitter voltage drop across Q2 is:

$V_{CE2} = V_{CC} - V_{R2} - V_{R3}$

$V_{CE2} = 5\ V - 2.7\ V - 0.6\ V = 1.7\ V$

This confirms that Q2 is still operating in the forward active mode.

With Q3 beginning to conduct, there is a conduction path for current through Q4 and the diode, D1, which then turns fully on. In this case:

$V_O = V_{CC} - V_{R1} - V_{BE4} - V_{D1}$

$V_O = 5\ V - 0.94\ V - 0.65\ V - 0.6\ V = 2.81\ V$

Point 3: $V_I = 1.2\ V$, $V_O = 2.81\ V$

Break Point P4

As the input voltage is further increased, Q2 conducts more heavily, eventually entering the saturation mode. Q3 also conducts more heavily and eventually reaches the point of saturation. As Q2 becomes more conductive, its collector current increases. This increases the voltage drop across R1, which means that the voltage across Q2—that is, VCE2—drops. This falls below the requirement for conduction in Q4 and the diode, D1, so that both turn off prior to the saturation of Q3.

When Q3 reaches the edge of saturation:

$V_I = V_{BE2} + V_{BE3} - V_{CE1}$

$V_I = 0.7\ V + 0.7\ V - 0.1\ V = 1.3\ V$

Point 4: $V_I = 1.4\ V$, $V_O = 0.2\ V$

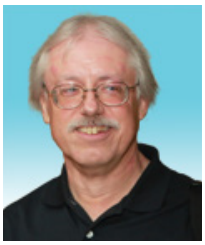
Question:

1. The output circuitry of a typical TTL logic gate is commonly referred to as a totem-pole output because the two output transistors are stacked one above the other like carvings on a totem pole. Is a gate circuit with a totem-pole output stage able to source load current, sink load current, or do both?

You can find the answer at the StudentZone blog.

About the Author

Antoniu Miclaus is a system applications engineer at Analog Devices, where he works on ADI academic programs, as well as embedded software for Circuits from the Lab®, QA automation, and process management. He started working at ADI in February 2017 in Cluj-Napoca, Romania. He is currently an M.Sc. student in the software engineering master's program at Babes-Bolyai University and he has a B.Eng. in electronics and telecommunications from Technical University of Cluj-Napoca.



About the Author

Doug Mercer received his B.S.E.E. degree from Rensselaer Polytechnic Institute (RPI) in 1977. Since joining Analog Devices in 1977, he has contributed directly or indirectly to more than 30 data converter products and holds 13 patents. He was appointed to the position of ADI Fellow in 1995. In 2009, he transitioned from full-time work and has continued consulting at ADI as a fellow emeritus contributing to the Active Learning Program. In 2016, he was named engineer in residence within the ECSE department at RPI.