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StudentZone— ADALM2000 Activity: CMOS Logic Circuits, Transmission Gate XOR

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Objective

The objective of this lab activity is to reinforce the basic principles of CMOS logic from the previous lab activity titled "Build CMOS Logic Functions Using CD4007 Array" and to gain additional experience with complex CMOS gates. Specifically, you will learn how to combine CMOS transmission gates and CMOS inverters to build transmission gate exclusive-OR (XOR) and XNOR logic functions.

Background

To construct the logic functions in this lab activity, you will be using the CD4007 CMOS array and discrete NMOS and PMOS transistors (ZVN2110A NMOS and ZVP2110A PMOS) from the ADALP2000 analog parts kit. The CD4007 consists of three pairs of complementary MOSFETs, as shown in Figure 1. Each pair shares a common gate (pins 6, 3, and 10). The substrates of all PMOSFETs are common (positive supply Pin 14), as well as those of the NMOSFETs (ground Pin 7). For the left pair, the NMOS source

terminal is tied to the NMOS substrate (Pin 7), and the PMOS source terminal is tied to the PMOS substrate (Pin 14). The other two pairs are more general-purpose. For the right pair, the drain terminal of the NMOS is tied to the drain terminal of the PMOS on Pin 12.

The CD4007 is a versatile IC with many uses. For example, a single CD4007 can be used to make three inverters, an inverter plus two transmission gates, or other complex logic functions such as NAND and NOR gates. Inverters and transmission gates are particularly useful for building transmission gate XOR and XNOR logic functions. The schematic symbols for XOR and XNOR logic gates are shown in Figure 2.
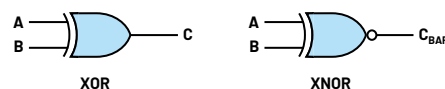
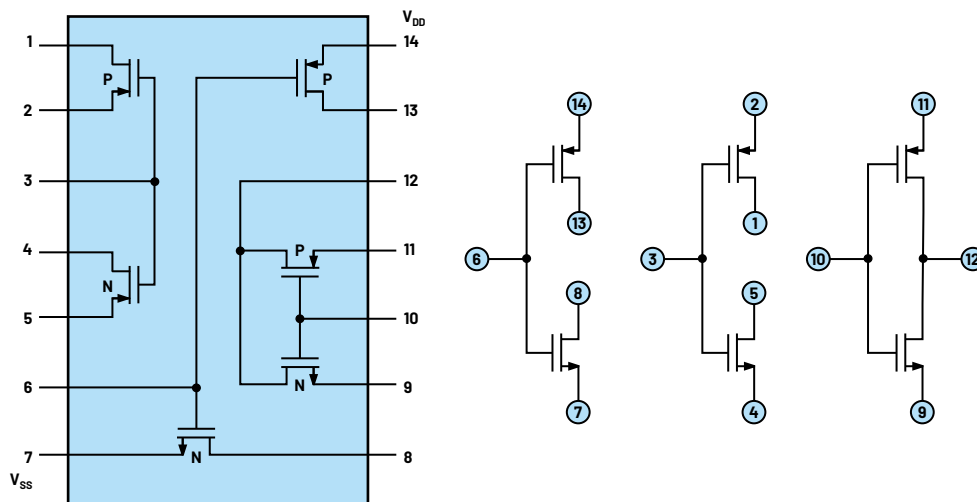*Figure 2. XOR and XNOR schematic symbols.*
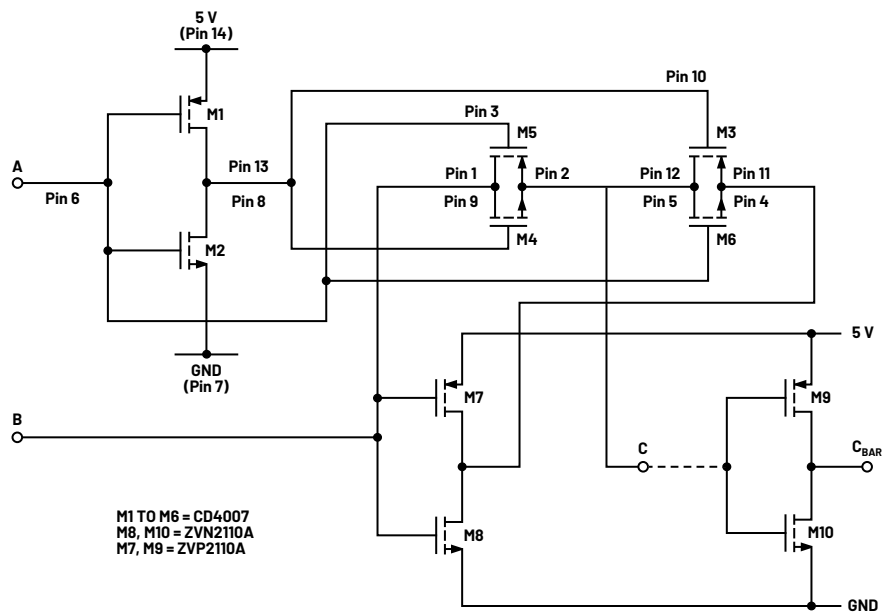
Figure 1. A CD4007 functional diagram.
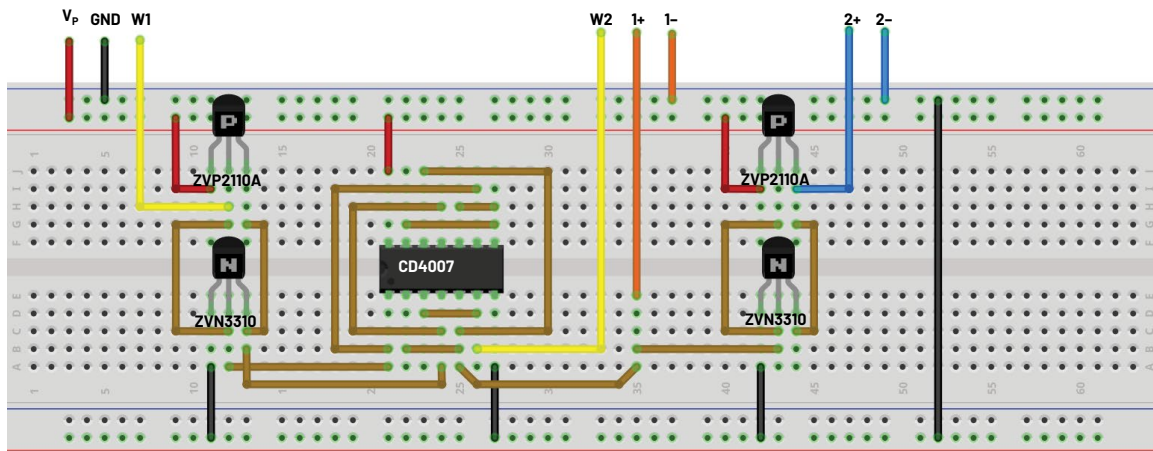
Figure 3. XOR and XNOR gate.

Figure 4. XOR and XNOR gate breadboard circuit.

Static Discharge

The CD4007, like many CMOS integrated circuits, is easily damaged by static discharge. The CD4007 includes diodes to protect it from static discharge, but it can still be damaged if it is not handled carefully. Normally, one would use antistatic mats and wrist straps when working with static sensitive electronics. However, you may not have those when working at home outside a formal lab environment. A low budget way to avoid static discharge is to ground yourself before touching an IC. Discharging any built-up static charge before handling a CD4007 will help ensure that you do not have a broken chip halfway through the lab.

Materials

▸ ADALM2000 Active Learning Module
▸ Solderless breadboard
▸ One CD4007 (CMOS array)
▸ Two ZVN2110A NMOS transistors
▸ Two ZVP2110A PMOS transistors

Directions

We will now combine the double-pole, single-throw (SPDT) transmission gate switch and two CMOS inverters to build an XOR gate (and XNOR) as shown in Figure 3. The two transmission gates work in tandem to realize a selector operation. Depending on the state of the A input, either Input B or the inverted version of Input B appears at the C (XOR) output. Two other inverters, M9 and M10, invert C to produce the C_{BAR} (XNOR) output.

Build the XOR/XNOR circuit shown in Figure 3 on your solderless breadboard. Use the CD4007 CMOS array for devices M1 to M6 and one ZVN2110A NMOS and ZVP2110A PMOS for each of the two inverter stages: the M7 and M8 stage and the M9 and M10 stage. Use the fixed 5 V power supply from the ADALM2000 to power your circuit.

There are two logic inputs A and B to the circuit. The noninverting XOR output is at Node C and an inverting version of the output is at Node C_{BAR} to form the XNOR function.

Hardware Setup

Configure both AWG outputs as DC sources for the first steps of the lab. The scope channels are to be used to monitor the inputs and outputs of the circuit as needed. The fixed +5 V power supply is to be used to power your circuit. The fixed –5 V supply should be disabled during this lab.

Procedure

Connect Pin 6, which serves as the A input, to AWG1. Connect pins 1 and 9, which serve as the B input, to the output of AWG2. Connect pins 2, 5, and 12, which serve as the C output, to Scope Channel 1. Connect the drain terminals of M9 and M10, which serve as the C_{BAR} output, to Scope Channel 2. Be sure to turn on the fixed 5 V power supply.

First, apply logic low to A by opening the AWG control screen and setting AWG1 to 0 V DC. Apply logic low to the B input by setting AWG2 to 0 V DC.
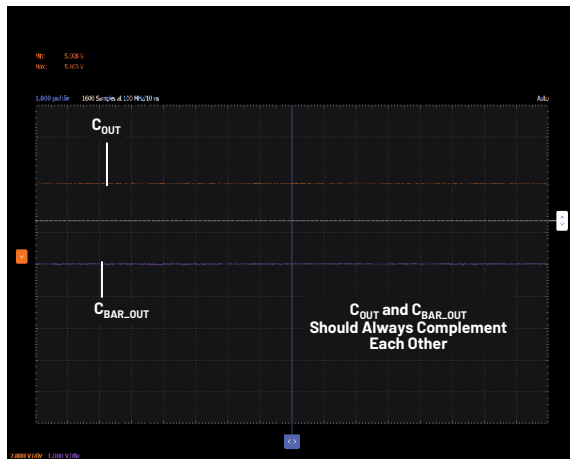

Figure 5. C_{OUT} and C_{BAR} output.

Observe the C output of the gate on Scope Channel 1. A steady DC voltage should appear on the scope screen.

Now configure both AWG channels as square waves with 5 V amplitudes peak-to-peak and 2.5 V offsets (0 V to 5 V swings). Set AWG1 to a frequency of 1 kHz and AWG2 to a frequency of 2 kHz or twice AWG1. Be sure to set the AWGs to run synchronously.

Observe both the C output and the C_{BAR} output on the scope screen with respect to the signals at the A and B inputs.

Next, set AWG2 to the same 1 kHz frequency as AWG1 but set the phase of AWG2 to 90°. Observe both the C output and the C_{BAR} output on the scope screen with respect to the signals at the A and B inputs.

XOR Gate as a Phase Detector

A phase detector or phase comparator is a logic circuit that generates an analog output voltage signal, which represents the difference in phase between two logic signal inputs. It is a central element of a phase-locked loop (PLL). Detecting the phase relationship between signals is an important functional block in many systems, such as motor control, radar, telecommunication, demodulators, and servo mechanisms.

A phase detector for square wave signals can be made from an XOR logic gate. When the two signals being compared are completely in-phase—that is, phase difference is 0°—the XOR gate's output will have a constant level of zero. When the two signals differ in phase by 10°, for example, the XOR gate's output will be high for 10/180th or 1/18th of a cycle, the fraction of a cycle during which the two signals differ in value. When the signals differ by 180°, that is, one signal is high when the other is low, and vice versa, the XOR gate's output remains high throughout each cycle.

When an XOR gate phase detector is used in a PLL system, it generally locks near a 90° phase difference in the middle of the phase detection range. At 90°, the XOR has a 50% duty cycle square wave output at twice the frequency of the input. The square wave changes duty-cycle in proportion to the phase difference of the two input signals. Passing the output of the XOR gate through a low-pass filter results in an analog voltage that is proportional to the phase difference between the two signals. It requires inputs that are symmetrical square waves. If the duty cycle of one input is slightly different than the duty cycle of the other, the low-pass filtered output will have an offset from the ideal middle of the range at 90° of phase difference.

Directions

Add the RC low-pass filter shown in Figure 6 to your XOR breadboard circuit. Connect Scope Channel 1 to the output of the RC filter.
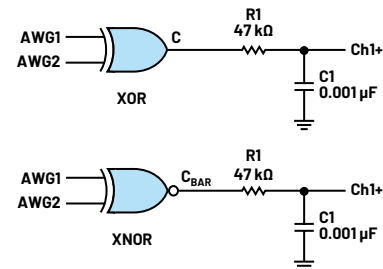

Figure 6. An XOR gate phase detector.

Hardware Setup

Configure both AWG channels as square waves with 5 V amplitudes peak-to-peak and 2.5 V offsets (0 V to 5 V swings). Set both AWG1 and AWG2 to a frequency of 1 kHz. Also be sure to start with the phase of both AWG1 and AWG2 set to 0°. Be sure to set the AWGs to run synchronously.

Procedure

Connect Scope Channel 1 to the output of the RC filter at C1 to observe the filtered (DC) output of the phase detector. Connect Scope Channel 2 to the output C of the XOR gate to observe the pulse width of the output of the logic gate.

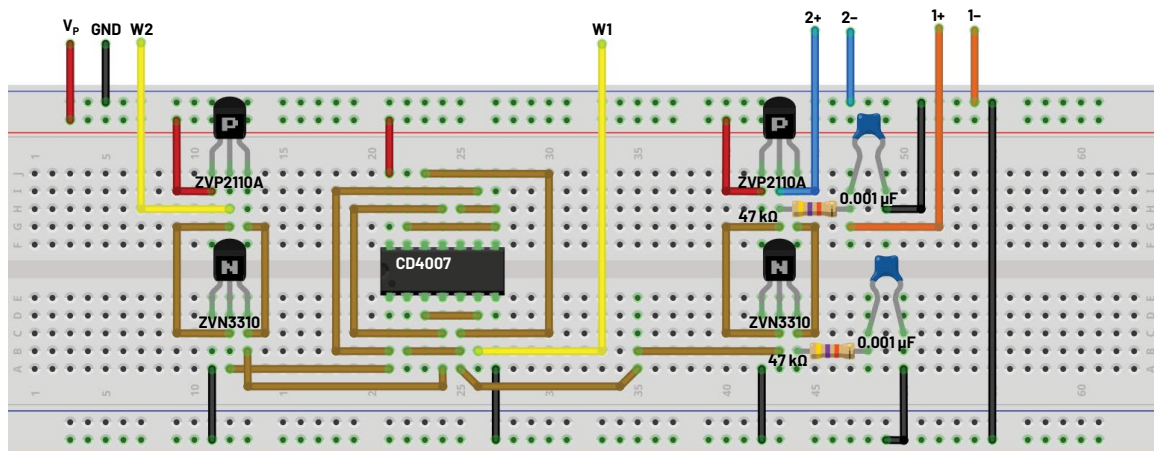A Scopy plot example is presented in Figure 8.

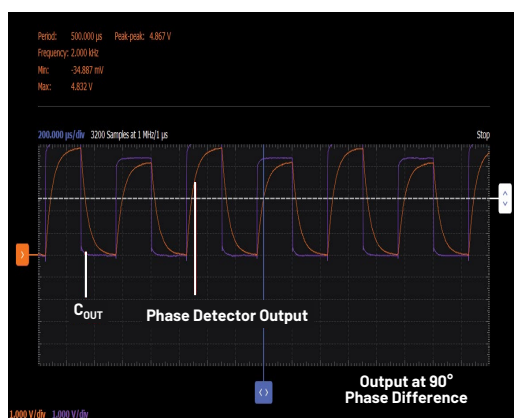*Figure 7. An XOR gate phase detector breadboard circuit.*

Figure 8. An XOR gate phase detector sample output.

Alternate Component Choices

The pair of inverters made using the four individual NMOS and PMOS transistors (ZVN2110A and ZVP2110A) could also be constructed from a second CD4007 IC or CMOS inverters from a hex inverter IC such as a 74HC04 or CD4049. The CD4066 quad SPST switch could also serve as an alternative to the switches built from the CD4007.

Question

1. For the circuit in Figure 3, fill in the table below by setting AWG1 and AWG2 to logic high (5 V) and low (0 V).

Table 1. Output Values for Each Combination of Inputs (A and B)

Input A	Input B	Output C	Output C_{BAR}
0	0		
1	0		
0	1		
1	1		

You can find the answer at the StudentZone blog.

About the Author

Antoniu Miclaus is a system applications engineer at Analog Devices, where he works on ADI academic programs, as well as embedded software for Circuits from the Lab®, QA automation, and process management. He started working at ADI in February 2017 in Cluj-Napoca, Romania. He is currently an M.Sc. student in the software engineering master's program at Babes-Bolyai University and he has a B.Eng. in electronics and telecommunications from Technical University of Cluj-Napoca.

About the Author

Doug Mercer received his B.S.E.E. degree from Rensselaer Polytechnic Institute (RPI) in 1977. Since joining Analog Devices in 1977, he has contributed directly or indirectly to more than 30 data converter products and holds 13 patents. He was appointed to the position of ADI Fellow in 1995. In 2009, he transitioned from full-time work and has continued consulting at ADI as a fellow emeritus contributing to the Active Learning Program. In 2016, he was named engineer in residence within the ECSE department at RPI.

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