Improved Data Acquisition Using a New Monolithic Dual-ADC Front End

by Albert O'Grady

Designers of measurement systems such as temperature-compensated weigh scales and RTD instrumentation, can perform their task more effectively with a new single-chip A/D converter/analog front end. The AD7719 features the high resolution inherent in sigma-delta converters; and for augmented throughput, contains *two* ADCs (24- and 16-bit resolution), permitting simultaneous parallel conversions of two input variables without the latency inherent in analog multiplexing schemes. It employs a signal-chopping approach that provides signal conditioning with stable gain and minimal offset, coupled with built-in calibration, to eliminate the need for calibration in the field. It conveniently includes a matched pair of current sources, to simplify transducer excitation and improve measurement accuracy when using resistive transducers. Other useful features include circuitry that can be switched off and low-side switches that can be used to conserve power when converters or transducer power are not being used, plus a digital I/O port for monitoring and control of external devices.

The AD7719, a complete analog front end for low-frequency measurement applications, is the newest addition to the Analog Devices family of high-resolution, low-bandwidth, sigma-delta converters. It builds on the experience gained from employing the previous generations of sigma-delta converters in applications ranging from weigh scales to portable instrumentation, pressure, temperature and transducer measurement, smart transmitters, liquid/gas chromatography, and industrial process control. The enhanced features mentioned above (see Figure 1) address many issues that commonly recur in the design of such high-performance data acquisition systems.

The AD7719 contains two independent, high-resolution, sigma-delta ADCs. Each analog-to-digital conversion is accomplished by a second-order sigma-delta modulator with a programmable sinc^3 filter. In addition, it makes available switchable matched 200 µA excitation current sources, low-side power switches, digital I/O port, and a temperature sensor. The 24-bit main channel, with a programmable-gain amplifier (PGA) that has gains from 1 to 128, accepts fully differential, unipolar, and bipolar input signals with ranges up to 1.024 × REFIN1 volts. The reference input is differential and can provide ratiometric conversion. The main analog input channel can be internally buffered to provide a very high input impedance; this allows input signals to be applied directly from a transducer without the need for external signal conditioning. The 16-bit auxiliary channel is unbuffered and offers an input signal range of REFIN2 or one-half REFIN2.

The device operates from a 32,768 Hz (32K) crystal, with an on-board PLL generating all of the required internal operating frequencies. The output data rate from the AD7719 is software

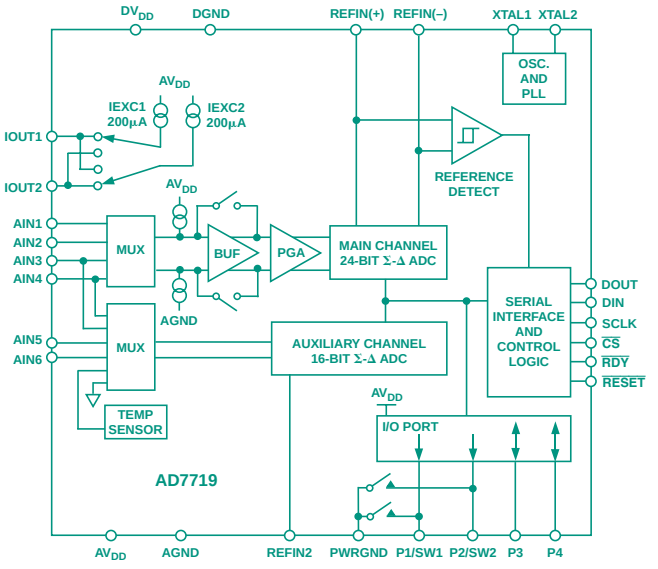

Figure 1. AD7719 functional block diagram.

programmable. This allows the digital filter notches to be placed at user-defined frequencies. For example, with a programmed update rate of 19.8 Hz, rejection notches at 50 Hz and 60 Hz can be achieved simultaneously.

The peak-to-peak resolution depends on the programmed gain and the output data rate. The device operates from a single 3 V or 5 V supply. When operating from a 3 V supply, the power dissipation is 4.5 mW with both ADCs continuously in use. Dissipation can be reduced by disabling one or both ADCs when appropriate. The AD7719 is available housed in space-saving 28-lead SOIC and TSSOP packages.

Signal-Processing Chain

The ADCs employ sigma-delta conversion to realize up to 24 bits of no-missing-codes performance. The sigma-delta modulator converts the sampled input signal into a digital pulse train whose duty cycle contains the digital information. A sinc^3 programmable low-pass filter then decimates the modulator output data stream to give a valid data conversion result at programmable output rates from 5.35 Hz (186.77 ms period) to 105.03 Hz (9.52 ms). A chopping scheme is employed to minimize ADC channel offset, gain, and drift errors. A block diagram of the main ADC input channel is shown in Figure 2. The signal chain for the auxiliary ADC is similar to that of Figure 2 but omits the buffer and PGA blocks.

The sampling frequency of the modulator loop is many times higher than the bandwidth of the input signal (oversampled). The integrator in the modulator shapes the quantization noise (which results from the analog-to-digital conversion) so that the noise is concentrated near one-half of the modulator frequency. The output of the sigma-delta modulator feeds directly into the digital filter, which band-limits the response to a frequency significantly lower than one-half of the modulator frequency. In this manner, the 1-bit output of the comparator is translated into a band-limited, low noise output from the ADC. The filter's cutoff frequency and decimated output data rate are programmable via the sinc-filter (SF) control word loaded to the filter register.

The alternating digital output values that result from the input chopping are summed in a final summing stage to average out dc offsets and low-frequency noise. Each output word from the filter is summed and averaged with the previous filter output to produce

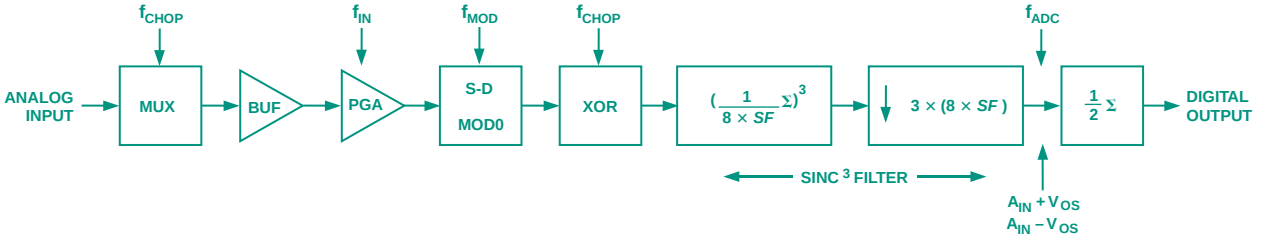

Figure 2. Main ADC signal chain.

a new valid output result to be written to the ADC data register. The resulting very low dc offset and offset- and gain-drift specifications are quite beneficial in applications where drift, noise rejection, and optimum EMI rejection are important.

Besides reduction of quantization noise, the digital filter also provides normal-mode rejection of 100 dB at 50 Hz and 60 Hz (±1 Hz) for respective filter control-word settings of 82 and 68. For applications requiring substantial rejection at both 50 Hz and 60 Hz, the filter's response at the default programmed setting of 69 (data-update rate of 19.8 Hz) has notches close to both frequencies, with >100 dB rejection at 60 Hz and >60 dB at 50 Hz, as shown in Figure 3.

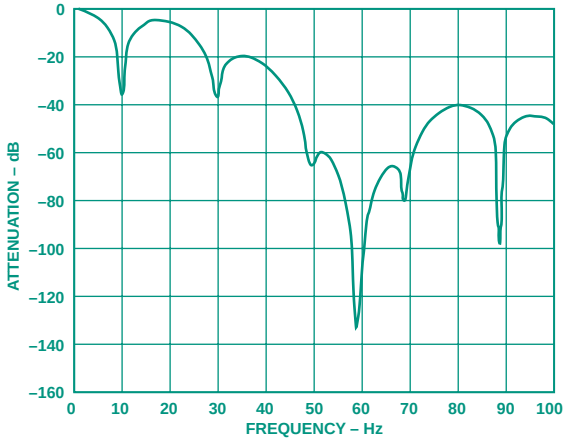

Figure 3. Filter profile showing simultaneous 50 Hz and 60 Hz rejection nulls with sinc^3 filter control word of 69.

Typical Applications

The AD7719 provides a complete analog front end for implementing low frequency measurements using temperature-, pressure-, and other transducers. In weigh-scale applications, for example, a secondary variable—such as temperature—may need to be monitored in addition to the primary variable from the bridge transducer in order to compensate for variations of bridge properties with temperature.

Traditionally, sigma-delta ADCs have used a single converter with integrated multiplexer on the front end to measure multiple input variables. This means that the end user has to switch channels on the front end to measure the secondary variable; as a consequence, measurement speed suffers from the settling time and latency associated with the digital filter when switching input sources. In systems where the sigma-delta ADC uses a second-order modulator and a third-order digital filter, the output settling time to a step input is three times the data rate in order to fully flush the digital filter of all data pertaining to the previous channel. This can greatly reduce the system throughput achievable in these applications.

The AD7719 overcomes this problem by incorporating two independent ADC channels, converting in parallel. The primary variable and the secondary variable are converted simultaneously, and output data from both measurements is available in parallel, thus avoiding the latency associated with multiplexed data acquisition systems. In addition, the on-chip current sources can be used to excite temperature sensors, such as thermistors or RTDs for temperature monitoring.

A second commonly encountered issue in low-power, battery-operated weighing systems is the unnecessary consumption of power in the front-end transducer when in standby mode. The AD7719's on-chip low-side power switches can address this issue by removing the power to the transducer when in low-power mode, thus offering substantial power savings.

Another issue with weigh-scale applications concerns calibration: when and how often should it take place? Because the AD7719 is factory-calibrated, and the signal chain uses a chopping scheme in its implementation, the gain and offset drift are reduced to a minimum, thereby eliminating the need for calibration in the field. This is a key performance advantage when the AD7719 is used in weigh-scale applications (Figure 4).

In the circuit of Figure 4, the main channel monitors the bridge by transducer, and the secondary channel monitors temperature by means of a thermistor. The bridge transducer's differential output terminals (OUT+ and OUT–), are connected to differential input terminals, AIN1 and AIN2. A typical bridge with a sensitivity of 3 mV/V will produce a rated full-scale output of 15 mV when excited with a 5 V excitation source. The excitation voltage for the bridge can be used to directly provide the reference for the ADC via a suitable resistor divider, which will allow the full dynamic range of the input to be utilized. Because this implementation is fully ratiometric, variations in the excitation voltage do not introduce errors in the system. The choice of resistance values, 20 kΩ and 12 kΩ, as shown in the diagram, gives a 1.875 V reference voltage for the AD7719 when the excitation voltage is 5 V. With the main channel programmed for a gain of 128, the full-scale 15 mV input span corresponds to the full output span from the transducer. A key requirement in weigh-scale applications is to reject ac power-mains frequency components (50 Hz and 60 Hz) as much as possible. Simultaneous 50 Hz and 60 Hz rejection can be obtained by programming the AD7719 for an output data rate of 19.8 Hz. 13-bit peak-to-peak resolution will be achieved with the AD7719 configured for a gain of 128 with a 19.8 Hz update rate. The peak- to-peak resolution can be increased by reducing the update rate or by performing extra digital filtering in the controller.

Temperature is measured using a thermistor and the AD7719's secondary channel. Thermistors, high-temperature-coefficient

electrical circuit elements formed with semiconductor material, are available with negative or positive temperature coefficients (NTC or PTC). An NTC thermistor acts like a resistor with a temperature coefficient of typically –3%/°C to –5%/°C. Thermistors offer the benefits of high stability, precision, small size, and compatibility at a competitive price in many applications. They have fast response and are among the highest-sensitivity temperature transducers available. The operating temperature range of the circuit of Figure 4 is determined by the choice of thermistor. Using a 1K7A1 thermistor from Betatherm, with a nominal resistance of 1 kΩ at 25°C, and employing the 200 µA excitation-current source, the operating temperature range is –26°C to +70°C.

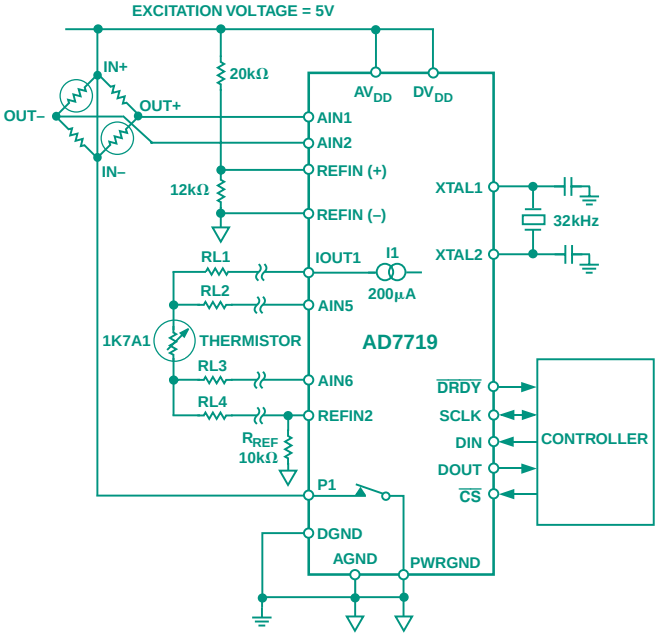

Figure 4. Weigh-scale application takes advantage of many features of the AD7719.

In this application, the same 200 µA current source that excites the thermistor also generates the reference voltage for the AD7719. As a result, variations in the excitation current do not affect performance, and the configuration provides fully ratiometric conversion. The most common wiring arrangement in these applications is a 4-wire force/sense configuration in order to reduce the effects of lead resistances on system performance. Although the lead resistance of the drive wires shifts the common-mode voltage, it does not degrade the performance of the circuit. Lead resistance of the sense wires is immaterial, as no current flows in these wires due to the high input impedance of the AD7719 analog inputs. However, the reference-setting resistor must have a low temperature coefficient to avoid errors in the reference voltage with temperature changes. By configuring the secondary channel on the AD7719 for a 19.8 Hz update rate, 16-bit peak-to-peak performance can be obtained.

Another application that makes good use of the matched current sources on the AD7719 is where a 3-wire RTD is used for precision temperature measurement, in the manner shown in Figure 5*. In 3-wire configurations, the lead resistances would cause errors if a single current source were used, as the 200 µA excitation current, flowing through RL1 and RL3, will develop a voltage drop across RL1, which adds to the RTD voltage and causes an error between AIN1 and AIN2.

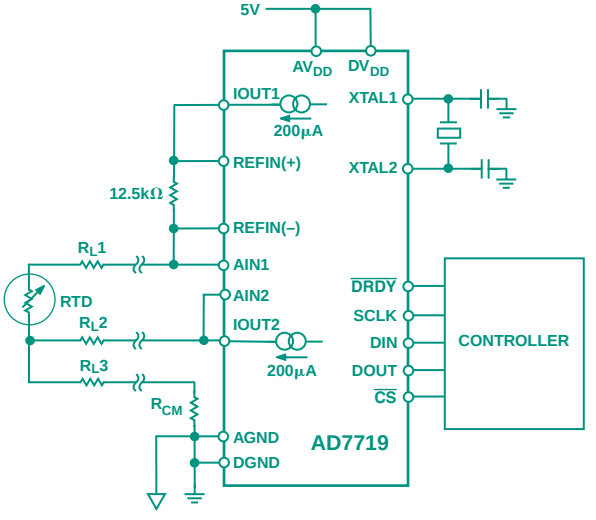

Figure 5. 3-wire RTD measurement using the AD7719.

In the scheme shown in Figure 5 however, the second current source is used to null out this error by furnishing an equal and opposite compensating current, IOUT2, through RL2, which produces an equal voltage drop in the opposite direction. This current adds to IOUT1 and flows harmlessly to ground through R3 and any common-mode resistance, producing a common-mode voltage, which is rejected by the differential inputs.

This analysis assumes that RL1 and RL2 are equal, since the leads would normally be of the same material and of equal length, and that the common-mode voltage developed by the sum of the currents is within the common-mode range of the ADC. The current from IOUT1 is also used to develop a reference voltage for the AD7719, across the 12.5 kΩ resistor, as shown, and applied to the differential reference inputs of the AD7719. This scheme ensures that the analog input voltage span remains ratiometric to the reference voltage. Any errors in the analog input voltage, due to the temperature drift of the RTD's current source, is compensated for by the variation in the reference voltage. The two RTD current sources are typically matched to better than 1%. The voltage compliance on either current source is AV_{DD} – 0.6 V.

* See the article, "Transducer/Sensor Excitation and Measurement Techniques," in *Analog Dialogue* 34-05 (2000).