X-Amp,™ A New 45-dB, 500-MHz Variable-Gain Amplifier (VGA) Simplifies Adaptive Receiver Designs

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INTRODUCTION

Wireless communications equipment design usually starts with strategic *signal-chain* definition and analysis. *Noise Figure* (NF), *linearity*, *distortion*, and *dynamic range* all need to be considered at an early stage in the product development cycle to properly identify component specifications for each element in the signal path. Signal-chain budget analysis allows designers to quickly select components, analyze, and compare the performance of design architectures being considered. The challenge is greater in mobile communications systems, where special attention needs to be focused on the *spectral selectivity*, *linearity*, and *noise mechanisms* associated with RF and IF signal blocks.

Receivers can be designed to provide adaptive sensitivity to incoming signal strength by employing variable gain at the lower IF frequencies, where it is easier to manipulate the signal of interest. Most spectral grooming (frequency shaping and filtering) tends to be implemented at the lower IF frequencies where very narrow-band pass filters can be easily realized through the use of SAW devices, crystals, and passive lumped-element RLC filter networks. After precise channel selection, automatic gain-control (AGC) circuitry can be employed to scale the received signal to a desired level. The use of AGC yields a receiver design whose sensitivity varies, based on received signal strength. Adaptive sensitivity reduces the effects of distance inherent in fading-channel mobile environments. High-performance variable-gain amplifiers are often necessary to provide the needed dynamic range and noise performance.

Background

Variable gain amplifiers (VGAs) have been used in a variety of remote sensing and communications equipment for more than a half century. Applications ranging from ultrasound, radar and lidar, to wireless communications—and even speech analysis—have utilized variable gain in an attempt to enhance dynamic performance. Early designs achieved gain selection by switching in fixed-gain amplifier stages to adjust receiver sensitivity in a binary fashion. Later implementations used step attenuators followed by fixed-gain amplifiers to achieve a wider range of discrete gain control. Modern designs achieve continuous voltage controlled gain, using analog techniques, by such means as voltage-variable attenuators (VVAs), analog multipliers, and gain interpolators.

A variety of architectures are commonly used to provide both continuous and discrete variable-gain control. Applications such as automatic gain control often require *continuous* analog gain control. The most straightforward designs utilize analog multipliers followed by fixed-gain buffer amplifiers. Such designs often involve

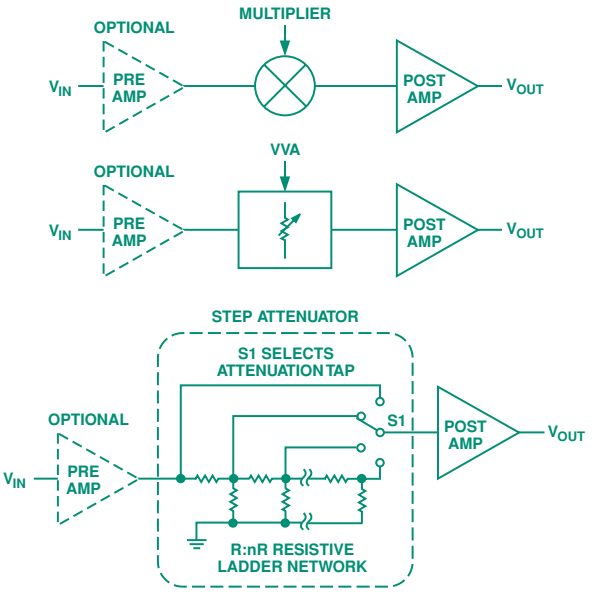

Figure 1. Typical variable-gain architectures.

a nonlinear gain-control function that requires calibration. Additionally, the multiplier cores suffer from temperature and supply voltage dependencies that can result in poor gain-law accuracy and stability, as well as unacceptable high-frequency gain variation. Designs that use preamplifier/attenuator/post-amplifier architectures can provide low-noise operation and good bandwidth, but tend to have quite low input third-order intercepts (IIP3), limiting their ability to perform in high-dynamic-range receivers.

Another class of solutions utilizes voltage-variable attenuators, followed by fixed-gain post-amplification. VVAs can provide an accurate attenuation transfer function that is linear in dB, but it is often necessary to cascade multiple VVAs in order to provide adequate attenuation range. The cascading results in an increased sensitivity to variations of the attenuation transfer function. It is sometimes necessary to preamplify the signal to buffer the signal source from the loading effects of the VVA, as well as to decrease the attenuator's influence on noise figure. The high gain required to yield a low-noise figure results in a decreased input third-order intercept.

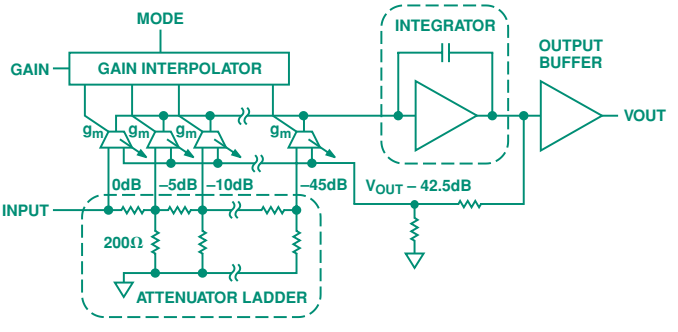

Figure 2. Architecture of the AD8367 X-Amp VGA.

The AD8367 X-AMP VGA with AGC

The X-AMP architecture, originating ten years ago with the Analog Devices AD600 and AD602, (*Analog Dialogue* 26-2, 1992), permits a linear-in-dB gain-control function that is essentially independent of temperature. It comprises a resistive ladder network, along with a highly linear amplifier and interpolator stage, to provide a continuous linear-in-dB gain-control function. The AD8367

(Figure 2) is the latest generation of X-AMP VGAs. Its design is implemented on a new eXtra Fast Complementary Bipolar process (XFCB2.0) that provides moderate gain out to hundreds of MHz and improved linearity at higher frequencies than heretofore available with conventional semiconductor processing.

As Figure 2 shows, the input signal is applied to a ground-referenced 9-stage *R-nR* resistive ladder network, designed to produce 5-dB steps of attenuation between tap points. Smooth gain control is achieved by sensing the tap points with variable-transconductance (g_m) stages. Depending on the gain-control voltage, an interpolator selects which stages are active. For example, if the first stage is active, the 0-dB tap point is sensed; if the last stage is active, the 45-dB point is sensed. Attenuation levels that fall between tap points are achieved by having neighboring g_m stages active simultaneously, creating a weighted average of the discrete tap-point attenuations. In this manner, a smooth, monotonic, linear-in-dB attenuation function with very precise scaling is synthesized. The ideal linear-in-dB transfer function can be expressed as:

$$Gain(dB) = M_Y \times V_{GAIN} + B_Z \quad (1)$$

where

M_Y is the gain scale (slope) usually expressed in dB/V, typically 50 dB/V (or 20 mV/dB)

B_Z is the gain intercept in dB, typically –5 dB, the extrapolated gain for $V_{GAIN} = 0\,V$

V_{GAIN} is the gain-control voltage

The AD8367's basic connection outline, gain transfer function, and typical gain-error pattern are illustrated in Figure 3, showing the gain transfer function's slope of 50 dB/V and –5-dB intercept over a gain-control voltage range of 50 mV ≤ V_{GAIN} ≤ 950 mV. The device allows the gain slope to be reversed by a simple pin-strap of the MODE pin. The inverse gain mode is convenient in automatic gain control (AGC) applications, where the gain-control function is derived from an error integrator, which compares the detected output power to a predetermined set-point level. A square-law detector and the error integrator, integrated on-chip, allow the device to be used as a self-contained AGC subsystem.

A typical stand-alone AGC circuit is shown in Figure 4, along with its time-domain response to a 10-dB input voltage step. In this example the signal input is a 70-MHz sinusoid, and its input is step modulated from –17 dBm to –7 dBm (referred to 200 Ω). The output signal power is measured as a voltage by the internal square-law detector and compared to an internal 354-mV rms reference. The output of the detector is a current, which is integrated using an external capacitor, C_{AGC}. The voltage that is developed across the C_{AGC} capacitor drives the GAIN pin to reduce or increase the gain. The loop is stabilized when the output signal level's rms value becomes equal to the internal 354-mV reference. When the input signal is less than 354 mV rms, the DETO pin sinks current which reduces the voltage at the GAIN pin. As the input signal increases above 354 mV rms, the DETO pin sources current causing the voltage at the GAIN pin to increase. The inverse gain mode is required in this application to ensure that the gain decreases when the input signal's rms value exceeds the internal reference. The resulting voltage applied to the GAIN pin, V_{AGC}, can be used as a received-signal-strength indication (RSSI), representing the input signal strength as compared to a 354-mV rms reference. For a sinusoidal waveform this results in a 1-V p-p output signal for a 200-Ω load.

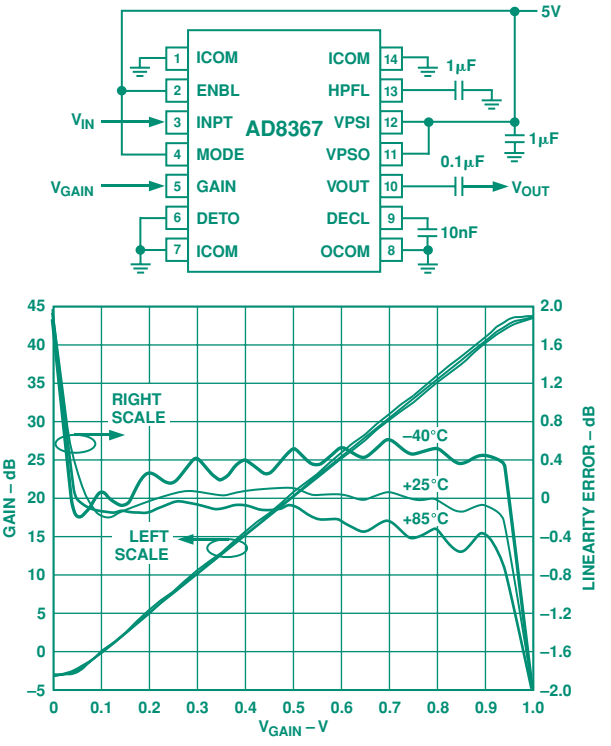

Figure 3. Basic AD8367 VGA application circuit and gain-control transfer function, showing typical errors at various temperatures.

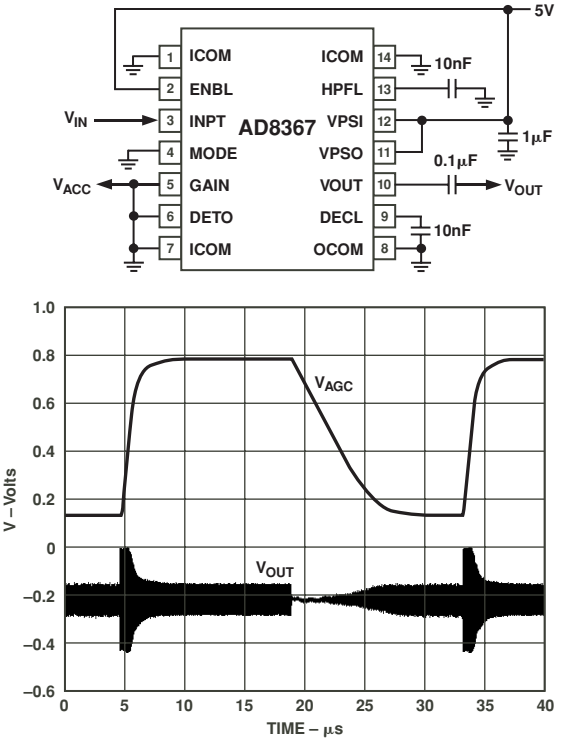

Figure 4. Basic AD8367 AGC application circuit and time-domain response at 70 MHz.

Signal Chain Analysis

A modern superheterodyne architecture is depicted in Figure 5. The AD8367 is used in the *receive* (Rx) path to adaptively adjust overall receiver gain as the RF signal level changes. In the *transmit* (Tx) path, the AD8367 is used in conjunction with an RF power detector to maintain a desired output power level.

Considering the receive path, the overall sensitivity and dynamic range can be assessed using signal-path budget analysis. For this example a PCS-CDMA signal was selected, using a 1-MHz noise bandwidth. Working backwards from the output of the AD8367 IF VGA, the input sensitivity and dynamic range can be analyzed. Figure 6 represents a detailed budget analysis from the receiver input to the output of the IF VGA.

In the example above, the AD8367 controls received signal levels prior to the I & Q demodulator. The AD8367 is an example of a VGA that uses variable attenuation followed by a post-gain amplifier. This style of VGA will exhibit essentially a constant OIP3 and a noise figure that varies with gain setting. The AD8367 provides minimum noise figure at maximum gain and maximum input third-order intercept at minimum gain. This unique combination allows for dynamic control of a receiver's sensitivity and input linearity, based upon received signal strength.

AD8367 is characterized over temperature from –40°C to +85°C and is packaged in a 14-lead thin-shrunk small-outline package (TSSOP). It operates on a single 3-V to 5-V supply. The device has a –3-dB operating bandwidth of 500 MHz; and its data sheet provides detailed specifications at common IF frequencies—such as 70 MHz, 140 MHz, 190 MHz, and 240 MHz. If you are reading the PDF or printed version of this article, please visit www.analog.com to download the data sheet or to request samples. The AD8367 is normally available from stock, and an evaluation board is also available.

Acknowledgements

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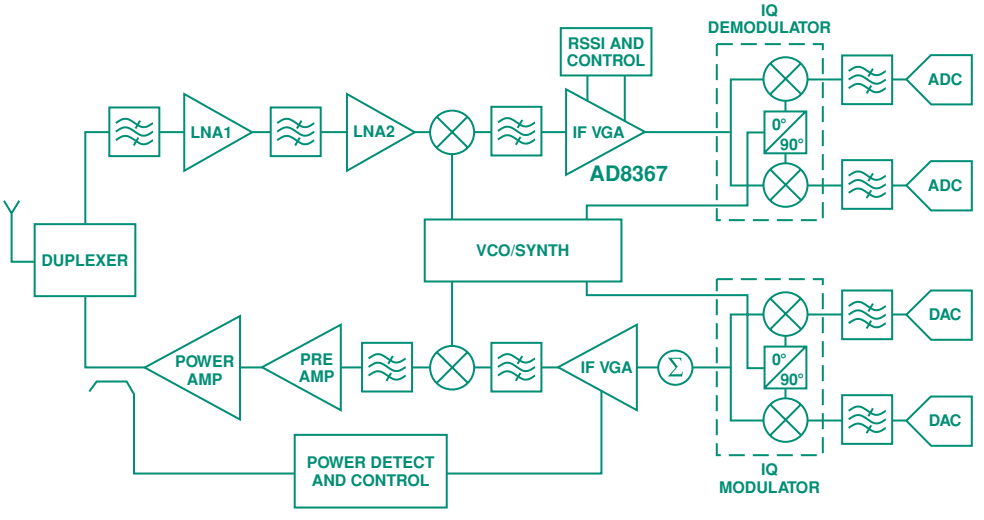

Figure 5. Superheterodyne architecture using VGAs for IF level control. VGAs are used in the intermediate frequency stages to adjust overall receiver sensitivity adaptively and to control transmitted power levels.

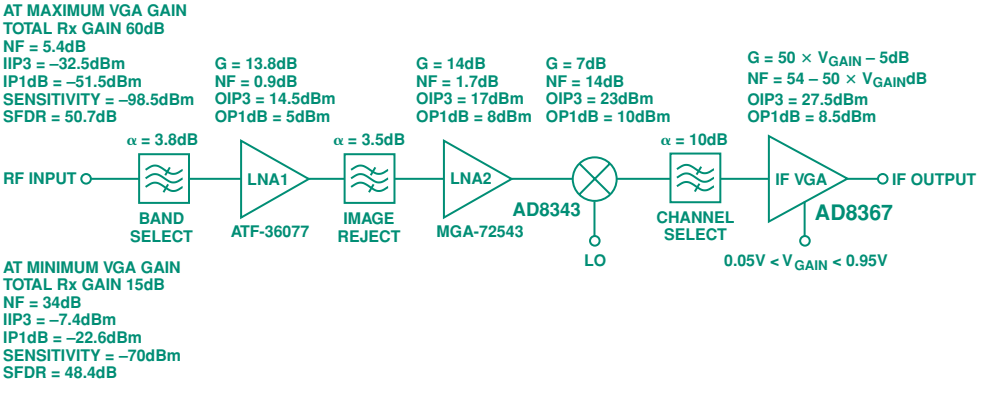

Figure 6. Rx Path Budget Analysis for 1900-MHz CDMA with a 70-MHz IF.