

# Analog Front End for 3G Femto Base Stations Brings Wireless Connectivity Home

By Thomas Cameron and Peadar Forbes

## INTRODUCTION

Imagine a device that can provide high-quality cellular phone reception within your home, allowing you and your family unlimited voice and data usage for a low monthly fee. A femto base station, usually referred to as a femtocell, provides all that and more. This small wireless device, which improves local wireless coverage when placed in a home or office, is poised to dramatically change the wireless infrastructure landscape.

Figure 1 illustrates the femtocell concept. While traditional base stations provide wide area coverage, a femtocell provides wireless coverage in a small area such as a residence. The femtocell routes mobile traffic to the network through the user's broadband Internet connection, thus offloading traffic from the radio network. The femtocell improves the capacity of the network, while reducing backhaul, power, and maintenance costs for the operator. It also enables operators to compete for services in homes that have limited signal coverage. In exchange for a subsidized femtocell, the operator adds an additional fee to the customer's monthly cellular plan. When in the femtocell zone, all mobile usage would be covered under the home billing plan, allowing unlimited voice and data usage in the home without incurring large monthly bills. The proximity of the femtocell enables a high quality link, while simultaneously reducing handset battery usage. The femtocell overcomes the limitation of 3G signals from the base station to penetrate walls, enabling high-speed access to mobile data services such as browsing the Internet, downloading music, and streaming video on the handset.

The femtocell, similar to a Wi-Fi router, is based on proven wireless infrastructure standards (UMTS, CDMA). Compatible with emerging standards, it provides an efficient, robust wireless link using operator-owned spectrum. Compatibility with existing handsets makes the connection transparent to the user. Unlike a macrocell network, which aggregates tens or hundreds of base stations onto the core network, a femtocell gateway must manage thousands or even millions of femtocell nodes.

Femtocells, which must provide the quality of service (QoS) expected from a base station at a cost similar to a handset, present unique challenges to the radio designer. The femtocell must provide both high-quality voice service and high-speed mobile data services (EVDO and HSPA) at a fraction of the cost of a

macrocell. In order to meet these challenges, the femtocell design must take advantage of low-cost manufacturing techniques and highly integrated circuits that minimize calibration and test time. Femtocells reside in the home, so they must be small, low cost, and user installed. Transmitting at low power—on the order of 100 mW—femtocells must be aware of the wireless environment to mitigate interference and meet regulatory requirements. 3G femtocells must monitor UMTS channels to detect base stations in the vicinity, as well as GSM channels to establish cells that might be appropriate for handover when a user leaves the femtocell zone.

The femtocell can be viewed as two distinct functions: the analog front end and the baseband processor. The front end, which is the topic of this article, converts the digital data stream into an RF signal in the *transmit* circuit, and vice versa in the *receive* chain. The front-end design entails trade-offs between integration and performance. Although discrete solutions can be tailored to provide the best performance, the cost would be prohibitive for a femtocell design. Conversely, a fully integrated solution may provide the lowest cost, but the performance may not be sufficient.

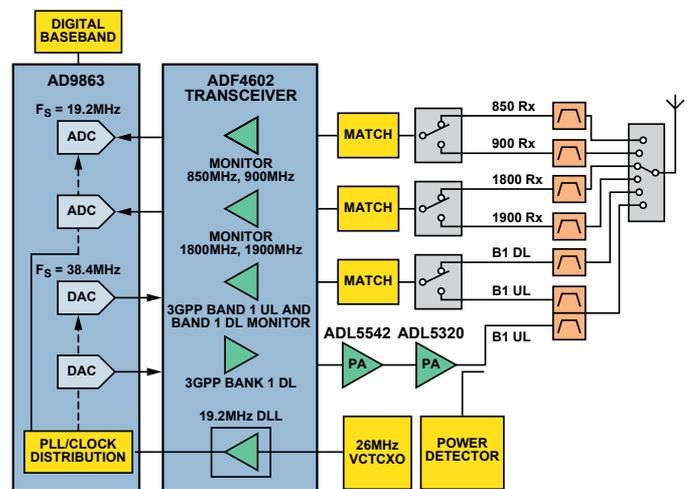


Figure 2. Femtocell analog front-end implementation based on ADI chipset.

Figure 2 illustrates a high-level block diagram of a femtocell designed to support local base station operation in UMTS band 1 as well as monitor signals in the 850-MHz, 900-MHz, 1800-MHz, 1900-MHz, and 2100-MHz bands. Together, the AD9863<sup>1</sup> mixed-signal front-end (MxFE<sup>®</sup>) baseband transceiver, ADF4602<sup>2</sup> integrated radio transceiver, ADL5542<sup>3</sup> and ADL5320<sup>4</sup> linear amplifiers, switches, filters, and other associated support circuitry form a compact, high-performance front end for the femtocell. A detailed description of the highlighted blocks follows.

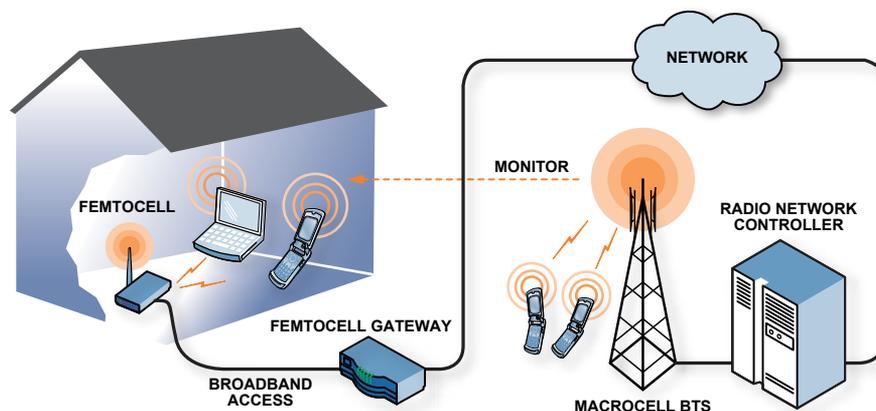


Figure 1. Femto base station compared to macro base station.

On the *transmit* side, the digital baseband feeds a 12-bit parallel data stream to the AD9863, which converts it to an analog I/Q baseband signal. The baseband signal is converted to RF by the ADF4602, amplified by the ADL5542 and ADL5320 gain stages, and sent to a duplexer. A power detector monitors the RF output. A single-pole, six-throw (SP6T) switch selects which *transmit* or *receive* monitoring chain is connected to the single antenna. This signal chain provides 13 dBm output power at the RF output connector, while meeting transmit ACLR specifications as defined in 3GPP standard TS25.104.

The *receive* chain includes surface acoustic wave (SAW) filters and SPDT switches for monitoring the main path. The matching blocks consist of a simple series/shunt inductor for each receive port. The ADF4602 has three receiver input pins: one for band 1, and one each for high- and low band monitoring functions. The band-1 *receive* function may be switched between 1960 MHz to receive the uplink signal and 2140 MHz to monitor the downlink frequency. The ADF4602 downconverts and filters the selected RF signal to a baseband I/Q signal. The baseband signal is sampled by the dual ADCs in the AD9863 and converted to dual 12-bit parallel bit streams for the digital baseband.

This functional partition provides the designer with flexibility, ensures high performance in the signal chain, and allows the data converter's speed and resolution to be chosen to fit the application's requirements. The ADI solution enables the designer to combine the analog front end with a commercially available baseband function, accelerating time to market of the femtocell design, while maintaining the benefit of future integration of ADI technology as the femtocell market matures.

### ADF4602 Integrated Radio Transceiver

The ADF4602, shown in Figure 3, is a 3G transceiver offering unparalleled integration and a feature set well-suited to high-performance 3G femtocells. The receiver, based on the direct-conversion architecture, is the ideal choice for highly integrated wideband CDMA (W-CDMA) receivers, reducing the bill of materials (BOM) by fully integrating all interstage filters. The *receive* baseband filters offer selectable bandwidth, enabling reception of both W-CDMA and GSM-EDGE radio signals. The selectable bandwidth, coupled with the multiband LNA input structure, allow GSM/EDGE signals to be monitored as part of a UMTS home base station.

The ADF4602 contains two fully integrated programmable frequency synthesizers for generation of *transmit* and *receive* local oscillator (LO) signals. The design uses a fractional-N architecture for low noise and fast lock-time. All necessary components, including loop filters, VCOs, and tank components, are fully integrated for both *transmit* and *receive* synthesizers. The VCOs run at twice the high-band frequency and four times the low-band frequency, minimizing VCO leakage power at the wanted frequency and the tuning range requirements of the VCO. The VCOs use a multiband structure to cover the wide operating frequency range. The design incorporates both frequency- and amplitude calibration to ensure that the oscillator is always operating at optimum performance. The fully self-contained calibrations, which occur during the 200- $\mu$ s PLL lock time, require no user inputs. The on-chip VCO outputs are fed to tuned buffer stages and then to the quadrature-generation circuitry. The tuned buffers ensure that minimum current and LO-related noise are generated in the VCO transport. The quadrature generators create the highly accurate phased signals required to drive the modulator and demodulator. Special precautions have been taken to provide the isolation demanded by frequency division duplex (FDD) systems between the *transmit* and *receive* chains.

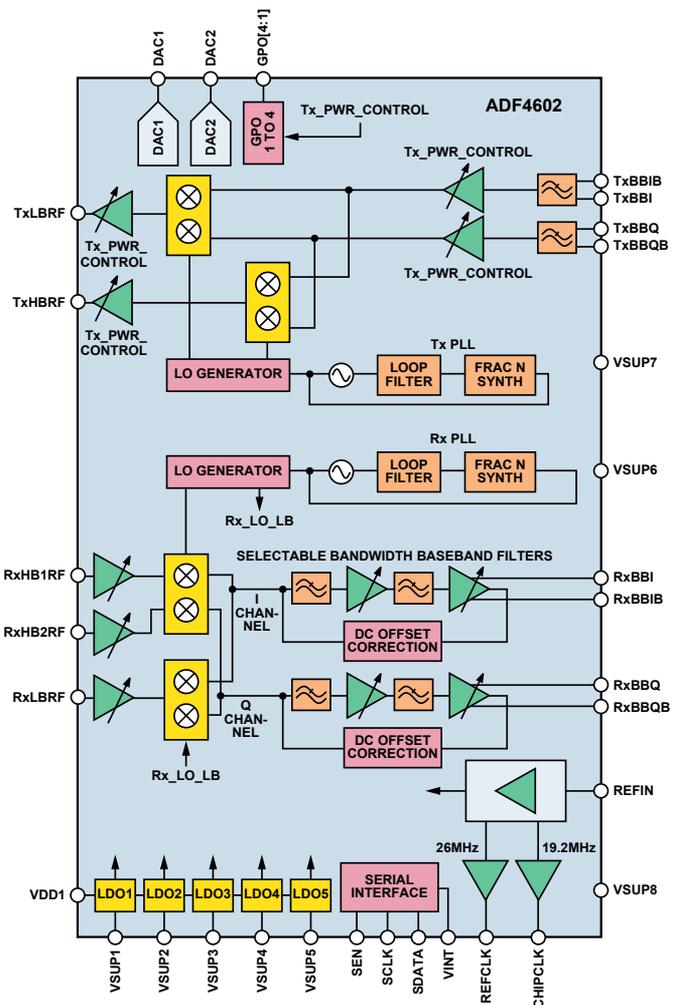


Figure 3. ADF4602 block diagram.

The receiver front-end includes three high-performance, single-ended, low-noise amplifiers (LNAs), allowing the device to support tri-band applications. Two are suitable for high-band operation from 1800 MHz to 2170 MHz, while one is suitable for operation from 824 MHz to 960 MHz. Interstage RF filtering is fully integrated, ensuring that external out-of-band blockers are suitably attenuated prior to the mixer stages. The single-ended 50- $\Omega$  input structure eases interfacing and reduces the matching components required for small footprint single-ended duplexers. The excellent device linearity ensures good performance with a large range of SAW- and ceramic filter duplexers.

High linearity demodulator circuits are used to convert the RF signal to baseband in-phase and quadrature components. Two demodulator sections are included: one optimized for the high-band LNA outputs and one optimized for the low band. The high-band- and low-band outputs are combined to drive directly into the first stage of the baseband low-pass filter, which reduces the largest blocking signals prior to baseband amplification. The receiver synthesizer section provides quadrature LO drive to the mixers from the VCO distribution system. A programmable divider allows the same VCO to be used for both high- and low bands. Excellent 90° quadrature phase- and amplitude match are achieved by careful design and layout of the demodulators and VCO distribution circuits.

The baseband section, which includes distributed gain and filtering, is designed to provide a maximum of 54-dB gain with a 60-dB gain-control range. Through careful design, pass-band ripple, group delay, signal loss, and power consumption are

kept to a minimum. Filter calibration is performed during the manufacturing process, resulting in a high degree of accuracy and ease of use. Two selectable 7<sup>th</sup>-order baseband filters are available: one with a 1.92-MHz cutoff for W-CDMA and one with a 100-kHz cutoff for GSM.

In W-CDMA mode, the ADF4602 is capable of providing 102-dB gain with a 90-dB gain-control range distributed throughout the *receive* signal chain. The RF front-end contains 30-dB of control range: 18 dB in the LNA and 12 dB in the mixer transconductance stage. The two baseband active filter stages each provide an 18-dB gain-control range in 6-dB steps. This results in a 36-dB total gain control range in three 12-dB steps. The variable-gain amplifier (VGA) implements a 24-dB gain control range in 1-dB steps. To simplify programming and ensure optimum receiver performance and dynamic range, simply program the total desired *receive* gain; the ADF4602 decodes the gain setting and automatically distributes the gain between the various blocks.

The transmitter uses an innovative direct-conversion modulator, which achieves high linearity and low noise while eliminating the need for external *transmit* SAW filters. The differential, dc-coupled baseband interface for I and Q channels supports a wide range of input common-mode voltages (VCM) from 1.05 V to 1.4 V. The maximum allowed signal swing is 550 mV peak, which corresponds to a differential range of 1.1 V p-p on either I or Q channels. Prior to the quadrature modulator, the baseband inputs' signals pass through a 2<sup>nd</sup>-order Butterworth filter with a cutoff frequency of 4 MHz to suppress out-of-band spurs. Calibration techniques maintain accurate I/Q balance and phase across frequency and environmental conditions, ensuring that 3GPP carrier leakage, EVM, and ACLR requirements are met with good margin under all conditions. The ADF4602 achieves a -163-dBm/Hz broadband noise floor at a 190 MHz offset and -8-dBm output power, while meeting TS25.104 requirements for EVM and ACLR. The output is matched to 50  $\Omega$  to enable a simple connection to the power amplifier.

### AD9863 Mixed-Signal Front-End Baseband Transceiver

The AD9863, a member of the MxFE family of integrated converters for the communications market, is ideally suited for low-cost, high-performance femtocell applications. It integrates dual 12-bit analog-to-digital converters and dual 12-bit TxDAC<sup>®</sup> digital-to-analog converters. The ADCs are optimized for sampling at 50 MSPS or less. The DACs, which operate at speeds up to 200 MHz, include a bypassable 2 $\times$  or 4 $\times$  interpolation filter. Packaged in a 64-lead LFCSP package, the AD9863 is only 9 mm  $\times$  9 mm  $\times$  0.9 mm. The AD9863 is highlighted here, but other members of the MxFE family (AD9860, AD9861, and AD9862) offer the designer flexibility in choice of performance and auxiliary converters for control circuits.

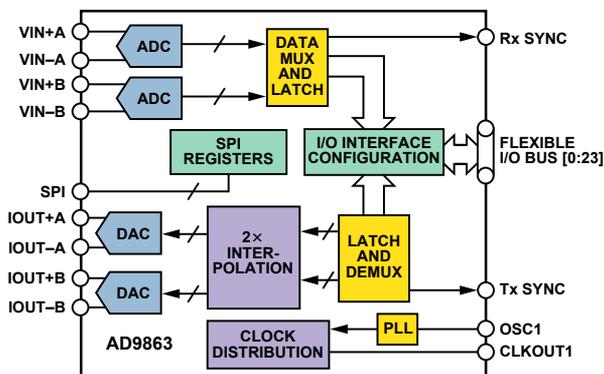


Figure 4. AD9863 MxFE block diagram.

A flexible, bidirectional 24-bit I/O bus accommodates a variety of commercially available baseband ASICs or DSPs. In half-duplex systems, the interface supports 24-bit parallel transfers or 12-bit interleaved transfers. In full-duplex systems, the interface supports a 12-bit interleaved ADC bus and a 12-bit interleaved DAC bus. The flexible I/O bus reduces pin count and package size. For frequency division duplex (FDD) W-CDMA, the AD9863 operates *transmit* and *receive* channels simultaneously. This requires the use of full duplex mode—one 12-bit interleaved Rx data bus and one 12-bit interleaved Tx data bus.

The DAC core converts the 12-bit data into two complementary differential current outputs, providing them to the ADF4602 using a resistor network, as shown in Figure 5.  $R_{DC}$  is set to 120  $\Omega$  for a 1.2-V common-mode voltage, and  $R_L$  is set to 63  $\Omega$  for a 1-V p-p differential input swing.

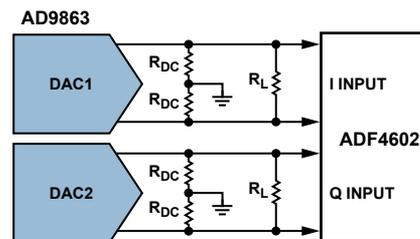


Figure 5. Simple interface between the AD9863 and ADF4602.

The DACs contain programmable fine-gain- and dc-offset controls that can be used to compensate for mismatches between I and Q channels to suppress LO feedthrough and improve EVM performance. The 10-bit dc-offset controls can be used independently to provide up to  $\pm 12\%$  of offset to either differential pin, thus allowing calibration of any system offsets.

The ADC input consists of a 2 k $\Omega$  differential input resistance and a switched capacitor circuit. The input can be self biased to midsupply, or it can be programmed to accept an external dc bias. It is thus recommended that the ADF4602 *receive* baseband outputs be connected directly to the AD9863 ADC inputs. The ADC input full-scale level is 2 V p-p differential.

### Clock Solution for the Femtocell

The femtocell requires a very accurate reference clock— $\pm 0.1$  ppm—in order to meet 3GPP specifications. Methods for implementing this very fine clock control are outside the scope of this article—but a number of possibilities exist, including GSM macrocell synchronization via the monitoring receivers, GPS synchronization, and IEEE 1588 precision timing protocol. In some instances, a combination of the above methods may be implemented by femtocell vendors. Ultimately, the reference timing control circuitry will regulate the reference frequency source. On the ADI evaluation board, this 26-MHz VCTCXO is used as the reference to the ADF4602. A delay-locked loop (DLL) generates 19.2 MHz, which is a multiple of the 3.84-MHz W-CDMA chip clock. This 19.2-MHz clock is used as the clock input for the AD9863.

The AD9863 has a versatile clocking configuration with many variables. The ADC clock rate, DAC clock rate, PLL, and interpolator settings are software controllable, allowing optimization of power vs. performance to suit the requirements. In the recommended configuration, the PLL multiplier is set to 2 $\times$ , giving a PLL output frequency of 38.4 MHz. The ADC is clocked at half this frequency. On the *transmit* side, the 38.4-MHz PLL output is used to clock the DAC. *Transmit* interpolation is set to 2 $\times$  in order to suppress DAC images. Other combinations of clock frequencies are also possible. The AD9863 data sheet provides

a complete description of the operating modes. Using the above clock scheme, the femtocell does not require any discrete frequency conversion PLLs, as are often found in macrocell base stations. All frequency conversion is integrated, helping the femtocell to meet the price point demanded by the market.

### RF Amplifiers

The amplifiers chosen for the RF power stage are low-cost, high-performance, broadband linear amplifiers fabricated on an InGaP process. They linearly amplify the output of the ADF4602 and compensate for losses in the RF duplexer and switching networks. The ADL5542 contains internal biasing and matching; the ADL5320 requires external matching, and is packaged in an industry-standard plastic SOT-23 package. Both amplifiers run directly off a 5-V rail, so no external bias circuitry is required. Key specifications for the amplifiers are shown in Table 1. Proprietary techniques applied to the design of the ADI RF amplifiers provide exceptional linearity vs. supply current.

**Table 1. Key Specifications for the ADF5542 and ADL5320 (@ 2 GHz)**

Specification	ADL5542	ADL5320
Gain	19 dB	13.2 dB
P1dB	18.9 dBm	25.7 dBm
Output IP3	37 dBm	42 dBm
Noise Figure	3.1 dB	4.4 dB
Supply Current (5 V Supply)	97 mA	104 mA

### Transmit Output Power and Interference Mitigation

To mitigate interference, the femtocell must set its output power flexibly and intelligently to account for deployments where multiple femtocells operating on the same frequency are located in close proximity to each other (e.g., in an apartment complex). Here, each femtocell will need to transmit at lower output powers to avoid same-frequency interference. Also, the femtocell cannot cause interference to geographically neighboring macrocell base stations operating on the adjacent channel, as this would create dead spots for nearby mobile phones connected to the macrocell network. The femtocell will thus have an *adjacent channel protection* requirement, forcing it to measure the power in the adjacent downlink channel and set its own power according to a predetermined formula so as not to obstruct the macrocell signal.<sup>1</sup>

To allow the femtocell to meet the price point required and for ease of customer installation, these interference mitigation techniques must be automatic and must not require input from a trained field technician or the home user. This process should be automatically initiated when the box is first turned on by the user, and updated at regular intervals thereafter. Together, the band 1 monitoring receiver on the ADI design and the large *transmit* dynamic range available on the ADF4602 allow the femtocell vendor to implement these interference mitigation techniques automatically without external input. The monitoring receiver allows the power in the adjacent channel to be measured accurately and the output power to be adjusted accordingly. About 30 dB of total *transmit* power dynamic range will be required.

### Radio Performance Measurements

To evaluate the transceiver chipset against the TS25.104 radio systems specifications, the transceiver lineup described above has been incorporated into an evaluation board design. The evaluation platform, shown in Figure 6, enables the independent testing of *transmit* and *receive* chains, as well as individual component

testing. The evaluation board includes the functionality of the block diagram in Figure 1 as well as power conditioning. The radio portion, including ADF4602, AD9863, ADL5542, ADL5320, VCTCXO, and all associated front-end switches and filters, occupies a 1" x 2" space on the board. Note that this board has not been optimized for space savings as it is provisioned for testing purposes, but a more compact design can be achieved for production. Some of the key test results against the TS25.104 specifications are included below to illustrate the performance of the ADI chipset on the evaluation board.

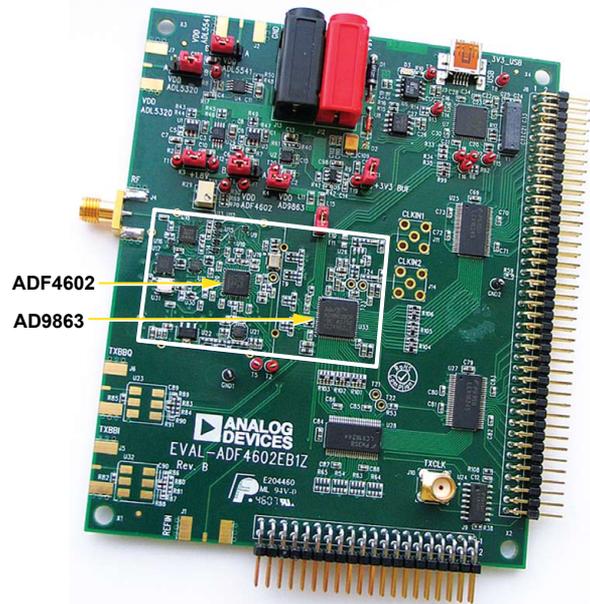


Figure 6. ADF4602/AD9863 evaluation board.

Figure 7 shows the band 1 receiver sensitivity measurement. Receiver sensitivity is a measure of how well the receiver can detect a low-level signal, and is an indicator of the noise figure of the receiver. In this measurement, a 12.2 kHz reference is used. The ADF4602 gain is set to 80 dB. The receiver sensitivity exceeds the TS25.104 specification by 6 dB or more across the band.

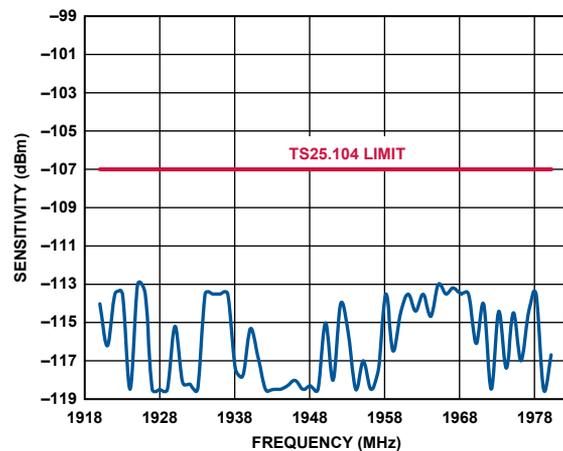


Figure 7. Band 1 receiver sensitivity.

Another key specification for the receiver is the performance under blocking conditions. The blocking tests simulate the ability to receive the wanted signal in the presence of large unwanted signals in adjacent channels. The UL 12.2-kHz reference signal is set to -101 dBm, and blocking signals are injected until a BER of  $10^{-3}$  is measured. As shown in Table 2, the ADF4602 exceeds the TS25.104 with some margin in all three cases.

<sup>1</sup>TSG R4#48 - TSG-RAN Working Group 4 (Radio) meeting #48. October 2008.

**Table 2. Summary of Receiver Blocking Testing vs. TS25.104 Specifications**

Receiver Blocking Specifications	TS25.104 Specification Limit	ADF4602 Evaluation Board Test Results
Adjacent Channel Selectivity	-38 dBm	-31 dBm (7 dB margin)
10 MHz WCDMA Blocker	-30 dBm	-21 dBm (9 dB margin)
20 MHz Out of Band CW Blocker (1900 MHz)	-15 dBm	-11 dBm (4 dB margin)

Key indications of transmit chain quality are adjacent channel leakage ratio (ACLR) and error vector magnitude (EVM). In both cases these tests are key indicators of the linearity of the combined transmit chain. Table 3 compiles the measurements taken on the ADI evaluation board compared to the TS25.104 specifications. It also includes peak code domain error, an EVM measurement that ensures even spreading of errors over the code domain.<sup>ii</sup> In all cases, the ADF4602 evaluation board exceeds the TS25.104 specifications with margin. A plot of the output spectrum used in the ACLR measurements is shown in Figure 8.

**Table 3. Summary of Transmitter Testing vs. TS25.104 Specifications**

Transmitter Specification	TS25.104 Specification Limit	ADF4602 Evaluation Board Test Results
Error Vector Magnitude (EVM)	<12%	4%
Peak Code Domain Error (PkCDE)	<-33 dB	-46 dB
Adjacent Channel (5 MHz) ACLR	<-45 dB	-49 dB
Alternate Channel (10 MHz) ACLR	<-50 dBm	-72 dB

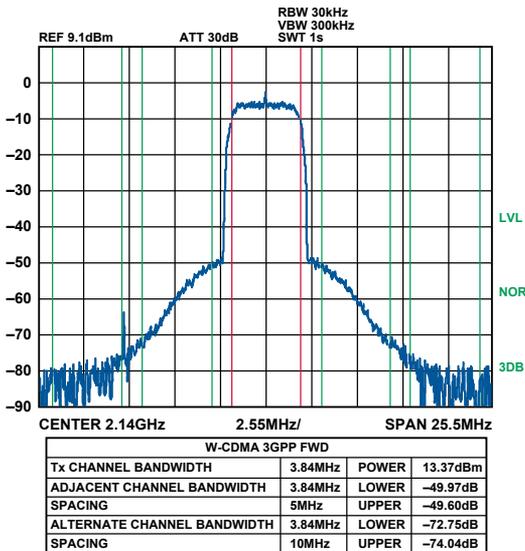


Figure 8. ACLR measurement for W-CDMA band 1 signal with 13 dBm output power.

Figure 9 shows a transmit EVM plot for a typical femtocell configuration involving two HSDPA channels and a number of voice/data channels. The composite EVM is below 4%. Evaluation of the circuit has shown that the EVM is dominated by the LO leakage introduced by the I/Q offsets voltage at the input of the modulator—a feature of direct-conversion transmitters. As mentioned above, these offsets may be calibrated out by using the AD9863 dc-offset controls.

<sup>ii</sup>TSG R4#8 (99)705 - TSG-RAN Working Group 4 (Radio) meeting #8. October 1999.

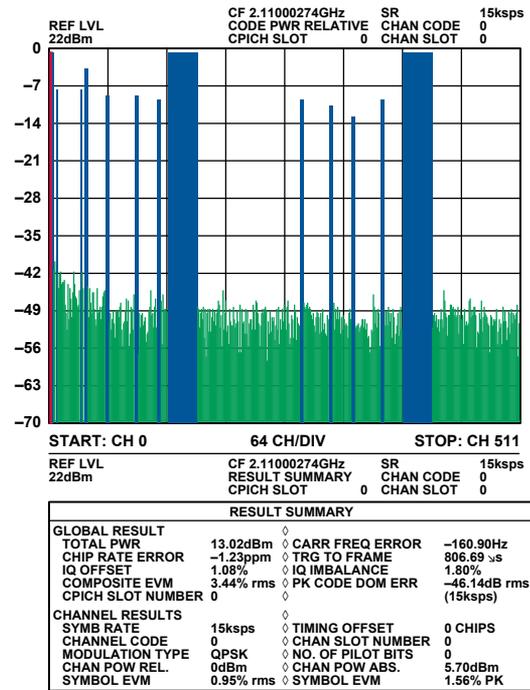


Figure 9. EVM measurement for a typical femtocell configuration.

**CONCLUSION**

The emerging femtocell application presents a unique challenge to the radio designer to minimize cost while maintaining base-station performance. The ADI 3G femtocell chipset comprised of the ADF4602 integrated radio transceiver, AD9863 MxFE baseband transceiver, and ADL5542 and ADL5320 RF amplifiers enables the femtocell designer to meet the TS25.104 specifications in a compact form factor.

**REFERENCES**

- [www.analog.com/AD9863](http://www.analog.com/AD9863)
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- [www.analog.com/ADL5542](http://www.analog.com/ADL5542)
- [www.analog.com/ADL5320](http://www.analog.com/ADL5320)

**THE AUTHORS**

**Thomas Cameron** (thomas.cameron@analog.com) joined ADI in 2006. Currently a technical business manager concentrating on the wireless infrastructure vertical market, he began his career in 1986 in the Radio Networks Division at Bell Northern Research (now Nortel Networks), where he held various positions spanning research, design, and management of technology, devices, and subsystems for telecom networks. In 1999, he joined Sirenza Microdevices, where he advanced to director of marketing for wireless products. In 2004, he moved to WJ Communications, where he held the position of European sales manager. Thomas holds a B.Sc. from Wilfrid Laurier University in Waterloo, Canada; an M.Eng. in Electrical Engineering from Carleton University in Ottawa, Canada; and a Ph.D. in Electrical Engineering from the Georgia Institute of Technology. He holds seven patents and has authored numerous technical papers and articles.



**Peadar Forbes** (peadar.forbes@analog.com) joined Analog Devices in 2004, following his graduation from University College Cork, Ireland, with a Bachelor of Science in Microelectronic Engineering. He currently works for the RF product line, providing applications support for RF transceivers and PLL products. In his spare time Peadar enjoys music, playing guitar, sports, and travel.

