

Designing High-Performance Phase-Locked Loops with High-Voltage VCOs

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Introduction

The *phase-locked loop* (PLL) is a fundamental building block of modern communication systems. PLLs are typically used to provide the *local-oscillator* (LO) function in a radio receiver or transmitter; they are also used for clock-signal distribution and noise reduction—and, increasingly, as the *clock* source for high-sampling-rate *analog-to-digital* (A/D) conversion.

As feature size has shrunk in integrated-circuit processing, device supply voltages, including supplies for PLLs and other mixed-signal functions, have followed downward. However, the practical technology for *voltage-controlled oscillators* (VCOs), a critical element of PLLs, has not decreased as rapidly. Many high-performance VCO designs are still implemented with discrete circuitry that may require supply voltages as great as 30 V. This imposes a challenge for today's PLL or RF system designer: to interface the low-voltage PLL IC with a higher voltage VCO. The level-shifting interface is typically implemented using active filter circuitry—to be discussed below.

This article will consider the basics of PLLs, examine the current state of the art in PLL design with high voltage VCOs, discuss the pros and cons of typical architectures, and introduce some alternatives to high-voltage VCOs.

PLL Basics

A phase-locked loop (Figure 1) is a feedback system in which a phase comparator or detector drives a VCO in a feedback loop to make the oscillator frequency (or phase) accurately track that of an applied reference frequency. A filter circuit is typically required to integrate and smooth the positive or negative error signal—and promote loop stability. A frequency divider is often included in the feedback path to establish the output frequency (within the range of the VCO) as a *multiple* of the reference frequency. The divider can be implemented so that the frequency multiple, N , will be either an integer or a fractional number, characterizing the PLL as an *integer-N PLL* or a *fractional-N PLL*.

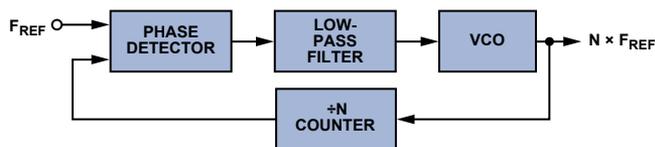


Figure 1. A basic phase-locked loop.

Because a PLL is a negative-feedback control loop, the frequency error signal will be forced to zero at equilibrium to produce an accurate and stable frequency of $N \times F_{REF}$ at the output of the VCO.

PLLs are implemented in various ways, using all-digital, all-analog, or combined circuitry, depending on the required frequency range, noise and spurious performance, and physical size. At present, the architecture of choice for high-frequency, or RF, PLLs combines all-digital blocks, such as feedback dividers and phase detectors, with high-precision analog circuits, such as charge pumps and VCOs. The main features of a mixed-signal PLL are:

1. *Reference frequency*: The stable, accurate frequency reference to which the RF output will be phase locked. It is typically derived from a crystal or *temperature-controlled crystal oscillator* (TCXO).

2. *Phase frequency detector* (PFD): Derives the phase-error signal from the reference and feedback signals.
3. *Charge pump*: Converts the error signal into a train of positive or negative current pulses in proportion to the phase error.
4. *Loop filter*: Integrates the current pulses from the charge pump, providing a clean voltage to the VCO tuning port.
5. *VCO*: Outputs a frequency that depends on the voltage presented to its tuning port (V_{tune}). The VCO has gain, K_V , expressed in MHz/V. The basic VCO expression relating output frequency to the input control voltage is $f_o = f_c + K_v (V_{tune})$, where f_c is the VCO offset frequency.
6. *N divider*: Divides the output frequency down to equal the PFD or reference frequency. It can straightforwardly divide by an integer—or, increasingly, be implemented as a *fractional* divider. The fractional divider can be simply implemented by toggling the divide values in an integer divider to get a fractional average (for example, to get an average of 4.25, count to 4 three times and count to 5 once. Seventeen pulses have been counted and 4 pulses have been created; so the frequency ratio is $17/4 = 4.25$). In practice, better results can be achieved by borrowing from techniques used in high-resolution noise-shaped converters. Thus, the fractional engine is usually implemented using a Σ - Δ architecture, which has the advantage of reducing spurious frequencies.

As an example of the highly integrated circuitry used in available devices, Figure 2 shows a block diagram of a fractional-N PLL IC, the ADF4350 wideband synthesizer with integrated VCO; it has an output frequency range of 137.5 MHz to 4400 MHz. (A brief summary of its capabilities can be found in the [Wide-Bandwidth PLLs with Integrated VCOs](#) section.)

The key performance-limiting characteristics of PLLs are *phase noise*, *spurious frequencies*, and *lock time*.

Phase noise: Equivalent to jitter in the time domain, phase noise is oscillator or PLL noise as evaluated in the frequency domain. It is the rms sum of the noise contributed by the various components in the PLL. The charge-pump-based PLL will suppress VCO noise inside the loop filter bandwidth. Outside of the loop bandwidth, the VCO noise dominates.

Spurs: Spurious frequency components are caused by the charge pump's periodic updating of the VCO tuning voltage. They will appear at a frequency offset from the carrier by the PFD frequency. In a fractional-N PLL, spurs will also occur due to the action of the fractional divider.

Lock Time: The time taken for the PLL's phase or frequency to return to lock range when changing from one frequency to another or responding to a transient offset. It can be specified in terms of frequency- or phase settling. Its degree of importance as a specification depends on the application.

Why Do VCOs Still Use High Voltages?

High-performance VCOs are among the last electronic components to resist the tide of silicon integration. Only in the past few years have VCOs for cellular handsets been fully integrated into their radio chipsets. However, cellular base stations, microwave point-to-point systems, military and aerospace, and other higher-performance applications are still beyond the capability of silicon-based VCOs and are still implemented using a discrete approach. Here's why:

Most commercially available discrete VCOs use a variable-capacitance *varactor* diode as the tunable element in an LC-based tank circuit. Varying the diode's voltage changes its capacitance and, thus, the resonant frequency of the tank circuit.

The noninverting loop filter configuration does not require a dedicated bias, so it can be a more compact solution. The charge pump voltage, instead of being biased at a fixed level, will now vary across its operating range. For this reason, it is much more critical to use an op amp with rail-to-rail inputs when using this filter type. (Input voltage range requirements are described in the next section.)

Choice of Op Amp

The choice of op amp is the key to maximizing the potential of an active filter. Besides bandwidth, the main performance specifications to consider are:

- Noise voltage density—expressed in nV/\sqrt{Hz}
- Current noise—expressed in pA/\sqrt{Hz}
- Input bias current
- Common-mode voltage range

The output of the filter directly affects the generated frequency and phase; therefore, the op amp's noise-voltage density gives an indication of how much phase noise will be added by the active filter. Amplifier noise is added both within the PLL loop bandwidth and out of band—and is most pronounced at the loop filter's corner frequency, especially for amplifiers with high noise voltage density. Thus, it is important to keep the amplifier's noise low to fulfill the mission of the amplifier and high-voltage VCO: to provide lower phase noise. A good design target would be $<10 nV/\sqrt{Hz}$. *Current noise* is usually quite small compared to the error current pulses, so its effects tend to be much smaller than those of voltage noise.

Op amps that have significant input bias currents in relation to the PFD output current can result in large spurs on the PLL output spectrum. To keep the VCO tuning voltage constant and the PLL in lock, the charge pump must replace the bias current drawn by the op amp inputs on each PFD cycle. This modulates the V_{TUNE} voltage at the PFD frequency and causes spurs around the carrier at an offset equal to the PFD frequency. The higher the input bias current, the greater the modulation of the V_{TUNE} voltage and the higher the spur amplitudes.

Common-mode voltage range, or *input voltage range (IVR)*, another important op amp specification, is often overlooked, causing serious problems in the end design. IVR determines the clearance needed at the input terminals between the maximum/minimum signals and the positive/negative power rails.

Early op amps that ran on ± 15 V had typical IVRs of ± 12 V. Slow lateral PNP input stages, added later, allowed the IVR to include the negative rail, thus providing single-supply capability. Although any op amp will run on ground and a positive supply, it is necessary to observe the distance from the rails.

For example, the popular OP27 has an IVR of ± 12.3 V with a ± 15 -V supply. This means that the input voltages need to be at least ± 2.7 V from the positive and negative rails. This limitation at the lower end of the range would make it unattractive for use with wide input swings in single-supply operation. A dual-supply design option, if available, allows a much greater choice of op amps (and simplifies the input bias question). If single-supply design is necessary, use op amps that allow the input voltage to swing from rail to rail (but many of them may have higher noise-voltage specs). Thus, for best results, one needs an op amp with low noise voltage density for low phase noise, low input bias currents for low spurs, and rail-to-rail inputs for single-supply operation. Table 1 lists some Analog Devices op amps and their specifications in relation to the above design criteria.

Table 1. Recommended Op Amps to Use in PLL Active Loop Filters

Op Amp	Voltage Noise, $f = 1$ kHz (nV/\sqrt{Hz})	Current Noise, $f = 1$ kHz (pA/\sqrt{Hz})	Input Bias Current (Typ)	Input Voltage Range, Clearance from Lower Rail (V)	V_{SUPPLY} Max, Single-Supply (V)
AD820	16	0.8	2 pA	-0.2	36
OP184	3.9	0.4	60 nA	0	36
AD8661	12	0.1	0.3 pA	-0.1	16
OP27	3	0.4	10 nA	+2.7	36
AD8099	2	8	100 nA	+1.3	12

The choice of op amp depends on the application. If the PFD spurs are far outside the loop bandwidth (for example, in fractional-N synthesizers), then a bipolar-junction-transistor-input (BJT) op amp—like the OP184 or OP27—will be suitable. The PFD spurs caused by the high input bias current of the BJT will be well attenuated by the loop filter, and the PLL can take full advantage of the BJT op amp's low noise voltage density.

If the application requires the PFD-to-loop-bandwidth ratio to be small (for example, in an integer-N synthesizer), a compromise should be reached between noise and spur levels; the AD820 and AD8661 could be good choices here.

It is worth noting that although active filters tend to contribute noise to the PLL, their ability to act as buffers provides a performance advantage over passive filters in some application niches. For example, if the VCO has high leakage current on its tuning port leading to high PFD spurs, an op amp can be used to reduce the spur levels. The op amp's low impedance output can easily supply the tuning port leakage current.

Design Example

Consider an example where the LO has the following specifications:

- Octave tuning range from 1000 MHz to 2000 MHz
- Phase noise requirement of -142 dBc/Hz at 1 MHz offset
- Spurs < -70 dBc
- 250-kHz channel spacing
- Lock time < 2 ms
- Single supply of 15 V or 30 V available

To cover the 1-GHz band, while meeting the phase-noise target, it is necessary to use a high-voltage VCO and an active loop filter. The phase-noise and spur specifications, and single-supply restriction, will drive the choice of op amp. To meet the spur specifications the op amp input bias current must be low, while best phase noise will be achieved with an op amp with low voltage noise. A compromise between the two can be reached by choosing a JFET-input op amp, such as the AD8661, which has an input bias current of 0.3 pA and voltage noise of $12 nV/\sqrt{Hz}$. This device can also handle the single-supply requirement. The RFMD UMS-2000-A16 VCO was selected to cover the octave range.

The best place to start is with a simulation involving the active-filter topologies supported in the ADIsimPLL™ tool. Two of the recommended filter types are shown in Figure 3, but ADIsimPLL supports other configurations as well.

For the PLL, the ADF4150, which can be operated in either integer or fractional mode, was chosen; it also has output divider options of 2/4/8/16/32—which allow continuous coverage from 2 GHz down to 31.25 MHz. The ADF4150 is similar to the ADF4350 shown in Figure 2, but it allows the choice of an external VCO for applications that need to meet more stringent phase-noise requirements. In the simulation, the PLL loop filter was set at 20 kHz to attempt to minimize the op amp noise contribution, while keeping the PLL lock time less than 2 ms.

Figure 4 shows a plot of noise (dBc) as a function of frequency offset in simulated and measured systems, using an ADF4150 PLL, a UMS VCO, and an AD8661-based filter. A -90 -dBc peak at about 20 kHz, due to the noise added by the active loop filter, can be seen in both noise profiles, but the -142 -dBc/Hz target at 1 MHz offset is still being met. To reduce the in-band noise, a lower-noise op amp, such as the OP184 or OP27, could be used at the expense of higher spurs; or the PLL loop bandwidth could be decreased to below 20 kHz.

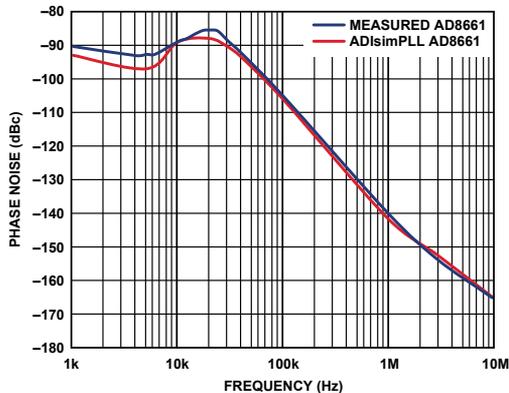


Figure 4. ADIsimPLL simulation vs. measured performance using AD8661 as an op amp in PLL active filter.

Figure 5 shows the approximately 6-dB improvement when the OP27 is used. In this case, spurs do not increase significantly, as the loop bandwidth is relatively narrow. Lowering the bandwidth further will improve phase noise for offsets below 100 kHz at the expense of increased PLL lock-time. All of these trade-offs can be tested with ADIsimPLL simulations prior to going into the lab.

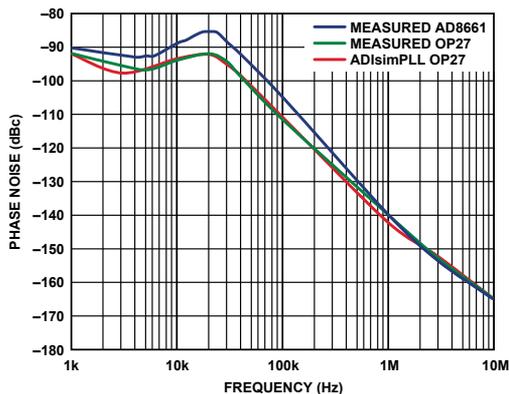


Figure 5. PLL measured performance using AD8661 vs. OP27 in active loop filter.

Breaking News: High Voltage PLLs

Up to this point the discussion has been driven by the need to use active filters to interface a low-voltage PLL device to a high-voltage VCO. *High-voltage PLLs are becoming available, however, greatly reducing the necessity for an active filter.* An example is the **ADF4113HV** PLL, which integrates a high-voltage charge pump and has -212 -dBc/Hz normalized phase-noise floor. In this case, the PLL charge pump output can be as high as 15 V, allowing a simpler passive filter before the VCO.

This family of high-voltage PLLs will soon be further augmented by devices that increase the maximum voltage to 30 V and fractional-N PLLs that have high-voltage charge pumps. Consult the [PLL web site](#) for updates and new-product information.

Wide-Bandwidth PLLs with Integrated VCOs

Another alternative to using an active filter with high-voltage VCO is to use a *fully integrated high-performance PLL* like the ADF4350,

shown in Figure 2. In this case, the VCO is integrated on chip. The inherent trade-off of wide tuning range and low phase noise discussed above is avoided by using a multiband VCO approach. In the ADF4350, three separate VCOs are integrated on chip, each of which has 16 overlapping subbands, giving a total of 48 subbands. Each time the frequency is updated, an automatic calibration is initiated to select the appropriate VCO subband.

This shows the real benefit of moving VCO designs from a discrete to a silicon-based solution: significant levels of integration can be achieved in minimal area, allowing greater design flexibility. For example, the ADF4350 also integrates a programmable output-divider stage that allows frequency coverage from 137.5 MHz all the way up to 4.4 GHz—a very attractive feature for radio designers who want to reuse the same design across multiple frequencies and standards.

The ADF4350 comes in a 5-mm square LFCSP package—as compared with the standard 12.7-mm square VCO package. Performance levels approach those of discrete designs, with phase noise of -114 dBc/Hz at 100-kHz offset and -134 dBc/Hz at 1-MHz offset. ([Return to Figure 2.](#))

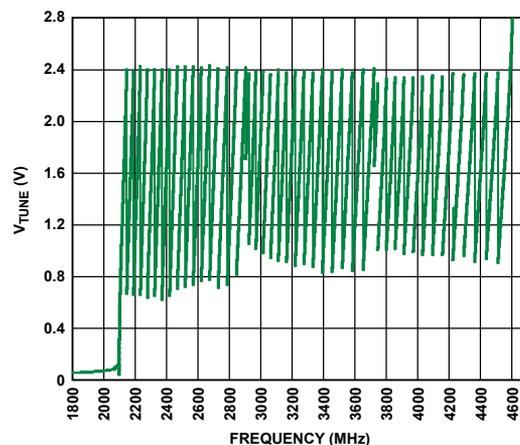


Figure 6. Plot showing the 48 distinct bands in the ADF4350 VCO voltage vs. frequency relationship.

For more on one of the broadest PLL portfolios in the industry, including integer-N, fractional-N, integrated VCO, and high-voltage PLL ICs—pushing performance boundaries and easing design challenges for PLL- and radio designers worldwide—consult the [PLL Synthesizers/VCOs website](#).

References

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2. Best, Roland E. *Phase-Locked Loops. Design, Simulation, and Applications.* McGraw Hill.
3. Curtin, Mike and Paul O'Brien. 1999. "Phase-Locked Loops for High-Frequency Receivers and Transmitters—Part 2." *Analog Dialogue*, Volume 33.
4. Information on all ADI components can be found at www.analog.com.

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