Termination of High-Speed Converter Clock Distribution Devices

By Jerome Patoux

When using clock distribution devices[1] or fanout buffers to clock ADCs and DACs, two main sources of signal degradation—printed-circuit board (PCB) trace implementation and output termination—need to be dealt with.

Clock Traces and Signal Swing

PCB traces behave like low-pass filters, attenuating clock signals as they travel along the trace and increasing pulse-edge distortion with trace length. Higher frequency clock signals are subject to increased attenuation, distortion, and noise, but to improve jitter, which is worst at low slew rates (Figure 1), clock edges with a high slew rate are typically used. To correctly implement a quality clock, use high-swing clock signals and short clock PCB traces; place the device to be clocked as close to the clock-distribution device as possible.

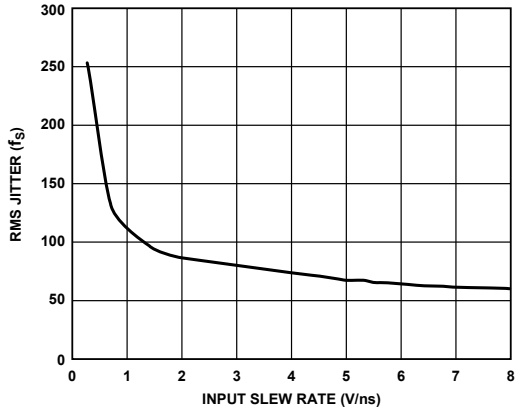


Figure 1. ADCLK925 rms jitter vs. input slew rate.

Two such clock-distribution devices are the ADCLK954[2] clock fanout buffer and the ADCLK914[3] ultrafast clock buffer. The ADCLK954 comprises 12 output drivers that can drive 800-mV full-swing ECL (emitter-coupled logic) or LVPECL (low-voltage positive ECL) signals into 50-Ω loads for a total differential output swing of 1.6 V, as shown in Figure 2. It operates at toggle rates to 4.8 GHz. The ADCLK914 can drive 1.9-V high-voltage differential signals (HVDS) into 50-Ω loads for a total differential output swing of 3.8 V. The ADCLK914 features a 7.5-GHz toggle rate.

When driving a DAC, the clock-distribution device should be placed as close as possible to the DAC's clock input so that the required high slew rate, high amplitude clock signals do not cause routing difficulties, generate EMI, or become degraded by dielectric and other losses. Note that the characteristic impedance (Z_0) of the trace will vary with trace dimension (length, width, and depth); the driver's output impedance must be matched to this characteristic impedance.

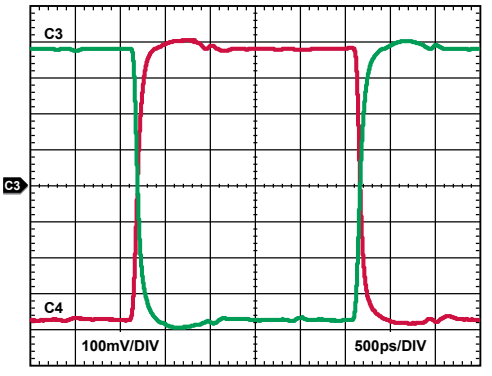


Figure 2. ADCLK954 clock buffer output waveforms with 3.3-V supply.

Output Termination

Clock-signal attenuation can cause increased jitter, so it is important to terminate the driver outputs to avoid signal reflection and to maximize power transfer over a relatively large bandwidth. Indeed, reflections may cause undershoot and overshoot, severely degrading the signal and the overall clock performance or, in extreme cases, possibly damaging the receiver or driver. Reflections, caused by impedance mismatches, occur when the traces are not properly terminated. They are more significant for high-speed signals with fast rise- and fall times due to the high-pass nature of the reflection coefficient. The reflected pulse is superimposed on the main clock signal, thus degrading the clock pulse. It also affects the edges of the clock signal by adding a time-delay uncertainty to the rising and falling edges, as shown in Figure 3.

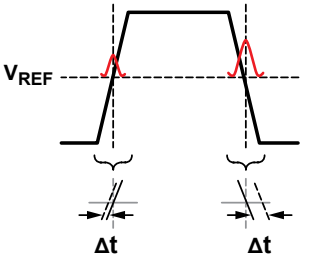


Figure 3. Jitter impact of reflected signal due to improper termination.

The magnitude of the echo due to the improper termination varies with time, so Δt will also vary with time. The termination time constant also affects the shape and width of the echo pulse. For these reasons, this additional reflection-induced jitter shape, which looks Gaussian, adds to the classical jitter. To avoid the adverse effects of this jitter and clock quality reduction, use proper signal termination, as summarized in Table 1. Z_0 is the impedance of the line; Z_{OUT} is the output impedance of the driver; and Z_{IN} is the input impedance of the receiver. Only CMOS and PECL/LVPECL circuits are shown.

References

[1] www.analog.com/en/clock-and-timing/clock-generation-and-distribution/products/index.html.

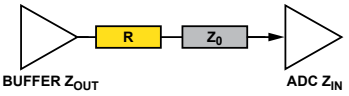
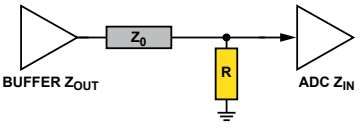
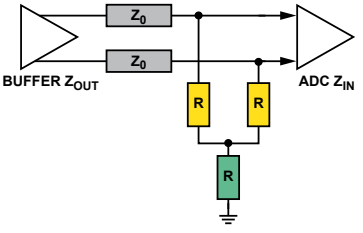
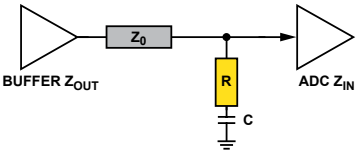
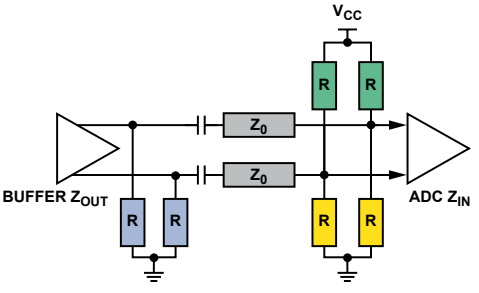
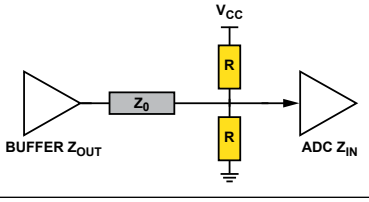
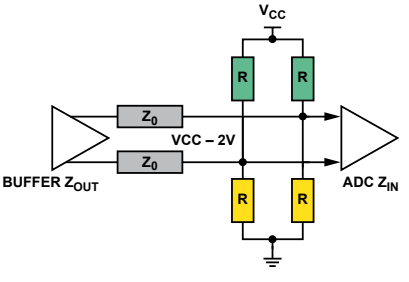
[2] www.analog.com/en/clock-and-timing/clock-generation-and-distribution/adclk954/products/product.html.

[3] www.analog.com/en/clock-and-timing/clock-generation-and-distribution/adclk914/products/product.html.

Author

Jerome Patoux [jerome.patoux@analog.com] is a product marketing engineer for ADI's Clock and Signal Synthesis Group in Greensboro, NC. In 2002, he graduated from ESIGETEL, Avon, France, with a master's degree in electronics and telecommunications engineering. He also has a master's degree in international project management from the University of Quebec in Hull-Gatineau, Canada, and ISMANS, Le Mans, France. Prior to joining ADI in 2005, Jerome worked as a radio engineer for SFR Group and as a department manager for SNCF.

Table 1. Clock Terminations

Method	Description	Strength	Weakness	Comments
Series Termination	**CMOS**  In practice, resistance (R) is omitted at the buffer output as it is hard to match the impedance due to its dynamic behavior over frequency.	Low power solution (no sink current to ground). Easy to calculate R ($Z_0 - Z_{OUT}$).	Rise/fall time impacted by circuit R and C, increasing jitter. Only useful with low-frequency signals.	CMOS drivers. Not suitable for high-frequency clock signals. Suitable for low-frequency clock signals and very short traces.
Pull-Down Resistor	**CMOS** 	Very simple ($R = Z_0$)	High power consumption.	Not recommended.
	LVPECL 	Simple, 3-resistor solution. Slightly better in terms of power saving, while saving a component compared to 4-resistor termination.		Recommended. Place termination resistors as close as possible to the PECL receiver.
AC Termination	**CMOS** 	No dc power consumption.		C should be small to avoid high power consumption, but not too small to allow sink current.
	LVPECL 	AC-coupling allows bias voltage adjustment. Avoids power flow between the two sides of the circuit.	AC-coupling is only recommended for balanced signals (50% duty cycle clock).	AC-coupling capacitors should be low ESR, low capacitance.
Resistor Bridge	**CMOS** 	Reasonable trade-off on power.	Uses two parts for single-ended clocks.	
	LVPECL 		Uses four external parts for differential output logic.	Widely used termination for 3.3-V LVPECL drivers.