ADuC7026 Provides Programmable Voltages for Evaluating Multiple Power Supply Systems

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Introduction

High-voltage switches, bipolar ADCs, and other devices with multiple power supplies often require that supply voltages be applied or removed in a particular sequence. This article proposes an easy, cost-effective method for determining the behavior of a system when subjected to supply transients, interruptions, or sequence variations. An example of a device using multiple supplies is the AD7656-1 (Table 1), a 16-bit, 250 kSPS, 6-channel, simultaneous-sampling, bipolar-input ADC. The ADuC7026 precision analog microcontroller's four 12-bit DACs provide the DUT's programmable supply voltages. Using the AD7656-1 evaluation board and the ADuC7026 evaluation board, prototyping can be performed with a minimum of hardware and software development.

Table 1. AD7656-1 Typical Supply Voltages and Maximum Supply Currents

Supply	AV_{CC}, DV_{CC}	V_{DRIVE}	V_{DD}	V_{SS}
Voltage (V)	5	3.3	10	–10
Current (mA)	30	10	0.25	0.25

Table 1 shows the typical voltage and maximum current for each of the ADC's power supplies. The programmable sequence-controllable voltage waveforms generated by the four DACs on the ADuC7026 are scaled by the ultralow noise-and-distortion AD797 op amps on the AD7656-1 evaluation board to provide the specified supply voltages and currents. The microcontroller's speed and programmability facilitate control of voltage level, period, pulse width, and ramp time of the power supply voltages.

For example, using external power supplies, the AD797 amplifiers on the AD7656-1 evaluation board, configured for a gain of 5, can generate a voltage range of 0 V to 12.5 V to drive the ADC's V_{DD} supply rail. The high output drive capability of the AD797 allows up to 50 mA to be provided to each supply rail. Figure 1 shows the connections to the ADC.

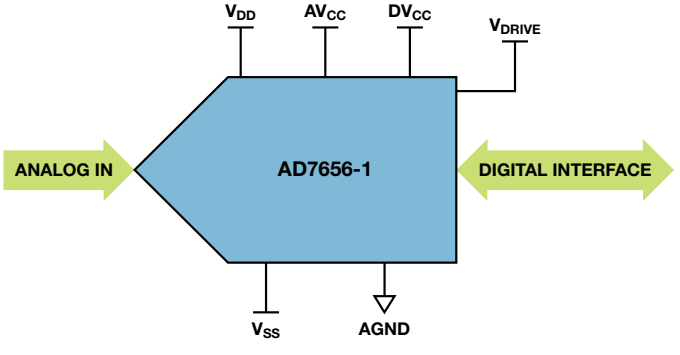

Figure 1. AD7656-1 connection diagram.

The ADuC7026 DAC data register can be updated at 7 MHz with a 41.78-MHz core clock, which maximizes the voltage update rate. The following sections describe the development process and provide measurement results obtained using the evaluation boards.

Hardware Development and Setup

The hardware connection and test setup are shown in Figure 2. Four DAC output pins and AGND on the ADuC7026 evaluation board are connected separately to the four AD797 inputs and AGND on the AD7656-1 evaluation board. An Agilent E3631A external power module provides ±15 V for the AD797. A computer connected via USB to the ADuC7026 evaluation board provides the 5-V power supply and serial communications.

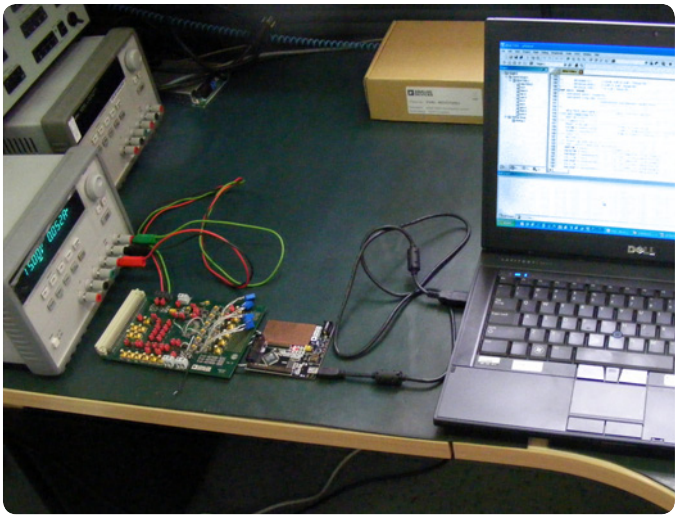

Figure 2. Hardware connections and test bench.

Schematic Design

The only hardware changes required on the AD7656-1 evaluation board relate to the AD797. R1 and R2 can be selected for different gain and bandwidth requirements. Figure 3 shows the AD797 set for gain = 4 to provide a 0-V to 10-V output from the 0-V to 2.5-V output of the ADuC7026 DAC. R3 and C1 form a low-pass filter to reduce high frequency noise. CL is used as a load capacitor on the power rail.

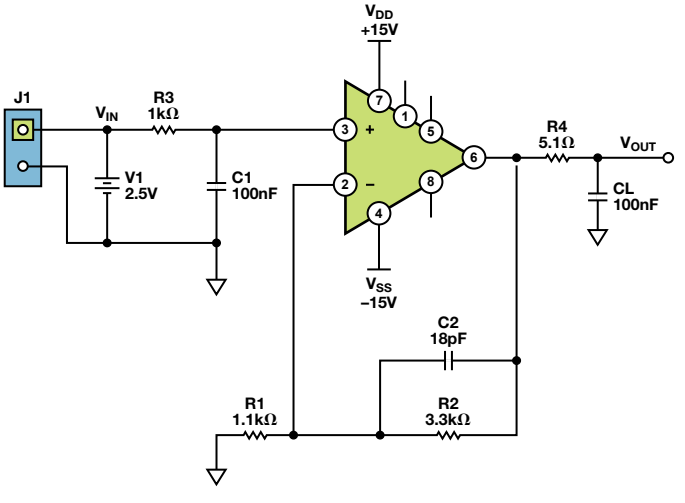

Figure 3. AD797 schematic design with gain = 4.

Figure 4 shows the frequency response of the AD797 with gain = 4, from an NI Multisim™ simulation. The 1.0-MHz bandwidth and 73° phase margin provide fast transient response and stable operation.

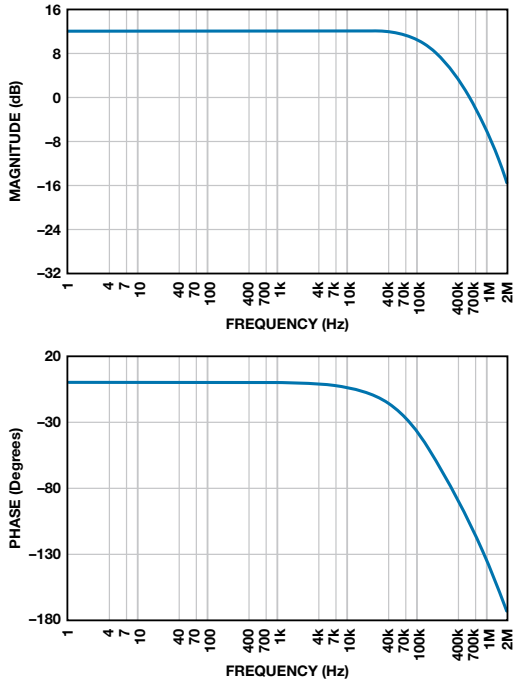

Figure 4. Frequency response of the AD797 with gain = 4.

AD797 Design Notes

The AD797 ultralow-distortion, ultralow-noise op amp features 80-µV maximum offset voltage, excellent dc precision, 800-ns settling time to 16 bits, 50-mA output current, and ±13-V output swing with ±15-V power supplies, making it well suited to driving power-supply rails.

It is not internally compensated for substantial capacitive loads though, so external compensation techniques must be used to optimize this application. Figure 5 shows oscillation on the AD797 output caused by driving capacitive loads.

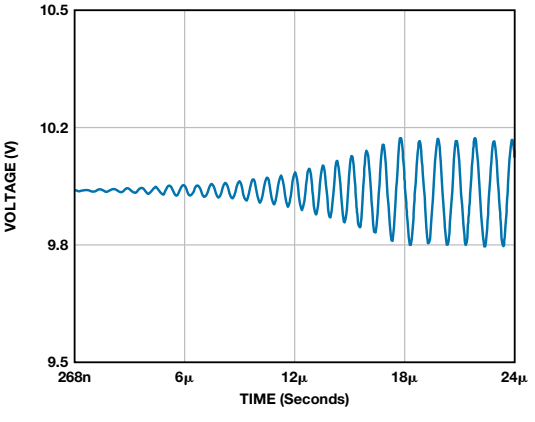

Figure 5. Oscillations without compensation.

For stable drive with capacitive loads on the power rail, Resistor R4 is placed between the output and the load. This resistor isolates the op amp output and feedback network from the capacitive load and introduces a zero in the transfer function of the feedback network, reducing the phase shift at higher frequencies.[1] The feedback capacitor, C2, compensates for the capacitive loading, including C1, at the input of the op amp.

Applying the DACs

The ADuC7026 precision analog microcontroller features four 12-bit voltage-output DACs with rail-to-rail output buffers, three selectable ranges, and 10-µs settling time.

Each DAC has three selectable ranges: 0 V to VREF (internal band gap 2.5-V reference), 0 V to DACREF (0 V to AV_{DD}), and 0 V to AV_{DD}. The range is set using the control register DACxCON. The DAC accepts an external reference with a range of 0 V to AV_{DD}. When using the internal reference, a 0.47 µF capacitor must be connected from the VREF pin to AGND to ensure stability.

Each of the four DACs is independently configurable through control register DACxCON and data register DACxDAT. Once the DAC is configured through the DACxCON register, data can be written to DACxDAT for the required output voltage level.

The four DAC outputs are easy to control using C or assembly language. This C-code example shows how to choose the internal 2.5-V reference and set the DAC0 output to 2.5 V.

```
//connect internal 2.5 V reference to VREF pin
REFCON = 0x01;
//enable DAC0 operation
DAC0CON = 0x12;
//update DAC0DAT register with data 0xFFF
DAC0DAT = 0x0FFF0000;
```

Using assembly language,

```
DAC0CON[5] is cleared to update DAC0 using core
clock (41.78 MHz) for fast update rate;
DAC0CON[1:0] is set to '10' to use 0 V to VREF
(2.5 V) output range
'DAC0DAT = 0x0FFF0000' can be compiled to assembly
code with two instructions:
MOV      R0, #0x0FFF0000
STR       R0, [R1, #0x0604]
```

These two instructions take a total of six clock cycles to execute, corresponding to a 7-MHz update rate with a 41.78-MHz core-clock frequency. Thus, the time delay between voltage rails can be as accurate as 144 ns.

Measurement Results

The four DACs in the ADuC7026 supply four power supplies to the AD7656-1 to test its behavior with power-supply transients or sequence variations. Table 2 shows the ADC's power supplies and voltage levels.

Table 2. Power Supplies for AD7656-1

DAC Channel	DAC0	DAC1	DAC2	DAC3
Output Range	0 V to 1.250 V	0 V to 0.825 V	0 V to 2.500 V	0 V to 2.500 V
AD797 Gain	4	4	5	–5
AD797 Output Swing	0 V to 5.00 V	0 V to 3.30 V	5.00 V to 12.50 V	–12.50 V to –5.00 V
Nominal Voltage	5.00 V	3.30 V	10.00 V	–10.00 V
AD7656-1 Power Supply	AV_{CC}, DV_{CC}	V_{DRIVE}	V_{DD}	V_{SS}

The waveforms from the four DAC outputs, as described in Table 2, were captured using a scope and are shown in Figure 6. The voltage level, period, pulse width, and ramp time of each channel are each programmable and easy to control. The specific parameters are measured and described in the following sections.

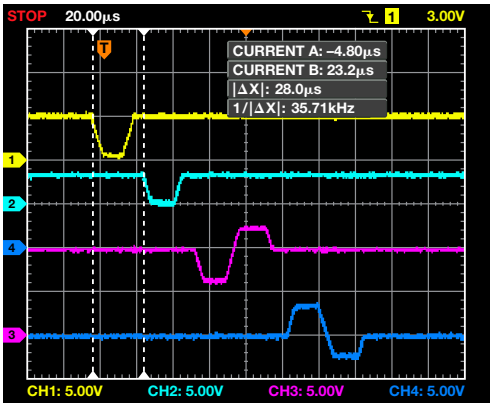

Figure 6. Four-channel voltage waveform.

To achieve an accurate voltage level for each power supply, an adjustable resistor can be used for R1 in Figure 3. The voltage level was calibrated by adjusting R1 with an Agilent 34401A digital multimeter.

Rising and falling ramp time are measured to determine the maximum frequency of the voltage waveforms. The ramp time is related to the value of Resistor R4 and the capacitive load, CL. For slower ramp times, larger resistor and capacitor values can be used for R4 and CL. The rising and falling ramp time of AV_{CC} and DV_{CC} were tested with different load capacitors, with the results shown in Table 3. The rising waveform with a 1-µF capacitor is shown in Figure 7. The ramp time is measured between 10% and 90% of 10 V.

Table 3. Ramp Time with Capacitive Load

Capacitive Load	10 nF (V/µs)	0.1 µF (V/µs)	1 µF (V/µs)	10 µF (V/µs)
Rising Edge	6.90	0.97	0.07	0.01
Falling Edge	5.71	0.93	0.06	0.01

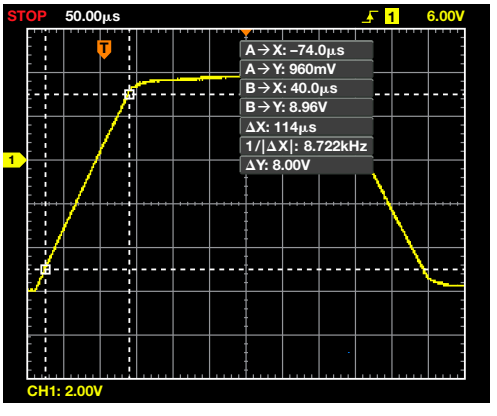

Figure 7. Rise time with 1-µF capacitive load.

Power-Supply Ripple

The excellent dc precision of the AD797 makes it easy to provide accurate nominal voltage levels for the AD7656-1 by adjusting the feedback resistor, R1. The peak-to-peak ripple of the power supplies was measured at nominal voltage levels with 200-MHz and 20-MHz bandwidths, a 0.1-µF capacitive load, and a DS1204B scope. Table 4 shows that the ripple is less than 1% of the nominal voltage, so the four supplies are qualified.

Table 4. Ripple of Each Power Supply

Power Supply	AV_{CC}, DV_{CC} (5.00 V)	V_{DRIVE} (3.30 V)	V_{DD} (10.00 V)	V_{SS} (–10.00 V)
200 MHz (mV)	20.8	28.0	25.6	30.4
20 MHz (mV)	12.8	24.8	15.2	18.4

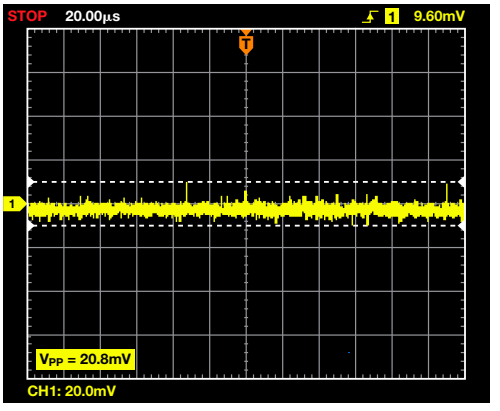

Figure 8. Ripple of 5-V supply on AV_{CC} and DV_{CC}.

Generating Waveforms

With simple modifications to the ADuC7026 source code, many different sequences of voltage waveforms can be generated for a variety of different applications that require evaluation of device operation under different supply conditions. Typical waveforms that can be generated are shown in Figure 9 and Figure 10.

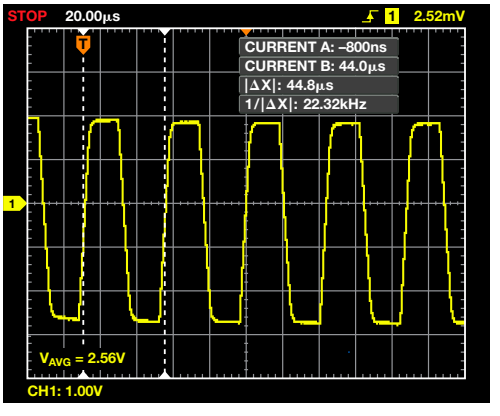

Figure 9. 22.32 kHz square waveform.

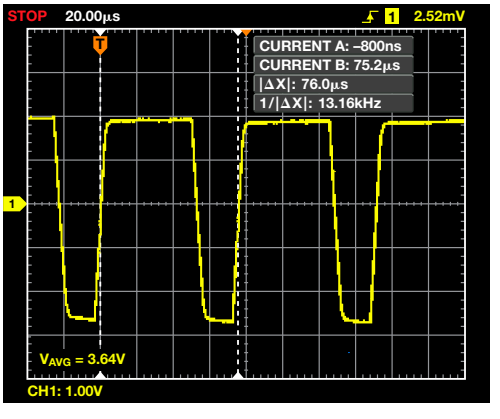

Figure 10. 13.16 kHz pulse waveform.

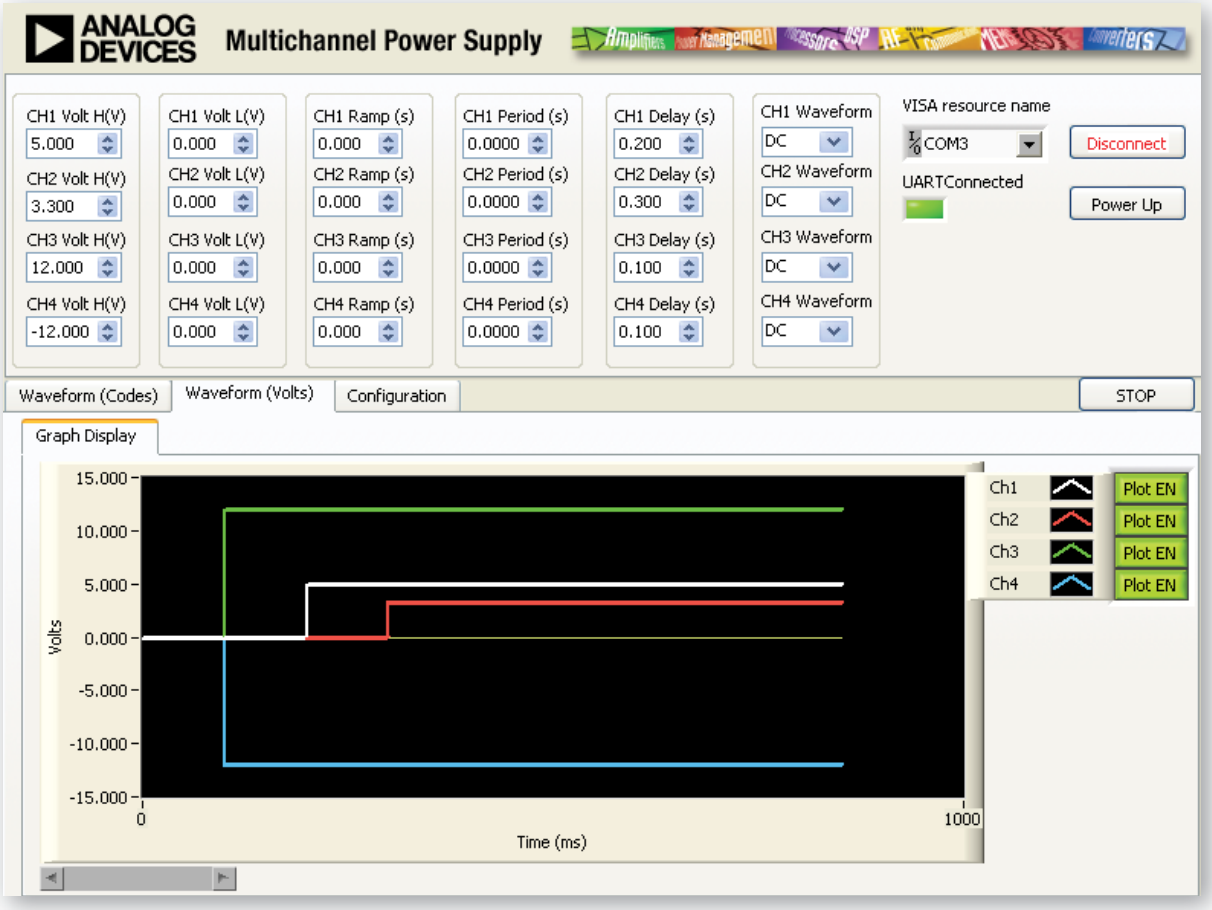

Figure 11. Power supply configuration GUI.

The LabVIEW® GUI shown in Figure 11 can be used to generate the power supply waveforms. The voltage level, ramp time, period, and sequence delay time of the four channels are easy to configure. The serial port is used for communication between GUI and the ADuC7026.

Conclusion

An easy, cost-effective way to evaluate the effects of supply sequencing was developed and verified using the AD7656-1 and ADuC7026 evaluation boards. The ADuC7026 evaluation board generates a controllable programmable sequence for four voltage supplies to evaluate the operation of the ADC under different supply sequence/ramp conditions. The 3-phase, 16-bit PWM generator in the microcontroller can provide a total of seven voltage channels.

With a standard ±15-V dc power module, this portable power supply evaluation systems allows designers to evaluate ADCs, especially for those with larger number of supplies.

Acknowledgments

The authors would like to thank Aude Richard (ADuC applications engineer) for her great advice and help.

[1]Bendaoud, Soufiane and Giampaolo Marino, Practical Techniques to Avoid Instability Due to Capacitive Loading (Ask the Applications Engineer—32), *Analog Dialogue*, Volume 38, Number 2 (2004).

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