Front-End Amplifier and RC Filter Design for a Precision SAR Analog-to-Digital Converter

By Alan Walsh

Successive-approximation (SAR) ADCs offer high resolution, excellent accuracy, and low power consumption. Once a particular precision SAR ADC has been chosen, system designers must determine the support circuitry needed to obtain the best results. The three principal areas to consider are the *front end,* which interfaces the analog input signal to the ADC, the *voltage reference,* and the *digital* interface. This article focuses on the circuit requirements and trade-offs in designing the front end. Useful information on the other areas, which are device- and system-specific, can be found in data sheets—and in this article's references.

The front end consists of two parts: the driving amplifier and the RC filter. The amplifier conditions the input signal—as well as acting as a low-impedance buffer between the signal source and the ADC input. The RC filter limits the amount of out-of-band noise arriving at the ADC input and helps to attenuate the kick from the switched capacitors in the ADC's input.

Choosing the right amplifier and RC filter for a SAR ADC can be a challenge, especially when the application needs to differ from the routine data sheet usage of the ADC. Looking at the various application factors that influence amplifier and RC choice, we provide design guidelines that lead to the best solution. Major considerations include *input frequency, throughput,* and *input multiplexing.*

Selecting a Suitable RC Filter

To select a suitable RC filter, we must calculate the RC bandwidth for single-channel or multiplexed applications, then select values for R and C.

Figure 1 shows a typical amplifier, single-pole RC filter, and ADC. The ADC input presents a switched-cap load to the driving circuitry. Its 10-MHz input bandwidth means that low-noise is needed over a wide bandwidth to get a good signal-to-noise ratio (SNR). The RC network limits the bandwidth of the input signal and reduces the amount of noise fed to the ADC by the amplifier and upstream circuitry. Too much band limiting will increase the settling time and distort the input signal, however.
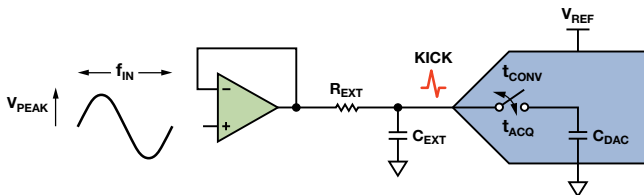

Figure 1. Typical amplifier, RC filter, and ADC.

The minimum RC value needed to settle the ADC input while also optimally band limiting the noise can be calculated assuming exponential settling of a step input. To calculate the size of the step, we need to know the input signal frequency, amplitude, and ADC conversion time. The *conversion time, t_{CONV}* (Figure 2), is when the capacitive DAC is disconnected from the input and is performing bit trials to generate the digital code. At the end of the conversion time, the capacitive DAC, which holds the previous sample charge, is switched back to the input. This step change represents how much the input signal has changed in that time. The time taken to settle this step is known as the *reverse settling time.*
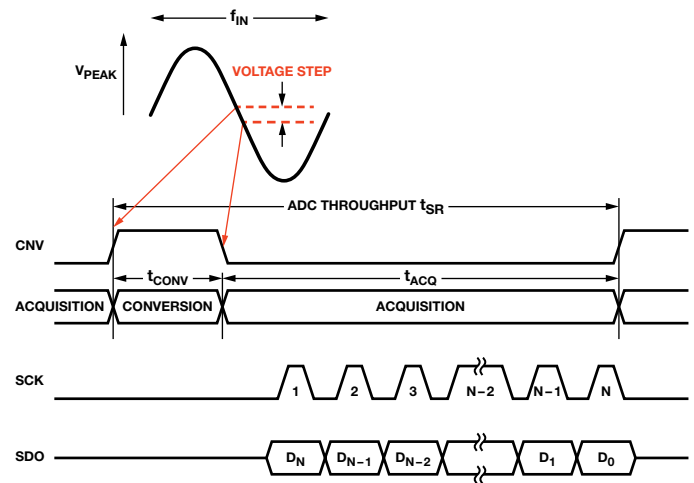

Figure 2. Typical timing diagram for N-bit ADC.

The maximum undistorted rate of change of a sine wave signal with a given input frequency can be calculated as

$$2\pi f_{IN} V_{PEAK}$$

If the conversion rate of the ADC is considerably higher than the maximum input frequency, the maximum amount the input voltage has changed during the conversion time is given by

$$2\pi f_{IN} V_{PEAK} t_{CONV}$$

This is the maximum voltage step that is seen by the capacitive DAC when it is switched back to acquire mode. This step is then attenuated by the parallel combination of the DAC's capacitance and that of the external capacitor. For this reason, it is important that the external capacitor be relatively large—a few nanofarads. This analysis will assume that the on resistance of the input switch has a negligible effect. The step size that now needs to be settled is given by

$$V_{STEP} = \frac{2\pi f_{IN} V_{PEAK} t_{CONV} C_{DAC}}{C_{EXT} + C_{DAC}}$$

Next, calculate the time constant to settle the ADC input to ½ LSB during the acquisition time of the ADC. Assuming exponential settling of the step input, the required RC time constant, τ, is

$$\tau = \frac{t_{ACQ}}{N_{TC}}$$

where t_{ACQ} is the acquisition time and N_{TC} is the number of time constants required to settle. The number of time constants required can be calculated from the natural logarithm of the ratio of the step size, V_{STEP}, to the settling error—which in this case is ½ LSB,

$$V_{half\_lsb} = \frac{V_{REF}}{2^{N + 1}}$$

giving

$$N_{TC} = \ln\left(\frac{V_{STEP}}{V_{half\_lsb}}\right)$$

Substituting this in the previous equation gives

$$\tau = \frac{t_{ACQ}}{\ln\left(\dfrac{V_{STEP}}{V_{half\_lsb}}\right)}$$

And the equivalent RC bandwidth is $\dfrac{1}{2 \times \pi \times \tau}$

Example: Armed with an equation for calculating the RC bandwidth, choose the AD7980 16-bit ADC—shown in Figure 3—with its 710-ns conversion time, 1-MSPS throughput, and 5-V reference. The maximum input frequency of interest is 100 kHz. Calculating the maximum step size at this frequency gives

$$2\pi(100 \text{ kHz})\left(\frac{5 \text{ V}}{2}\right)(710 \text{ ns}) = 1.115 \text{ V}$$

This step is then attenuated by the charge from the external capacitor. Using a DAC capacitance of 27 pF and assuming a 2.7-nF external capacitance, the attenuation factor will be about 101. Plugging these numbers into the equation for V_{STEP} gives

$$V_{STEP} = \frac{1.115 \text{ V} \times 27 \text{ pF}}{2.7 \text{ nF} + 27 \text{ pF}} = 11.042 \text{ mV}$$

Next, calculate the number of time constants to settle to ½ LSB at 16 bits; with a 5-V reference

$$N_{TC} = \ln\left(\frac{11.042 \text{ mV}}{\dfrac{5 \text{ V}}{2^{16+1}}}\right) = 5.668$$

The acquisition time is

$$t_{ACQ} = t_{SR} - t_{CONV} = \frac{1}{1 \text{ MSPS}} - 710 \text{ ns} = 290 \text{ ns}$$

Calculating for τ,

$$\tau = \frac{290 \text{ ns}}{5.668} = 51.16 \text{ ns}$$

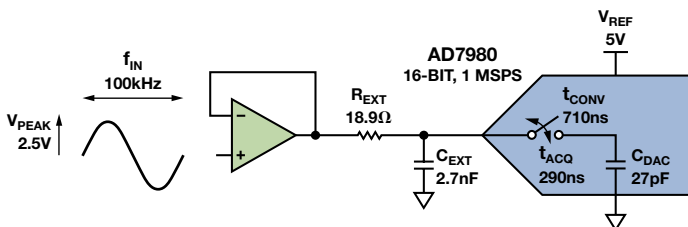So, bandwidth = 3.11 MHz and R_{EXT} = 18.9 Ω.

Figure 3. RC filter using AD7980 16-bit, 1-MSPS ADC.

This relationship between the minimum bandwidth, throughput, and input frequency shows that higher input frequencies require a higher RC bandwidth. Similarly, higher throughput, which results in lower acquisition time, increases the RC bandwidth. The acquisition time has the largest influence on the bandwidth needed; if it were doubled (reducing throughput), the bandwidth required would be halved. This simplified analysis does not include second-order charge kickback effects that become dominant at lower frequencies. In the case of very low input frequencies (<10 kHz), including dc, there will always be ~100 mV of voltage step to settle on the cap DAC. This number should be used as the minimum possible voltage step in the analysis above.

A *multiplexed* input signal is rarely continuous, typically consisting of large steps when switching between channels. In the worst case, one channel is at negative full scale, while the next channel is at positive full scale (see Figure 4). In this case, the step size will be the full range of the ADC, or 5 V in the above example, when the mux switches channels.
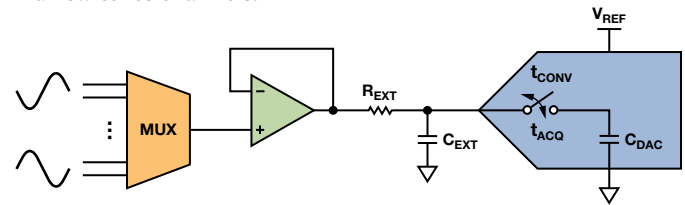

Figure 4. Multiplexed setup.

When using a multiplexed input in the above example, the required filter bandwidth for linear response would increase to 3.93 MHz (step size = 5 V vs. 1.115 V with a single channel). This assumes the mux switches shortly after conversion begins (Figure 5) and that the amplifier and RC forward settling time is sufficient to settle the input capacitor before acquisition begins.
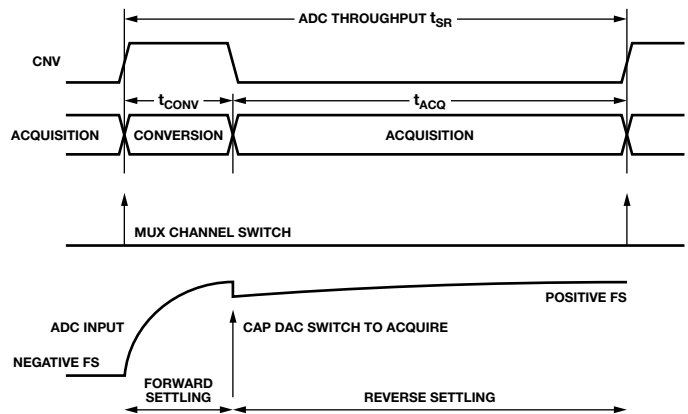

Figure 5. Multiplexed timing.

This can be checked for the calculated RC bandwidth by using Table 1. From the table, 11 time constants are needed to settle a full-scale step to 16 bits (Table 1). For the calculated RC, the forward settling time of the filter is 11 × 40.49 ns = 445 ns, which is much less than the conversion time of 710 ns. The forward settling does not necessarily have to occur completely during the conversion time (before the cap DAC gets switched to the input), but the combined forward and reverse settling time should not exceed the required throughput rate. Forward settling is less important for low-frequency inputs, as the rate of change of the signal is much lower.

Table 1. Number of Time Constants to Settle to N-Bit Resolution

Resolution (Bits)	LSB (%FS)	No. of Time Constants to 1- LSB Error
6	1.563	4.16
8	0.391	5.55
10	0.0977	6.93
12	0.0244	8.32
14	0.0061	9.70
16	0.0015	11.09
18	0.00038	12.48
20	0.000095	13.86
22	0.000024	15.25

With an approximate filter bandwidth calculated, the individual values of R_{EXT} and C_{EXT} can be chosen. The calculations above assume that C_{EXT} = 2.7 nF. This is a typical value in application circuits shown on data sheets. If a larger capacitor were chosen, there would be greater attenuation of the kick when the cap DAC is switched in. However, the larger the capacitance, the greater the chance the driving amplifier will become unstable, especially as the value of R_{EXT} gets smaller for a given bandwidth. If the value of R_{EXT} is too small, the amplifier phase margin will be degraded, potentially causing the amplifier output to ring or become unstable. Amplifiers with low output impedance should be used to drive loads with smaller series R_{EXT}. A stability analysis can be performed using Bode plots for the RC combination and amplifier to verify sufficient phase margin. It is best to choose a capacitance value of 1 nF to 3 nF and a reasonable resistance value that will keep the driving amplifier stable. It is also important to use capacitors with a low voltage coefficient, such as NP0 types, to keep distortion low.

It is important that the value of R_{EXT} keeps the level of distortion within requirements. Figure 6 shows the effect of the resistance of the driving circuit on distortion as a function of frequency for the AD7690. Distortion increases with both input frequency and source resistance. The cause of this distortion is mainly the nonlinear nature of the impedance presented by the cap DAC.
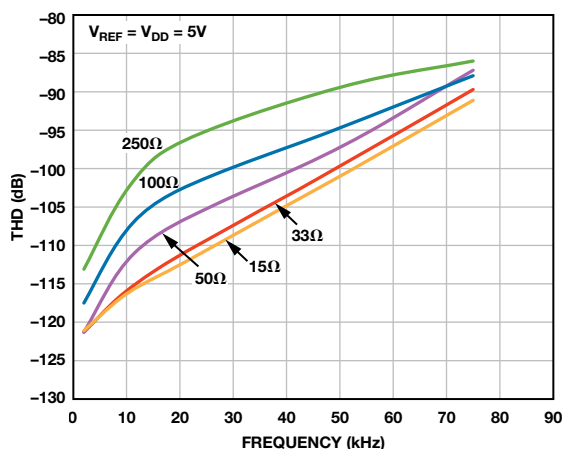

Figure 6. Effect of source resistance on THD vs. input frequency.

Larger series resistance values can be tolerated for low input frequencies (<10 kHz). The distortion is also a function of the input signal amplitude; a lower amplitude will allow a higher value of resistance for the same distortion level. Calculating for R_{EXT} in the example above, where τ = 51.16 ns and C_{EXT} is assumed to be 2.7 nF, yields a resistor value of 18.9 Ω. These are close to common values seen in application sections of Analog Devices data sheets.

The nominal RC values calculated here are useful guidelines, not a final solution. Choosing the right balance between the R_{EXT} and C_{EXT} requires knowledge of the input frequency range, how much capacitance the amplifier can drive, and the acceptable level of distortion. In order to optimize the RC value, it is important to experiment with actual hardware to arrive at the best performance.

Selecting a Suitable Amplifier

In the previous section, we calculated the RC bandwidth suitable for the ADC input, based on input signal and ADC throughput. Next, this information must be used to select a suitable amplifier to drive the ADC. The following aspects will be considered:

- Amplifier large and small signal bandwidth
- Settling time
- Amplifier noise specification and effect on system noise
- Distortion
- Headroom requirements for distortion and resulting supply rails

An amplifier's *small-signal bandwidth* is typically specified on its data sheet. Depending on the type of input signal, however, the *large-signal bandwidth* may be more important. This is especially the case for high input frequencies (>100 kHz) or multiplexed applications—due to the large voltage swings—and forward settling of the input signal is more critical. For example, the ADA4841-1 has an 80-MHz small-signal bandwidth (20 mV p-p signal), but its large-signal bandwidth is 3 MHz (2 V p-p signal). In the above example, using the AD7980, the calculated RC bandwidth was 3.11 MHz. The ADA4841-1 is a good choice for lower input frequencies, as its 80-MHz small-signal bandwidth is more than sufficient for reverse settling, but it would struggle in a multiplexed application—where the RC bandwidth requirement increases to 3.93 MHz for a large signal swing. A more suitable amplifier in this case would be the ADA4897-1, which has a 30 MHz large-signal bandwidth. In general, the small/large signal bandwidth of the amplifier should be at least two to three times greater than the RC bandwidth, depending on whether the reverse or forward settling is dominant. This is especially applicable if the amplifier stage is required to provide voltage gain, which will reduce the available bandwidth; an amplifier with even wider bandwidth may be required.

Another way of looking at the forward settling requirement is to look at the amplifier's settling-time specification, usually the time required to settle to a percentage of the specified step size. For 16- to 18-bit performances, settling to 0.001% is typically required—but most amplifiers are specified for 0.1% or 0.01%, with varying step sizes; hence, some compromises with the numbers are needed in order to get a good idea whether the settling behavior could be acceptable for the ADC throughput. The ADA4841-1 specified settling time to 0.01% is 1 μs for an 8-V step. In a muxed application driving the AD7980 at 1 MSPS (1-μs period), it will not be able to settle the input in time for a full-scale step, but a lower throughput of, say, 500 kSPS may be possible.

The RC bandwidth is important in determining the maximum amount of noise allowed in the amplifier. Amplifier noise is generally specified by low-frequency 1/f noise (0.1 Hz to 10 Hz) and wideband noise spectral density at a higher frequency on the flat part of the noise curve (Figure 7).
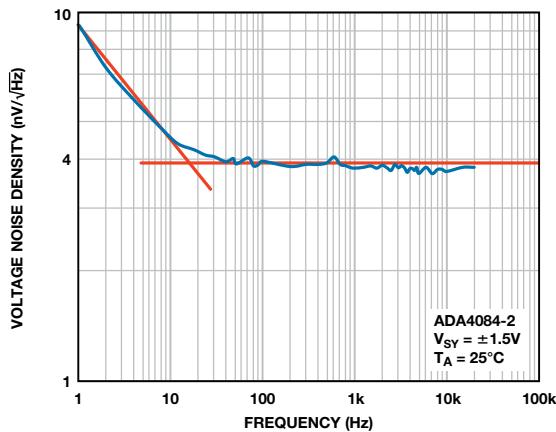

Figure 7. Voltage noise vs. frequency for the ADA4084-2.

The total noise referred to the input of the ADC can be calculated as follows. First, calculate the noise due to the wideband spectral density of the amplifier over the RC bandwidth

$$v_{n,\,rms} = N e_{n,\,rms} \sqrt{\frac{\pi}{2} BW_{RC}}$$

where e_n = noise spectral density in nV/$\sqrt{\text{Hz}}$, N = amplifier circuit noise gain, and BW_{RC} = RC bandwidth in Hz.

Next, add in the low-frequency 1/f noise, which is usually specified peak-to-peak and needs to be converted to rms, typically using this equation

$$v_{n,1/f,\,rms} = N \frac{v_{n,1/f,\,pk-pk}}{6.6}$$

where $v_{n,1/f,\,pk-pk}$ = 1/f peak-to-peak noise voltage and N = amplifier circuit noise gain.

Total noise is then given by the root-sum-square:

$$v_{n,\,total} = \sqrt{v_{n,\,rms}^2 + v_{n,1/f,\,rms}^2}$$

This total noise should be ~1/10 of the noise of the ADC in order to have a minimal effect on the overall SNR. Higher noise may be allowable, depending on the target system's SNR. For example, if the ADC's SNR = 91 dB, with V_{REF} = 5 V, then the total noise should be less than or equal to

$$\frac{5\,\text{V}}{2\sqrt{2}} 10^{\left(-\frac{91\,\text{dB}}{20}-1\right)} = 5\,\mu\text{V rms}$$

From this number, it is easy to work out maximum allowable specifications for 1/f noise and wideband noise spectral density. Assuming that the amplifier under consideration has negligible 1/f noise, operates at unity gain, and uses a filter with the RC bandwidth calculated previously, 3.11 MHz, then

$$v_{n,\,rms} = 5\,\mu\text{V} \Rightarrow e_{n,\,rms} = \frac{5\,\mu\text{V}}{(1)\sqrt{\frac{\pi}{2}(3.11\,\text{MHz})}} = 2.26\,\text{nV/}\sqrt{\text{Hz}}$$

Thus, the amplifier must have a wideband noise spectral density ≤ 2.26 nV/$\sqrt{\text{Hz}}$. The ADA4841-1 meets this criterion with a specification of 2.1 nV/$\sqrt{\text{Hz}}$.

Another important specification to consider for the amplifier is the distortion at a particular input frequency. Typically, for best performance, total harmonic distortion (THD) of ~100 dB is required at 16 bits and ~110 dB for 18-bit ADCs at the input frequency of interest. Figure 8 shows a typical distortion vs. frequency plot for the ADA4841-1 for a 2-V p-p input signal.
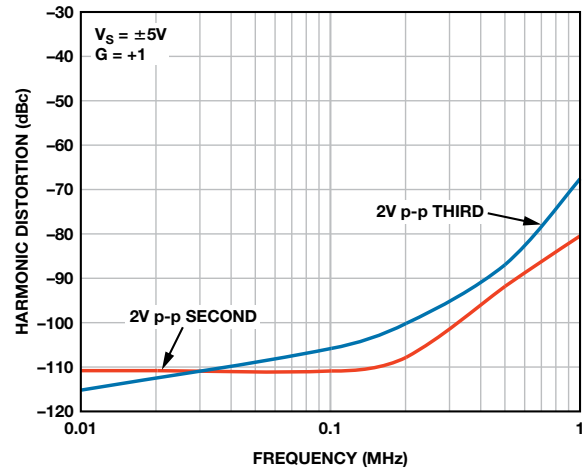

Figure 8. Distortion vs. frequency for the ADA4841-1.

Instead of showing total harmonic distortion, the plot is broken out into the generally most dominant second and third harmonic components. The ADA4841-1 is sufficiently clean to drive an 18-bit ADC up to ~30 kHz with excellent distortion characteristics. As the input frequency approaches 100 kHz and beyond, the distortion performance begins to degrade. For lower distortion at higher frequencies, a higher-power, wider-bandwidth amplifier will be required. Larger signals will also reduce performance. For an ADC input of 0 V to 5 V, the distortion performance signal range increases to 5-V p-p. This will produce differing performance from the distortion plot shown in Figure 8, so the amplifier potentially requires testing to make sure it still meets requirements. Figure 9 compares distortion performance at several output voltage levels.
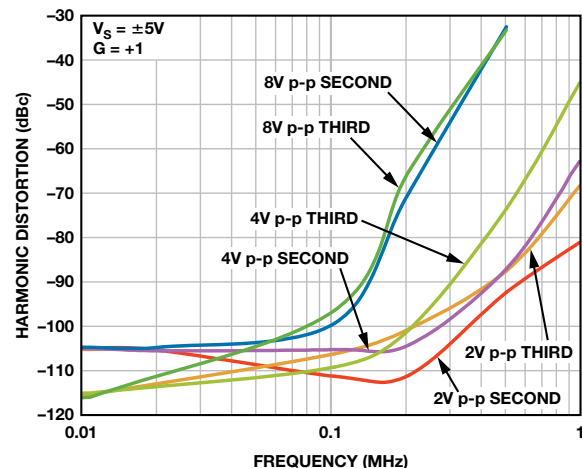

Figure 9. Distortion vs. frequency for various output voltage levels.

The THD can also be affected by the headroom—the difference between the amplifier's maximum practical input/output swing and the positive and negative supply rails. Amplifiers can have rail-to-rail inputs and/or outputs, or require up to 1 V or more headroom. Even with rail-to-rail inputs/outputs, it is difficult to get good distortion if running at a signal level that is close to the rails of the amplifier. For this reason, it is a good idea to choose supply levels that keep the maximum input/output signal away from the rails. Consider, for example, an ADC with a 0 V-to-5-V input range driven by an ADA4841-1 amplifier and a need to maximize the range of the ADC. The amplifier has a rail-to-rail output and a 1-V headroom requirement on the input. If used as a unity gain buffer, at least 1-V input headroom is needed, so the positive supply must be at least 6 V. The output is rail to rail but still can only drive to within ~25 mV of ground or the positive rail, so a negative rail is needed in order to drive all the way to ground. The negative rail could be –1 V, for example, in order to leave a margin for distortion performance.

The negative supply could be eliminated if it were feasible to lose some SNR by accepting a reduction in the ADC input range. For example, if the ADC's input range were to be reduced to 0.5 V to 5 V, this 10% loss of the ADC range would result in a ~1-dB reduction in SNR. However, this would allow the negative rail to be connected to ground, thus eliminating the circuitry necessary to generate the negative supply, reducing power consumption and cost.

Thus, when selecting the amplifier, it is important to consider the input and output signal range requirements, as this will determine the supply voltage needed. In this example, an amplifier rated for 5-V operation would not suffice; the ADA4841-1 is specified up to 12 V, however, so using a higher supply voltage will allow it to work well—with adequate supply margins.

Additional Information About the Featured Devices

Low-Power, Low-Noise, Low-Distortion Operational Amplifier Has Rail-to-Rail Output

The ADA4841-1 low-power op amp's 2-nV/$\sqrt{\text{Hz}}$ wideband noise and –110-dBc spurious-free dynamic range (SFDR) make it ideal for driving 16- and 18-bit PulSAR® ADCs—and for use in portable instrumentation, industrial process control, and medical equipment. Unity-gain stable, its specifications include 60-μV input offset voltage, 114-dB open-loop gain, 114-dB common-mode rejection, 80 MHz bandwidth (–3 dB), 12-V/μs slew rate, and 175-ns settling time to 0.1%. The input signal can extend 100 mV below the negative rail, and the output can swing to within 100 mV of either rail, providing true single-supply capability. Operating on a single 2.7-V to 12 V supply or ±1.5-V to ±6-V dual supplies, the ADA4841-1 consumes 1.1 mA in *normal* mode and 40 μA in *power-down* mode. Available in an 8-lead SOIC package, it is specified from –40ºC to +125ºC and priced at $1.59 in 1000s.

Low-Noise, Low-Power Op Amps Feature Rail-to-Rail Outputs

The ADA4897-1 low-noise, high-speed operational amplifier features rail-to-rail outputs, 1 nV/$\sqrt{\text{Hz}}$ voltage noise, 2.8-pA/$\sqrt{\text{Hz}}$ current noise, 230-MHz bandwidth, 120-V/μs slew rate, 45-ns settling time, and unity-gain stability, making it ideal for a variety of applications, including ultrasound, low-noise preamplifiers, driving high-performance ADCs, and buffering high-performance DACs. Operating on a single 3-V to 10-V supply, the AD4897-1 draws 3 mA. Available in 8-lead MSOP, LFCSP, and SOIC packages, it is specified from –40°C to +125°C and priced from $1.89 in 1000s.

16-Bit, 1-MSPS Successive-Approximation ADC Operates on 7 mW

The AD7980 low-power successive-approximation ADC achieves 16-bit resolution with no missing codes at a 1-MSPS sampling rate. Accepting pseudo-differential inputs with a 0-to-V_{REF} range, it specifies 91.5-dB signal-to-noise-and-distortion (SINAD), –110-dB total harmonic distortion (THD), and ±1.25-LSB maximum integral nonlinearity. Its successive-approximation architecture ensures that there will be no pipeline delays; and daisy-chaining allows several ADCs to share a single bus. Automatically powering down between conversions, its power consumption scales with throughput rate. Operating on a single 2.5-V supply, the AD7980 consumes 7 mW at 1 MSPS, 70 μW at 10 kSPS, and 350 pA in *standby* mode. Available in a 10-lead MSOP package, it is specified from –40ºC to +85ºC and priced from $11.95 in 1000s.

References

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