Noise-Reduction Network for Adjustable-Output Low-Dropout Regulators

By Glenn Morita

Introduction

Noise is extremely important to designers of high-performance analog circuits, especially high-speed clocks, analog-to-digital converters, digital-to-analog converters, voltage-controlled oscillators, and phase-locked loops. A low-dropout regulator (LDO) can power these circuits. A key to reducing noise is keeping the LDO's noise gain close to unity without compromising either ac performance or dc closed-loop gain.

This article describes how a simple RC network can reduce the output noise of an adjustable-output, low-dropout regulator. Experimental data demonstrates the efficacy of this simple technique. Although noise reduction is its primary focus, the RC network also improves power-supply rejection and load-transient response.

Figure 1 shows a simplified block diagram of a typical adjustable-output LDO. The output voltage, V_{OUT}, is the product of the reference voltage and the dc closed-loop gain of the error amplifier: $V_{OUT} = V_R \times (1 + R1/R2)$, where $(1 + R1/R2)$ is the dc closed-loop gain of the error amplifier.

The error-amplifier noise, V_N, and reference-voltage noise, V_{RN}, are multiplied by the same factor, resulting in output noise that increases in proportion to the programmed output voltage. This results in a modest increase in the output noise for output voltages less than a factor of two greater than the reference voltage, but even this modest increase may be unacceptable in sensitive applications.
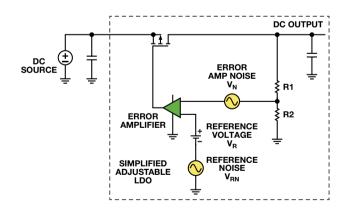

Figure 1. Simplified adjustable LDO block diagram shows internal noise sources.

LDO Noise

The major sources of noise in LDOs are the internal reference voltage and the error amplifier. Modern devices operate with internal bias currents of a few hundred nanoamps or less to achieve quiescent currents of up to 15 µA. These small currents require bias resistors of up to 1 GΩ, resulting in noisier error-amplifier and reference-voltage circuits as compared to discrete implementations. Typical LDOs use a resistive divider to set the output voltage, so the noise gain is equal to the ac closed-loop gain, which as it turns out, is the same as the dc closed-loop gain.

Reducing LDO Noise

Two major methods for reducing LDO noise are filtering the reference and reducing the noise gain of the error amplifier. Some LDOs enable an external capacitor to filter the reference. In fact, many so-called ultralow noise LDOs require the use of an external noise-reduction capacitor to achieve their low-noise specifications. The drawback of this technique is that both the error-amplifier noise and any residual reference noise are still amplified by the ac closed-loop gain. This results in noise that is proportional to the output voltage.

Reducing the noise gain of the error amplifier can produce an LDO where the output noise does not increase dramatically with output voltage. Unfortunately, this is not possible for fixed-output LDOs because the feedback node is not accessible. Fortunately, this node is readily accessible in adjustable-output LDOs.

Figure 2 shows an adjustable-output LDO where R1 and R2 set the output voltage. The network formed by R3 and C1 reduces the ac gain of the error amplifier. To ensure stability with LDOs that have low-phase margin or are not unity-gain stable, choose R3 to set the amplifier's high-frequency gain to approximately 1.1. To reduce noise in the 1/f region, choose C1 to set the low-frequency zero to less than 10 Hz.
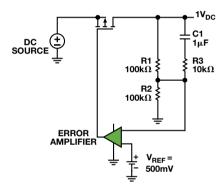

Figure 2. Simple RC network reduces noise gain of an adjustable-output LDO.

Figure 3 compares the ac closed-loop gain with a properly designed noise-reduction network to the open-loop gain and unmodified closed-loop gain. With the noise-reduction network, the ac gain is close to unity for much of the bandwidth, so the reference noise and error amplifier noise are amplified to a lesser degree.
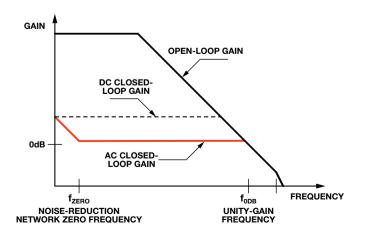

Figure 3. LDO loop gains vs. frequency with noise reduction network.

Figure 4 shows the effect of the noise-reduction network on the noise spectral density of the ADP125 LDO. For comparison, the plot shows the noise spectral density at 4 V with and without the noise-reduction network, as well as the noise spectral density at unity gain.

Note the significant improvement in noise performance between 20 Hz and 2 kHz. Above the zero created by R1 and C1, the noise characteristic with the noise-reduction network is nearly the same as it is at unity gain. Above 20 kHz, the noise spectral density plots converge because the closed-loop gain of the error amplifier meets the open-loop gain, and no further reduction in noise gain is possible.
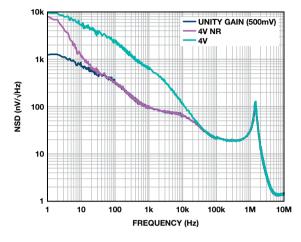

Figure 4. Noise spectral density of the ADP125 adjustable-output LDO.

Power Supply Rejection

The power-supply rejection ratio (PSRR) over this frequency range also improves. PSRR is a measure of how well a circuit suppresses extraneous signals (noise and ripple) that appear on the power supply input to keep them from corrupting the circuit output. PSRR is defined as $PSRR = VE_{IN}/VE_{OUT}$. This can also be expressed in decibels: $PSR = 20 \times \log(VE_{IN}/VE_{OUT})$, where VE_{IN} and VE_{OUT} are the extraneous signals appearing at the input and output.

For most analog circuits, PSR applies to the pins that supply power to the inner workings of the circuit. With LDOs, however, the input pin supplies power to the internal circuitry as well as load current to the regulated output.

Improving PSR

An additional benefit of using a noise-reduction network to reduce the output noise of an adjustable-output LDO is that the low-frequency PSR is also improved. R1, R3, and C1 in Figure 2 form a lead-lag network with a zero at approximately $1/(R1 \times C1)$ and a pole at approximately $1/(R3 \times C1)$. The lead-lag network acts as a feed-forward function in the compensation loop and therefore improves the PSR. The amount of improvement, in dB, is approximately $20 \times \log(1 + R1/R3)$ for frequencies below where the closed-loop gain and open-loop gain converge.

Figure 5 shows the effect of the noise-reduction network on the PSRR of the ADP7102 adjustable-output LDO. With a 9-V output, R1 = 64 kΩ, R2 = 10 kΩ, R3 = 1 kΩ, and C1 = 1 μF. The zero created by R1 and C1 at about 2.5 Hz is evident by the improvement in PSRR above 10 Hz. The overall PSRR increases by about 17 dB from 100 Hz to 1 kHz. The improvement decreases until about 20 kHz where the open-loop gain and closed-loop gain converge.
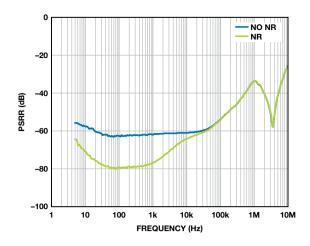

Figure 5. PSRR of the ADP7102/ADP7104 adjustable-output LDO with and without a noise-reduction network.

Transient-Load Improvement

The noise-reduction network also improves the LDO's transient-load response. Again, R1, R3, and C1 perform a feed-forward function in the compensation loop. High-frequency components of the load transient—sensed by the error amplifier without attenuation—allow the error amplifier to respond quickly to the load transient. Figure 6 shows the load transient response of an ADP125 with and without the noise-reduction network. With the noise-reduction network, the LDO is able to respond to the load transient in less than 50 μs, as compared to 500 μs without the network.
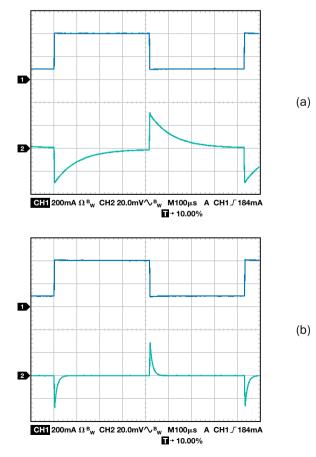

Figure 6. Transient-load response of the ADP125 adjustable-output LDO (a) without noise-reduction network (b) with noise-reduction network.

Effect on Start-up Time

One drawback to the noise-reduction network is that it significantly increases the start-up time. Figure 7 shows the start-up time of the ADP125 with and without the noise-reduction network. The normal start-up time is about 600 µs. The start-up time increases to 6 ms with C1 = 10 nF, and to 600 ms with C1 = 1 µF. The increase in start-up time should not be an issue for applications that do not switch the LDO off and on once the circuit is fully powered.
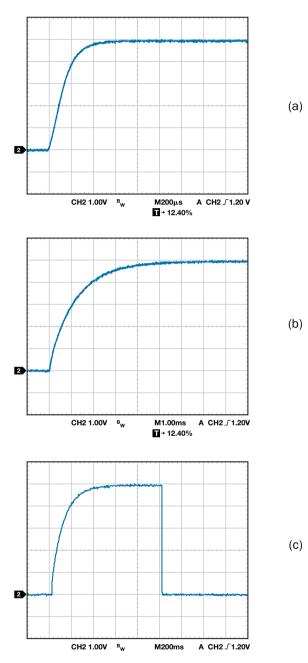

Figure 7. Start-up time of the ADP125 adjustable-output LDO (a) without noise-reduction network (b) with noise-reduction network, C1 = 10 nF, (c) with noise-reduction network, C1 = 1 µF.

Conclusion

The noise, power-supply rejection, and transient performance of an adjustable-output LDO can be improved significantly by adding a simple RC noise-reduction network, bringing significant benefits to noise-sensitive applications such as high-speed clocks, analog-to-digital converters, digital-to-analog converters, voltage-controlled oscillators, and phase-locked loops.

This technique will work with LDOs with architectures similar to that shown in Figure 2, where both the reference-voltage noise and the error-amplifier noise are amplified by the dc closed-loop gain, such that the output noise scales with the output voltage. LDOs such as the ADP125, ADP171, ADP1741, ADP1753, ADP1755, ADP7102, ADP7104, and ADP7105 all share this general architecture and will benefit greatly from the use of a noise-reduction network.

Newer, ultralow-noise LDOs such as the ADM7151 will not benefit from the noise-reduction network because the architecture uses the LDO error amplifier in unity gain, so the reference voltage is equal to the output voltage. In addition, the internal reference filter has a pole below 1 Hz, heavily filtering the reference voltage and virtually eliminating any reference noise contribution.
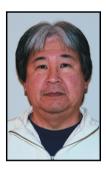
References

Morita, Glenn. "Low-Dropout Regulators—Why the Choice of Bypass Capacitor Matters." *Analog Dialogue*, Volume 45, Number 1, 2011.

Morita, Glenn. AN-1120 Application Note. *Noise Sources in Low-Dropout (LDO) Regulators*. Analog Devices, Inc., 2011.

Author

Glenn Morita [glenn.morita@analog.com] graduated from Washington State University with a BSEE in 1976. His first job out of school was at Texas Instruments, where he worked on the infrared spectrometer instrument for the Voyager space probe. Since then, Glenn has worked as a designer in the instrumentation, military and aerospace, and medical industries. In 2007, he joined ADI as an applications engineer with the Power Management Products Team in Bellevue, WA. He has over 25 years of linear and switch-mode power supply design experience at power levels ranging from microwatts to kilowatts. Glenn holds two patents for harvesting energy from body heat to power implantable cardio-defibrillators and an additional patent for extending battery life in external cardio-defibrillators. In his spare time, he enjoys collecting minerals, faceting gemstones, photography, and visiting the national parks.