Accurate Analog Controller Optimizes High-Efficiency Li-Ion Battery Manufacturing

By Wenshuai Liao and Luis Orozco

Energy conservation and environmental protection play an important role in people's daily lives, with the introduction of affordable hybrid and electric vehicles increasing awareness even more. Both technologies use a large quantity of rechargeable batteries, with high-quality, high-power Li-Ion cells representing the best solution at this time. These batteries have been widely used in laptop computers, cell phones, digital still cameras, camcorders, and other portable equipment, but manufacturing efficiency has not been a major concern because of their low storage capacity, typically fewer than 5 Ah per cell or cell pack. A typical cell pack contains fewer than a dozen cells, so matching is also not a major concern.

One approach to energy conservation is storing energy during nonpeak times to compensate for peak usage. Batteries used for vehicles or energy storage have much higher capacity, typically in the hundreds of amp-hours. This is achieved with a large number of small cells or a few high-capacity batteries. For example, one electric vehicle model uses about 6800 Type-18650 Li-Ion cells, weighing up to 450 kg. Because of this, faster battery manufacturing with higher efficiency and better control is required to meet market needs at a lower cost.

Li-Ion Battery Manufacturing Overview

Figure 1 shows an overview of the Li-Ion battery manufacturing process. Battery formation and testing at the end-of-line conditioning step are the process bottlenecks, in addition to having the greatest impact on battery life and quality.

With today's technology, formation must be done at the cell level, and can take hours, or even days, depending on the battery chemistry. A 0.1 C (C is the cell capacity) current is typically used during formation, so it would take 20 hours to go through a full charge and discharge cycle. Formation can account for 20% to 30% of the total battery cost.



Figure 1. Li-lon battery manufacturing process.

Electrical testing typically uses a 1 C charging current and a 0.5 C discharge current, but each cycle still requires one hour to charge the battery and two hours to discharge it, and a typical test sequence encompasses several charge-discharge cycles.

Formation and electrical testing have stringent accuracy specifications, with the current and voltage controlled to within $\pm 0.05\%$. In contrast, the accuracy can be $\pm 0.5\%$ for voltage and $\pm 10\%$ for current when charging batteries in portable equipment such as cell phones and laptops. Figure 2 shows typical Li-Ion charge and discharge profiles.



Figure 2. Typical Li-Ion cell charge and discharge profiles.

Linear or Switching Formation and Testing System

The top factors that must be taken into account when selecting a manufacturing method are power efficiency, system accuracy, and cost. Other factors like small size and easy maintenance are also important, of course.

To meet the high-accuracy requirements in battery manufacturing, system designers traditionally use linear voltage regulators, which easily meet the accuracy requirements but have low efficiency. With low-capacity batteries, this may be a good trade-off, but some manufacturers can still use switching technology to their advantage. The decision hinges on efficiency, channel cost, and current. As a guideline, switching technology will provide higher efficiency at the same per-channel cost for cells with higher than 3 Ah capacity. Table 1 shows a comparison of different cell categories in terms of power capacity and end function.

Battery Size	Small	Medium	Large
Capacity (Ah)	Less than 2	10 To 15	30 To 100
Applications	Cell phone, digital still camera, camcorder	Laptop computer	HEV, EV, scooter
Number of Channels	~512	~768	16 To 64
Technical Requirements	Lower drift over temperature and time	Higher accuracy over temperature and time	Highest accuracy over temperature and time Current sharing
Tester Topology	Linear Lower efficiency	Linear or switching Trend towards switching	Switching; Higher efficiency Energy recycling

Table 1. Comparison of Linear and Switching Systems

analog.com/analogdialogue

To produce batteries faster and at lower cost, systems use hundreds or thousands of channels in the formation and testing steps, with the topology of the tester depending on the system's total energy capacity. High current flow in the tester will cause the temperature to rise significantly, increasing the challenge of maintaining high measurement accuracy and repeatability over time.

During the discharge phase, the stored energy must go somewhere. One solution is to discharge the batteries into resistive loads, converting the energy into wasted heat. A much better solution is to recycle the energy, using precision control to feed current from the discharging cells into another group of charging cells. This technique achieves significantly higher tester efficiency.

The energy balance is typically implemented via a dc-bus and a bidirectional PWM converter on each cell. The dc-bus voltage, which depends on the particular system, can be 12 V, 24 V, or even up to 350 V. For the same amount of power, lower voltage buses have higher currents and higher losses due to conductor resistance. Higher voltages have additional safety concerns and require expensive power and isolation electronics. Figure 3 shows a typical switching topology for energy recycling. The energy can be recycled directly between cells (red path), between cells via a dc link bus (green path), or it can be returned to the power grid (purple path). These flexible, high-efficiency designs can result in lower production costs and can achieve better than 90% efficiency.

Although this technology offers many benefits, it also introduces several technical challenges. The voltage and current control loops must be fast enough and must maintain high accuracy over time and temperature. Using air- or water cooling is helpful, but it's more important to start with low-drift circuits. The system includes switching power supplies, so the supply ripple must be suppressed at a reasonable cost. It is also important to minimize the time it takes to calibrate the system, as it doesn't generate revenue when down for calibration.

Control-Loop Design: Analog or Digital

Each system has one loop for voltage control and another for current control, as shown in Figure 4. For cells used in vehicles, fast-ramping current is required during vehicle acceleration, so this has to be simulated during testing. The fast rate of



Figure 3. Switching systems with power recycling feature.



Figure 4. Control loops in battery manufacturing systems.

change and wide dynamic range make the current control loop a challenge to design.

A system requires four different control loops, which may be implemented in either analog or digital domains: constant current (CC) charge, CC discharge, constant voltage (CV) charge, and CV discharge. Switching between CC and CV modes must be clean, without glitches or peaks.

Figure 5 shows a block diagram of a digital control loop. The microcontroller or DSP continuously samples the voltage and current; a digital algorithm determines the duty cycle for the PWM power stage. This flexible method allows field upgrades and bug fixes, but has a few drawbacks. The ADCs must sample at more than twice the loop bandwidth, with most systems sampling at 10 times the loop bandwidth. This means that the bipolar-input ADC must run at 100 kSPS to

cover charge and discharge modes with a single converter and shunt resistor. Some designers use 16-bit, 250-kSPS ADCs for faster, higher-accuracy systems. As part of the control loop, the ADC's accuracy sets the overall system accuracy, so it is important to select fast, low-latency, low-distortion ADCs, such as the 6-channel, 16-bit, 250-kSPS AD7656.

In multichannel systems, each channel will typically require a microcontroller and a set of dedicated ADCs. The microcontroller handles the data acquisition, digital control loop, PWM generation, control, and communication functions, so its processing capability must be very high. In addition, because the processor has to handle multiple parallel tasks, jitter in the PWM signal can be a problem, especially when the PWM duty cycle is low. As part of the control loop, the microprocessor affects the loop bandwidth.



Figure 5. Digital control loops.

Figure 6 shows a battery test system that uses analog control loops. Two DAC channels control the CC and CV set points. The AD8450/AD8451 precision analog front end and controller for battery test and formation systems measures the battery voltage and current, and compares it to the setpoints. The CC and CV loops determine the duty cycle of the MOSFET power stage. When the mode changes from charge to discharge, the polarity of the in-amp that measures the battery current reverses to ensure that its output remains positive and switches inside the CC and CV amplifiers select the correct compensation network. This entire function is controlled via a single pin with standard digital logic.

In this implementation, the ADC monitors the system, but it's not part of the control loop. The scan rate is unrelated to control-loop performance, so a single ADC can measure current and voltage on a large number of channels in multichannel systems. This is true for the DAC as well, so a low-cost DAC can be used for multiple channels. In addition, a single processor only needs to control the CV and CC set points, mode of operation, and housekeeping functions, so it can interface with many channels. The processor doesn't determine the control-loop performance, so high performance isn't required.

The ADP1972 PWM generator uses a single pin to control buck- or boost-mode operation. The interface between the analog controller and the PWM generator consists of lowimpedance analog signals that don't suffer from the jitter that causes problems in the digital loop. Table 2 shows how an analog loop can offer higher performance and lower cost than a digital loop.



Figure 6. Analog control loop.

Table i	2. Com	parison	of Ana	log and	Digital	Control	Loops

	Digital Solution	Analog Solution	Analog Benefits
Loop Bandwidth	Varies with amplifier, ADC, microprocessor 20 kHz with 250-kSPS ADC	Depends on amplifiers; 1.5 MHz for AD845x at G = 66	Faster control
Accuracy	0.05% or worse; depends on ADC and algorithm	0.04% or better; depends on AD845x	Higher accuracy
Switching Frequency	Depends on algorithm and microprocesor speed; low-frequency jitter	Up to 300 kHz; depends on ADP1972 Clean PWM output	Lower-cost power solution
Power Efficiency	Trade-off between resources and buck/ boost switching frequency	90%+; no limitation from chipset	Higher efficiency
Power Electronics	Large, expensive components	Small, low-cost component	Smaller; lower cost
Converter Sharing	No; expensive, dedicated bipolar-input ADC	Yes; multichannel, low voltage unipolar ADC	Lower cost
Total Solution	Expensive ADCs and power electronics; large software investment	Low-cost ADCs and power electronics; no software required	Lower cost including hardware, calibration, and operation; higher performance

System Accuracy over Temperature

Calibration will remove most of the initial system errors. Remaining errors include the amplifier CMRR, the nonlinearity of the DAC used to control the current and voltage set points, and errors due to temperature drift. Manufacturers specify different temperature ranges, but 25°C ±10°C is one of the most common, and will be used in this example.

This design uses a battery that varies from 2.7 V when fully discharged to 4.2 V when fully charged, a full-scale current of 12 A using a 5-m Ω shunt, a gain of 66 for the AD8450's current-sense amplifier, and a gain of 0.8 on the diff-amp that measures the battery voltage.

The current-sense resistor drift can account for a large part of the total system error. A Vishay bulk metal resistor; part number Y14880R00500B9R, with a 15-ppm/°C maximum temperature coefficient, reduces drift. The AD5689 dual 16-bit *nano*DAC+TM digital-to-analog converter, which specifies 2-LSB maximum INL, reduces nonlinearity. The ADR4540 4.096-V reference, which specifies a 4-ppm/°C maximum temperature coefficient, is a good compromise between current and voltage setpoints. The DAC INL adds about 32 ppm of full scale error after dividing by the current-sense amplifier gain of 66, and the reference contributes 40 ppm of gain error.

The current-sense amplifier has 116-dB minimum CMRR at a gain of 66. If the system is calibrated with a 2.7-V battery, a 40-ppm full-scale error would occur with a 4.2-V battery. In addition, the CMRR will vary by 0.01 μ V/V/°C, or 0.1 μ V/V

over the 10°C temperature range. The offset voltage drift of the current-sense amplifier is 0.6 μ V/°C max, so a 10°C temperature excursion would result in 6 μ V of offset, or 100 ppm of full scale.

Finally, the gain drift of the current-sense amplifier is 3 ppm/°C max, for a total drift of 30 ppm over 10°C. The sense resistor drift is 15ppm/°C, so it adds 150 ppm gain drift over 10°C. Table 3 summarizes these error sources, which produce a total full-scale error of just under 0.04%. A big percentage of this error is from the shunt resistor, so a lower drift shunt resistor can be used to improve system accuracy if necessary.

Similarly, for the voltage input, the 2-LSB DAC INL is equivalent to 31 ppm error referred to the 5.12-V full-scale input. As the battery voltage changes between 2.7 V and 4.2 V, the diff-amp's 78.1-dB CMRR creates 187- μ V offset error, or 36.5 ppm of full scale. The additional error from CMRR drift is well under 1 ppm, so we can neglect it.

The offset drift of the diff-amp is 5 μ V/°C, or 10 ppm of full scale over 10°C. The gain drift of the diff-amp is 3 ppm/°C, or 30 ppm over 10°C. The reference drift is 40 ppm over 10°C. The total voltage error is 0.015% maximum, as summarized in Table 4.

Achieving high accuracy on the current measurement is more difficult than on the voltage measurement because of the smaller signal level and wider dynamic range. The shunt resistor and in-amp offset drift cause the largest errors over temperature.

Table 3. Current Measurement Error over 10°C Range

		-
Error Source	Error	Units
AD5689R INL	31	ppm FS
AD8450 CMRR	40	ppm FS
AD8450 Offset Drift	100	ppm FS
AD8450 CMRR Drift	3	ppm FS
Total Offset Error	174	ppm FS
ADR4540A Drift	40	ppm reading
AD8450 Gain Drift	30	ppm reading
Shunt-Resistor Drift	150	ppm reading
Total Gain Drift	220	ppm reading
Total Error	0.039	% FS

Table 4. Voltage Measurement Error over 10°C Range

Error	Units
31	ppm FS
36	ppm FS
10	ppm FS
Negligible	ppm FS
77	ppm FS
40	ppm reading
30	ppm reading
70	ppm reading
0.015	% FS
	Error 31 36 10 Negligible 77 40 30 70 0.015

Reducing Calibration Time

The system calibration time can be several minutes per channel, so reducing it can reduce manufacturing cost. At 3 minutes per channel, it would take 4.8 hours to calibrate a 96-channel system. The voltage and current measurement paths are different due to the change in current polarity, and the offset and gain errors will be different for each mode, so they must be calibrated separately. Without low-drift components, temperature calibration would have to be done for each mode, making the calibration time very long.

When the AD845x changes between charge and discharge mode, an internal multiplexer changes the current polarity before it reaches the in-amp and other signal conditioning circuits. Thus, the in-amp will see the same signal regardless of whether it is in charge or discharge mode, and the gain error will be the same in both modes, as shown in Figure 7. The multiplexer resistance will differ in charge and discharge modes, but the high input impedance of the in-amps allows this error to be neglected.

From the system design point of view, having the same offset and gain error in both modes means a single calibration can remove the initial errors in both charge and discharge modes, cutting the calibration time in half. In addition, the very low drift of the AD845x makes a single, room-temperature calibration sufficient, rather than having to calibrate at different temperatures. The time savings can turn into significant cost savings considering the calibration required over the life of the system.

Reducing Ripple

One of the concerns for system designers moving from linear topology to switching topology is the ripple in the voltage and current signals. Every switching power system will have some ripple, but the technology is evolving fast, driven by the voltage-regulator modules in PCs and other high-volume power management applications that require high efficiency at low cost. With careful circuit design and PCB layout, the ripple can be reduced to a level where a switching power supply can power a 16-bit ADC without degrading its performance, as explained in AN-1141 Application Note, Powering a Dual Supply Precision ADC with Switching Regulators. In addition, the data sheet of the ADP1878 synchronous buck controller provides more information on high-power applications. Most switching supplies use a single-stage LC filter, but a two-stage LC filter can be helpful if better ripple and higher system accuracy are needed.

Current Sharing

The AD8450 allows easy pure analog current sharing, making it a fast, cost-effective way to combine multiple channels for formation and testing of high-capacity cells. For example, a 5-V, 20-A single-channel design can be leveraged to generate a 5-V, 60-A system by combining three identical channels. The current sharing bus and control circuits are implemented by the AD8450 and a few passive parts. Compared with single-channel design, this can be cost effective because lowcost power electronics can be used and no extra development time is needed. Details can be found on the AD8450 data sheet.







OFFSET VOLTAGE AND SLOPE ARE THE SAME IN AD845x

Figure 7. The AD845x has the same offset and slope in both charge and discharge modes.

Conclusion

A switching power supply provides a high-performance, cost-effective solution for modern rechargeable-battery manufacturing. The AD8450, AD8451, and ADP1972 simplify the system design with better than 0.05% system accuracy and more than 90% power efficiency, helping to solve the rechargeable-battery manufacturing bottleneck problem and contribute to the wider adoption of environmentally friendly technologies.

References

Wang, Jianqiang, et al. "Study of High-Capacity Single-Body Li-Ion Battery Charging and Discharging System." PEDS2009.

Wolter, M, et al. "End-of-Line Testing and Formation Process in Li-Ion Battery Assembly Lines." 9th International Multi-Conference on Systems, Signals and Devices, 2012 IEEE



Wenshuai Liao [wenshuai.liao@analog.com] is a marketing engineer in ADI's Linear Products Group (LPG) located in Wilmington, Mass. After earning a master's degree in optical engineering from Tsinghua University, Wenshuai spent three years as a 3G Node B RF engineer at Datang Telecommunications Group. He joined ADI in August 2002.



Wenshuai Liao

Also by this Author:

"High-Side Current Sensing with Wide Dynamic Range: Three Solutions"

Volume 44, Number 4

Luis Orozco

Also by this Author:

"Programmable-Gain TIAs Maximize Dynamic Range in Spectroscopy Systems"

Volume 47, Number 2

Luis Orozco [luis.orozco@analog.com] is a system applications engineer in ADI's Industrial and Instrumentation Segment. He focuses on precision instrumentation, chemical analysis, and environmental monitoring applications. Luis joined ADI in February 2011. Prior to joining ADI, he designed data-acquisition equipment for over 10 years.

