# Demystifying High-Performance Multiplexed Data-Acquisition Systems

By Maithil Pachchigar

#### Introduction

High-channel-density data-acquisition systems used for medical imaging, industrial process control, automatic test equipment, and 40G/100G optical communication systems multiplex signals from many sensors to a small number of ADCs that can convert every channel in a sequence. Multiplexing allows the use of fewer ADCs per system, offering significant savings in power, size, and cost. Successive-approximation ADCs often called SAR ADCs for their successive-approximation register—have low latency, making them popular in multiplexed systems that demand fast response to a full-scale input step (worst case) without any settling time issues. Easy to use, SAR ADCs offer low power and small size. This article focuses on the key design considerations, performance results, and application challenges associated with multiplexed data-acquisition systems using high-performance precision SAR ADCs.

#### Multiplexed Data-Acquisition System Challenges

Multiplexed data-acquisition systems demand wideband amplifiers that settle quickly while driving the ADC's fullscale (FS) input range. In addition, switching and sequential sampling of the multiplexer channels must be synchronized with the ADC conversion cycle. The large voltage differential between adjacent inputs makes these systems prone to channel-to-channel crosstalk. To avoid errors, the complete signal chain, including multiplexer and amplifier, must settle to the required accuracy, typically specified as crosstalk error or settling error. Figure 1 shows a block diagram of a data-acquisition system that includes a multiplexer, ADC driver, and SAR ADC.



Figure 1. Block diagram of multiplexed data-acquisition system.

#### Multiplexer

Fast input switching and wide bandwidth of the multiplexer are critical for high performance. The multiplexer's turn-on or turn-off times specify the delay between application of the digital control input and the output crossing 90% of  $V_{OUT}$ , as shown in Figure 2.



Figure 2. Switching time in a typical multiplexer.

A voltage glitch or kickback occurs at the multiplexer input when it switches channels. This kickback is a function of the turn-on and turn-off times, on-resistance, and load capacitance. Large switches with low on-resistance typically result in a large output capacitance that must be charged to a new voltage each time the input is switched. If the output doesn't settle to a new voltage, crosstalk error will occur. Therefore, the multiplexer's bandwidth must be sufficient and a buffer amplifier or large capacitors must be used at the multiplexer input to settle a full-scale step. In addition, the leakage current flowing through the on-resistance will introduce a gain error, so both should be kept small.

#### **ADC Driver**

When the multiplexer input channel is switched, the ADC driver amplifier must settle a large voltage step within the specified sample period. The input can change from negative full-scale to positive full-scale, or vice versa, so a large input voltage step can be created in a small time. The amplifier must have a wide large-signal bandwidth and fast settling time to handle this step. In addition, nonlinear effects appear as a result of slew rate or output current limitations. Also, the driver amplifier must settle the kickback caused by charge rebalancing on the SAR ADC input at the start of the acquisition period. This could become a bottleneck in settling the inputs in a multiplexed system. Settling time issues can be reduced by lowering the throughput rate of the ADC to provide longer acquisition time, thus allowing the amplifier sufficient time to settle to the required accuracy.

Figure 3 shows a timing diagram of a multiplexed dataacquisition system when its input makes a full-scale change. The cycle time of the ADC, which consists of the conversion time plus the acquisition time ( $t_{CYC} = t_{CONV} + t_{ACO}$ ), is usually specified as 1/throughput rate in the data sheet. The capacitive DAC of the SAR ADC is disconnected from the inputs at the start of the conversion, and the multiplexer channel can be switched to the next channel after a small switching delay, t<sub>s</sub>. This allows the maximum time to settle the selected channel. To guarantee performance at maximum throughput, all of the components in the multiplexed system must settle at the ADC input between the time that the multiplexer switches and the end of the acquisition time. The multiplexer channel switching must be properly synchronized with the ADC conversion time. The achievable throughput rate in a multiplexed system is the single ADC throughput rate divided by the number of channels being sampled.



**Figure 3.** Typical timing diagram of a multiplexed data-acquisition system.

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#### **RC Filter at Inputs of Multiplexer**

Some designers use a low-output-impedance buffer to handle the kickback from the multiplexer inputs. The input bandwidths of the SAR ADC (tens of MHz) and ADC driver (tens to hundreds of MHz) are higher than the sampling frequency, and the desired input signal bandwidth is typically in the tens to hundreds of kHz range, so an RC antialiasing filter may be required at the input of the multiplexer to eliminate unwanted signals (aliases) from folding back into the bandwidth of interest and to reduce settling time issues. The value of the filter capacitance used at each input channel should be carefully selected based on the following trade-off: if the capacitance is large, it will help attenuate the kickback from the multiplexer, but it can also make the previous amplifier stage unstable by degrading its phase margin. C0G or NP0 type capacitors are recommended for an RC filter that has high Q, low temperature coefficient, and stable electrical characteristics under varying voltages. A reasonable value of series resistance should be chosen to keep the amplifier stable and limit its output current. The resistance cannot be too large, or the amplifier will not be able to recharge the capacitor after the multiplexer kickback.

#### Multiplexed Data-Acquisition Signal Chain

Figure 4 shows a simplified signal chain for a multiplexed data-acquisition system. One of two differential channels is selected by the ADG774 CMOS multiplexer. To evaluate this system, the positive and negative differential inputs of the ADG774 are switched continuously to generate a full-scale step. Two ADA4899-1 ultralow-distortion op amps buffer the

multiplexer outputs and drive the AD7960 18-bit, 5 MSPS PulSAR<sup>®</sup> ADC. The RC filter (33  $\Omega$ /56 pF) helps to reduce the kickback coming from the capacitive DAC input of the AD7960 and limits the noise going to the AD7960 inputs.

The ADG774 quad 2:1 CMOS multiplexer offers fast switching speed ( $t_{ON}$  = 7 ns,  $t_{OFF}$  = 4 ns), low on-resistance ( $R_{ON}$  = 2.2  $\Omega$ ), wide bandwidth ( $f_{-3dB}$  = 240 MHz), and low power dissipation (5 nW), making it ideally suitable for portable and battery powered instrument. The inputs of the ADG774 are tied to a fixed 5-V reference and a ground, so the output should swing from positive full-scale to negative full-scale. Figure 5 shows a typical profile of on-resistance vs. input voltage over the full 0-V-to-5-V analog-input range and  $-40^{\circ}$ C to  $+85^{\circ}$ C temperature range. This level of performance ensures excellent linearity and low distortion for fast-switching signals.

The output of the ADG774 is connected to a high-inputimpedance amplifier stage. The ADA4899-1 high-speed op amp features ultralow noise (1 nV/ $\sqrt{Hz}$ ) and distortion (-117 dBc), 600 MHz bandwidth, and 310 V/µs slew rate. Operating on +7-V and -2.5-V supplies allows enough headroom to achieve low system noise and distortion. The amplifier's 50 ns settling time of 0.1% for a 2 V p-p input signal, shown in Figure 6, makes it ideal for driving the AD7960.

The AD7960 precision differential ADC offers best-in-class noise and linearity without latency or pipeline delay, high accuracy (18-bit resolution,  $\pm 0.8$ -LSB INL, 99-dB SNR, and -117-dB THD), fast sampling (5 MSPS), low power dissipation, and low cost. Powered from +5 V (VDD1) and +1.8 V



Figure 4. Simplified signal chain for a multiplexed data-acquisition system.





Figure 6. Typical settling time of the ADA4899-1.

(VDD2 and VIO) supplies, it dissipates only 46.5 mW at 5 MSPS when converting in echoed-clock mode. Its core power dissipation scales linearly with throughput, making it well suited for low-power applications with high channel density. The 5 V and 1.8 V supplies can be generated by low-noise LDOs such as ADP7104 and ADP124.

The ADC's full-scale differential input range is set to 5 V or 4.096 V by an external reference. To fully use its dynamic range, the input signals must swing from 0 to  $V_{REF}$ . In this signal chain, the 5-V reference is supplied by the ADR4550 high-precision ( $\pm 0.02\%$  max initial error), low-power (950  $\mu$ A max operating current) voltage reference, which features excellent temperature stability and low output noise. The AD8031 rail-to-rail op amp buffers the external reference. Stable with large capacitive loads, it can drive the decoupling capacitors required to minimize voltage spikes caused by transient currents. The AD8031 is ideal for a wide range of applications, from battery-operated systems with wide bandwidth to high-speed systems where high component density requires low power dissipation.

The AD7960 digital interface offers self-clocked and echoedclock modes using low-voltage differential signaling (LVDS) to enable high-speed data transfer up to 300 MHz (CLK± and D±) between the ADC and the digital host. The LVDS interface allows multiple devices to share a common clock, reducing the number of digital lines and easing signal routing. The lower power dissipation as compared to parallel interfaces is especially useful in multiplexed applications.

The AD7960 returns to acquisition mode about 115 ns after the start of conversion, leaving about 40% of the total 200-ns cycle time to acquire the signal. This relatively long acquisition time relaxes the burden on the amplifier's bandwidth and settling time requirements and makes the differential inputs easier to drive. The 5-MSPS throughput rate allows multiple channels to be multiplexed at fast scan rates, so fewer ADCs are required in high-channel-count systems.

During the conversion, the AD7960 has a quiet-time requirement at 90 ns to 110 ns where the multiplexer inputs must not be switched. Thus, to avoid corrupting the ongoing conversion, the external multiplexer must be switched to less than 90 ns or more than 110 ns after the rising edge of the  $CNV\pm$  start signal. If the analog inputs are switched during this quiet time, the current conversion may be corrupted by up to 15 LSBs. The analog inputs should be switched as early as possible to allow the maximum time to slew a full-scale signal and settle the input.

After every 16 conversions, the multiplexer switches between -5 V and +5 V about 10 ns after the rising edge of CNV±, as shown in Figure 7. This creates a full-scale differential step, so the ADC output change from negative full-scale to positive full-scale as shown in Figure 8.



Figure 7. Oscilloscope plot shows kickback from the internal CAP DAC.



*Figure 8.* AD7960 output shows the ADG774 switching after every 16 conversions.

This switching time delay must be greater than the ADC's 1.6-ns aperture delay. The signal measured at the ADC input shows about 1-V p-p kickback (Figure 7, highlighted in red) from the capacitive DAC in the AD7960. To ensure that the output is fully settled, the driver amplifier must settle this transient before the next conversion starts, within the approximately 80 ns acquisition time of the ADC when running at 5 MSPS. Running the ADC at lower throughput rates provides more acquisition time to settle this kickback, resulting in a lower crosstalk error between the multiplexer input channels and better settling time to a full-scale step.

The signal measured at the multiplexer input also shows a kickback from the channel switching. A buffer amplifier at the multiplexer inputs helps to settle this kickback. If the input buffer amplifier cannot be used for cost or space reasons, an optimized RC filter can be added to the inputs to reduce the effect of the kickback and crosstalk. The value of RC filter used on the multiplexer inputs impacts the overall noise and settling time of the signal chain.

When the multiplexer is static, the output of the dataacquisition system with the AD7960 running at its maximum 5-MSPS throughput rate is about 14 LSBs away from nominal full scale, representing the system's overall gain and offset error. When the multiplexer is switching, the ADA4899-1 driver amplifier helps to settle the output to positive and negative full scale within an acceptable channel-to-channel crosstalk error for most applications. The output error scales exponentially with throughput, reaching a maximum of 0.01% at 5 MSPS, as shown in Figure 9. The zero crosstalk error at lower throughput rates shows that the ADC output settles to its final value during the first conversion.



Figure 9. Crosstalk error vs. throughput as a percentage of fullscale amplitude.

As shown in Figure 10, the crosstalk error relative to full scale is less than 0.001% at 1 V p-p (10% of full scale), and scales linearly with differential input amplitude. The crosstalk error relative to step amplitude is almost flat over the full input span and is always less than 0.01%.



Figure 10. Crosstalk error vs. differential input signal.

This multiplexed signal chain offers optimized performance with the best noise vs. settling time trade-off. These results demonstrate that a wide bandwidth, fast-settling amplifier is required to settle the large voltage step and kickback from the ADC input and to reduce the magnitude of the crosstalk error when multiplexing.

## Multiplexed Data-Acquisition System Layout Considerations

The printed circuit board (PCB) layout is critical for preserving signal integrity and achieving the expected performance from the signal chain. Figure 11 shows the top of the 69 mm  $\times$  85 mm, four-layer evaluation board. Care must be taken with the placement of individual components and routing of various signals on the board. In this case, the input signal is routed from left to right. All of the power supplies and reference pins of the ADC must be decoupled with capacitors placed close to the DUT and connected using short, wide, low-impedance traces, to provide a path for high-frequency currents, minimize EMI susceptibility, and reduce the effect of glitches on the power-supply lines. From the data sheet, recommended values are typically 10 µF and 100 nF. Ground and power planes should be removed beneath the input and output pins of the multiplexer, amplifiers, and ADC to avoid undesired parasitic capacitance. The exposed paddle of the device should be soldered directly to the ground plane of the PCB using multiple vias. Separate sensitive analog and digital sections while keeping the power supply circuitry away from the analog signal path. Fast switching signals, such as CNV± or CLK±, should not run near or cross over analog signal paths to prevent noise coupling to the ADC.

#### Multiplexed Data-Acquisition Applications

The high-performance, multichannel data-acquisition systems used in industrial automation and medical imaging demand wide bandwidth, high accuracy, and fast sampling—all in a small, low-cost form factor. The 5-MSPS throughput rate of the 18-bit AD7960 and 16-bit AD7961 allows more channels to be multiplexed into fewer ADCs, while significantly reducing the cost, power dissipation, and package size. This helps designers meet space, thermal, power, and other key design challenges common to high-channel-density systems.

The excellent linearity and low noise provide enhanced image quality in computed tomography (CT) and digital X-ray (DXR) applications. Switching many channels at high sampling rates into fewer ADCs allows a shorter scanning period and decreased exposure to the X-ray dosage, providing an accurate, affordable diagnosis and a better patient experience. In CT scanners, the pixel current is captured continuously using a single integrator and track-and-hold per channel, with outputs multiplexed to a high-speed ADC. A low-noise analog front end transforms the small current from each pixel into a large voltage, which is then converted into digital data that can be processed.

Multiplexed medical imaging systems, especially CT and DXR, specify typical pixel-to-pixel crosstalk error of  $\pm 0.1\%$  from adjacent pixels and  $\pm 0.01\%$  from nonadjacent pixels. The results presented here suggest that the crosstalk error generated from this multiplexed signal chain is well within the acceptable limits, even at maximum throughput and full-scale range.



**Figure 11.** Top layer of evaluation board for a multiplexed data-acquisition system.

#### Conclusion

High-performance, high-channel-density, multiplexed dataacquisition systems demand reliable performance, functional flexibility, and high accuracy, while meeting power, space, and thermal constraints. This article provides guidelines for choosing multiplexed signal chain components with key design considerations to meet the expected performance, and insights on the trade-offs among throughput, settling time, and noise. This signal chain achieves optimized performance with less than 0.01% of crosstalk error at 5 MSPS at full-scale range.



Maithil Pachchigar [maithil.pachchigar@analog.com] is an applications engineer in ADI's Precision Converters business unit in Wilmington, MA. He joined ADI in 2010 and supports the precision ADC product portfolio and customers in the industrial, instrumentation, medical, and energy segments. Having worked in the semiconductor industry since 2005, Maithil has published several technical articles and application notes. He received an MSEE from San Jose State University in 2006 and an MBA from Silicon Valley University in 2010.



#### Maithil Pachchigar

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