Ask the Applications Engineer—41
LDO Operational Corners: Low Headroom and Minimum Load

LDO Headroom and Its Effects on Output Noise and PSRR

By Glenn Morita

The latest multigigahertz analog circuits, built on deep submicron processes, require ever-lower power supply voltages, in some cases less than 1 V. These high-frequency circuits often require a considerable amount of supply current, so thermal management can become difficult. A design goal is to reduce power dissipation to that which is absolutely necessary for circuit performance.

Switch-mode dc-to-dc converters make the most efficient power supplies, with some devices exceeding 95% efficiency, but this high efficiency comes at the cost of increased power-supply noise, often over a wide bandwidth. Low-dropout linear regulators (LDOs) are frequently used to clean up noisy supply rails, but they also present trade-offs, dissipating power and increasing the system's thermal load. To minimize these problems, LDOs can be operated with a smaller difference (headroom voltage) between input and output voltages. This article discusses the impact of low-headroom voltage operation on power-supply rejection and total output noise.

LDO Power-Supply Rejection vs. Headroom

LDO power-supply rejection ratio (PSRR) is strongly dependent on headroom voltage—the difference between the input and output voltages. For a fixed headroom voltage, PSRR decreases as the load current increases; this is especially true with large load currents and small headroom voltages. Figure 1 shows the PSRR for the ADM7160 ultralow-noise, 2.5-V linear regulator with 200-mA load current and 200-mV, 300-mV, 500-mV and 1-V headroom voltages. As the headroom voltage decreases, the PSRR decreases, and the difference can be dramatic. For example, at 100 kHz, changing the headroom voltage from 1 V to 500 mV results in a 5-dB decrease in PSRR. However, a smaller change in headroom voltage, from 500 mV to 300 mV, causes the PSRR to drop more than 18 dB.

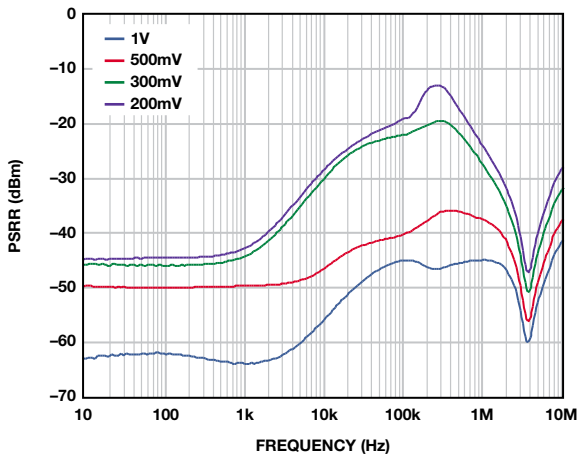
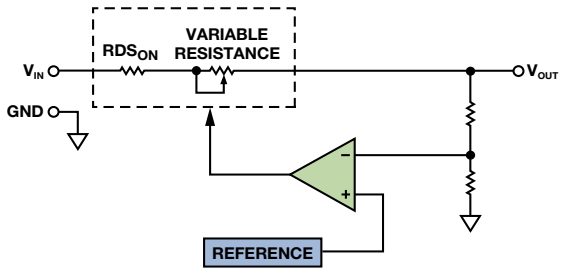


Figure 1. *ADM7160 PSRR vs. headroom.*

Figure 2 shows a block diagram of the LDO. As the load current increases, the gain of the PMOS pass element decreases as it leaves saturation and enters the triode region. This causes the overall loop gain to decrease, resulting in lower PSRR. The smaller the headroom voltage, the more dramatic the reduction in gain. As the headroom voltage continues to decrease, it reaches a point at which the gain of the control loop drops to 1, and the PSRR falls to 0 dB.

Another factor that reduces the loop gain is the resistance of the pass element, which includes the FET's on resistance, the on-chip interconnect resistance, and the wire bonds. An estimate of this resistance can be derived from the dropout voltage. For example, the ADM7160 in the WLCSP package has a maximum dropout voltage of 200 mV at 200 mA. Using Ohm's law, the resistance of the pass element is about 1 Ω. The pass element can be approximated as a fixed resistor plus a variable resistance.

Voltage drops due to the load current flowing through this resistance subtract from the drain-to-source operating voltage of the FET. For example, with a 1-Ω FET, a load current of 200 mA reduces the drain-to-source voltage by 200 mV. When estimating the PSRR of LDOs operating with 500-mV or 1-V headroom, the voltage drop across the pass element must be taken into account, as the pass FET is effectively operating with only 300 mV or 800 mV.



NOTES
1. ERROR AMP CONTROLS VALUE OF VARIABLE RESISTOR TO REGULATE OUTPUT VOLTAGE.
2. AT LOW HEADROOM VOLTAGE, THE VARIABLE RESISTOR IS NEARLY 0Ω.

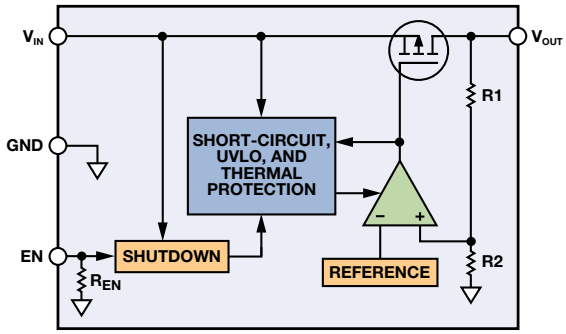


Figure 2. *Block diagram of a low-dropout regulator.*

Effect of Tolerances on LDO Headroom

Customers often ask applications engineers to help them select an LDO to generate low-noise voltage X from input voltage Y at load current Z, but one factor frequently ignored when setting these parameters is the tolerance of the input and output voltages. As headroom voltage falls to lower and lower values, the tolerance of the input and output voltages can dramatically affect the operating conditions. The worst-case tolerance of the input and output voltages always results in a lower headroom voltage. For example, the worst-case output voltage can be 1.5% high and the input voltage can be 3% low. When a 3.3-V regulator is powered by a 3.8-V source, the worst-case headroom voltage is 336.5 mV, far lower than the expected 500 mV. With the worst-case load current of 200 mA, the drain-to-source voltage of the pass FET is only 136.5 mV. The PSRR of the ADM7160 in this case can be expected to fall far short of the published 55 dB at 10 mA.

PSRR of an LDO Operating in Dropout

Customers frequently ask applications engineers about an LDO's PSRR in dropout. Initially this may seem like a reasonable question, but a glance at the simplified block diagram will show it to be meaningless. When the LDO is in dropout, the variable resistance portion of the pass FET is zero, and the output voltage is equal to the input voltage minus the voltage drop due to the load current through the RDS_{ON} of the pass FET. The LDO is not regulating and has no gain to reject noise on the input; it is simply operating as a resistor. The RDS_{ON} of the FET forms an RC filter with the output capacitor, providing a small amount of residual PSRR, but a simple resistor or ferrite bead could perform the same job much more cost effectively.

Maintaining Performance when Operating with Low Headroom

It is imperative to consider the effect of headroom voltage on PSRR when operating at low headroom, as failure to do so will result in a noisier output voltage than expected. PSRR vs. headroom voltage plots, such as that shown in Figure 3, are usually found in the data sheet and can be used to determine the amount of noise rejection possible for a given set of conditions.

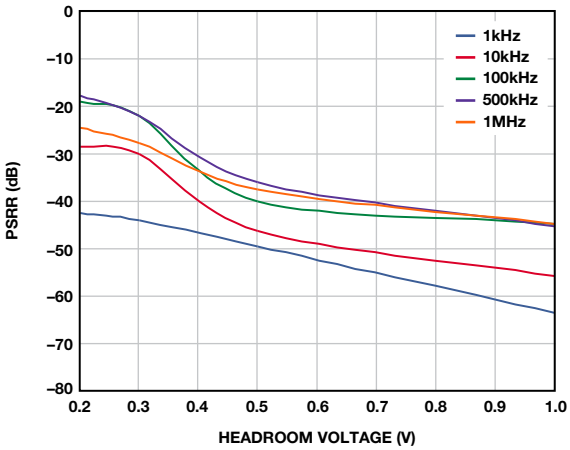


***Figure 3.** PSRR vs. headroom voltage.*

However, it's sometimes easier to see how to apply this information by demonstrating how the LDO's PSRR effectively filters out the noise of the source voltage. The following plots show the impact on the total output noise of an LDO when operating at different headroom voltages.

Figure 4 shows the output noise of a 2.5-V ADM7160 with 500-mV headroom and 100-mA load compared to the baseline noise of an E3631A bench supply, which specifies less than 350-μV-rms noise from 20 Hz to 20 MHz. The many spurs below 1 kHz are harmonics related to rectification of the 60-Hz line frequency. The broad spur above 10 kHz is from the dc-to-dc converter that generates the final output voltage. The spurs above 1 MHz are due to RF sources in the environment unrelated to the power-supply noise. The measured noise of the supply used for these tests is 56 μV rms from 10 Hz to 100 kHz and 104 μV rms including the spurs. The LDO rejects all of the noise on the power supply, and has about 9-μV-rms output noise.

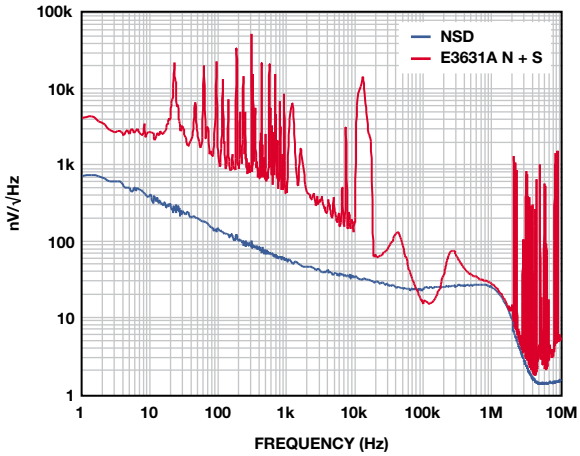


***Figure 4.** ADM7160 noise spectral density with 500 mV headroom.*

As the headroom voltage drops to 200 mV, the noise spurs above 100 kHz begin to poke though the noise floor as the high-frequency PSRR approaches 0 dB. The noise rises slightly to 10.8 μV rms. As the headroom falls to 150 mV, rectification harmonics start to affect the output noise, which rises to 12 μV rms. A moderate peak appears at about 250 kHz, so sensitive circuitry may be adversely affected even though the increase in total noise is modest. As the headroom voltage drops further, performance becomes compromised, and spurs related to rectification become visible in the noise spectrum. Figure 5 shows the output with 100-mV headroom. The noise has risen to 12.5 μV rms. The harmonics contain very little energy, so the noise with spurs is only slightly higher at 12.7 μV rms.

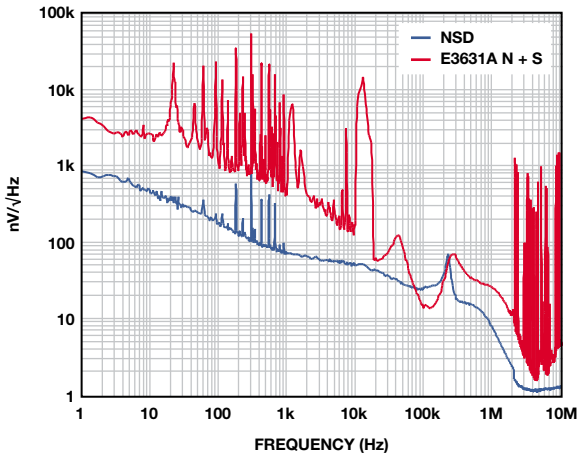


***Figure 5.** ADM7160 noise spectral density with 100 mV headroom.*

With 75-mV headroom, the output noise becomes severely compromised, and rectification harmonics appear throughout the spectrum. The rms noise rises to 18 µV rms and the noise plus spurs rises to 27 µV rms. The noise beyond ~200 kHz is attenuated because the LDO loop has no gain and acts as a passive RC filter. With 65-mV headroom, the ADM7160 is operating in dropout. As shown in Figure 6, the output voltage noise of the ADM7160 is essentially the same as the input noise. The rms noise is now 53 µV rms and the noise plus spurs is 109 µV rms. The noise beyond ~100 kHz is attenuated because the LDO is acting as a passive RC filter.

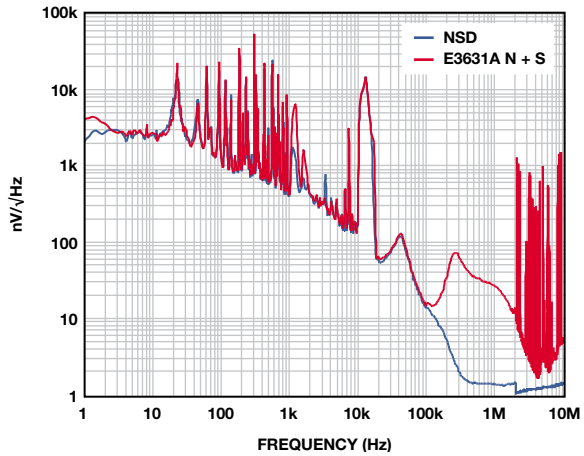


Figure 6. ADM7160 noise spectral density in dropout.

Ultralow-Noise LDOs with High PSRR

A new class of LDOs such as the ADM7150 ultralow-noise, high-PSRR regulator essentially cascade two LDOs, so the resulting PSRR is approximately the sum of that of the individual stages. These LDOs require somewhat higher headroom voltages but are able to achieve PSRRs exceeding 60 dB at 1 MHz and well over 100 dB at lower frequencies.

Figure 7 shows the noise spectral density of a 5-V ADM7150 with 500-mA load current and 800-mV headroom. The output noise is 2.2 µV rms from 10 Hz to100 kHz. As the headroom drops to 600 mV, the rectification harmonics start to become apparent, but the effect on the noise is small as the output noise rises to 2.3 µV rms.

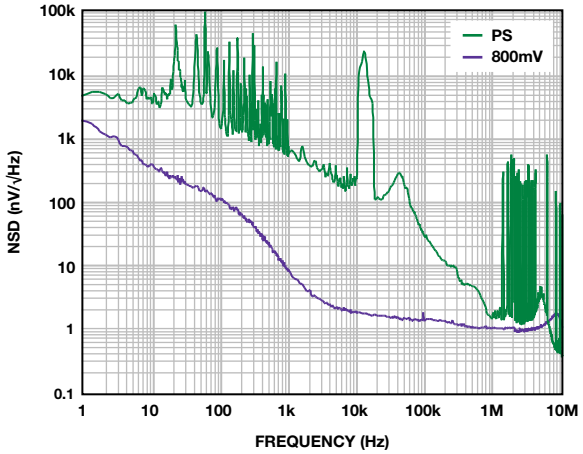


Figure 7. ADM7150 noise spectral density with 800-mV headroom.

With 500-mV headroom, rectification harmonics and a peak at 12 kHz are clearly visible, as shown in Figure 8. The output voltage noise rises to 3.9 µV rms.

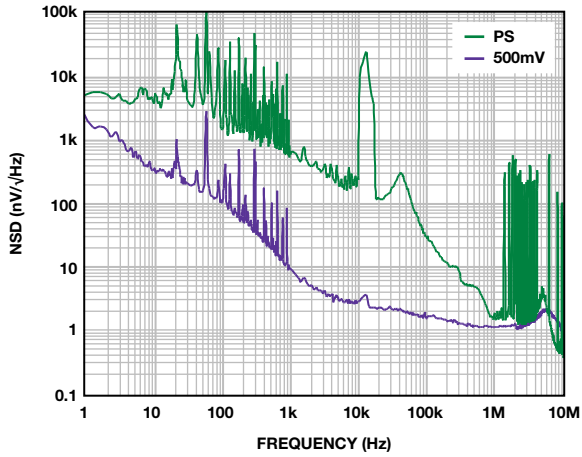


Figure 8. ADM7150 noise spectral density with 500-mV headroom.

With 350-mV headroom, the LDO is in dropout. No longer able to regulate the output voltage, the LDO acts like a resistor, and the output noise has risen to nearly 76 µV rms, as shown in Figure 9. The input noise is only attenuated by the pole formed by the RDS_{ON} of the FET and the capacitance at the output.

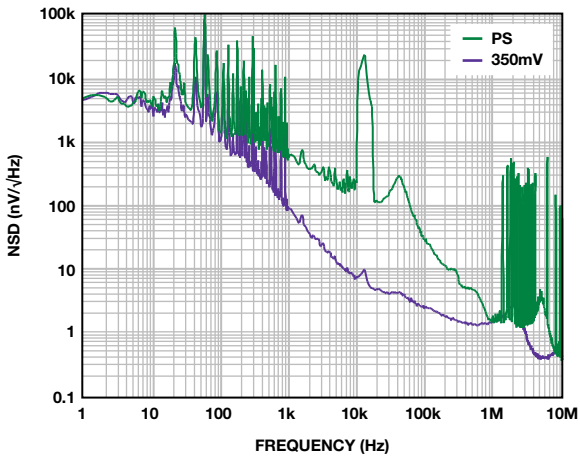


Figure 9. ADM7150 noise spectral density in dropout.

Conclusion

Modern LDOs are increasingly being used to clean up dirty power supply rails, which are often implemented with switching regulators that generate noise over a broad spectrum. The switching regulators create these voltage rails at high efficiency, but the dissipative LDOs reduce both noise and efficiency. Therefore, LDOs should be operated with as little headroom voltage as possible.

As shown, their PSRR is a function of both load current and headroom voltage, decreasing as the load current increases or the headroom voltage decreases due to the reduced loop gain as the operating point of the pass transistor moves from the saturation region to the triode region.

Considering the input source noise characteristics, PSRR, and worst-case tolerances allows designers to optimize both the power dissipation and output noise to achieve an efficient, low-noise power supply for sensitive analog circuits.

When operating at very low headroom voltages, the worst-case tolerance of the input and output voltages can affect the PSRR. Designing for worst-case tolerances will ensure a robust design; failure to do so will yield a power solution with lower PSRR resulting in higher than expected total noise.

References

Linear Regulators

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Minimum Load Current Operation—Zero-Load Operation

By Luca Vassalli

As an applications engineer, I am frequently asked about operating regulators with no load. Most modern LDOs and switching regulators are stable with no load, so why do people repeatedly ask? Some older power devices require a minimum load to guarantee stability, as one of the poles that must be compensated is affected by the effective load resistance, as discussed in "Low-Dropout Regulators (Ask the Applications Engineer—37)." For example, Figure A shows that the LM1117 requires a 1.7-mA minimum load current (up to 5 mA).

LM1117-N ELECTRICAL CHARACTERISTICS (continued)

Typicals and limits appearing in normal type apply for T_J = 25°C. Limits appearing in **Boldface** type apply over the entire junction temperature range for operation, 0°C to 125°C.

Symbol	Parameter	Conditions	Min(1)	Typ(2)	Max(1)	Units
I_{LIMIT}	Current Limit	$V_{IN} - V_{OUT}$ = 5V, T_J = 25°C	800	1200	1500	mA
	Minimum Load Current(5)	LM1117-N-ADJ V_{IN} = 15V		1.7	**5**	mA

***Figure A.** LM1117 minimum load current specifications.*

Most newer devices are designed to operate with no load, and exceptions to this rule are very limited. The same design techniques that allow LDOs to be stable with any output capacitor, especially low ESR caps, are used to guarantee stability at no load. For those few modern devices that require a load, the limitation is usually a result of leakage current through the pass element, not the stability. So, how can you tell? Read the data sheet. If the device requires a minimum load, the data sheet would surely say something.

The ADP1740 and other low-voltage, high-current LDOs fall into this category. The worst-case leakage current from the integrated power switch is about 100 µA at 85°C and 500 µA at 125°C. Without a load, the leakage current would charge the output capacitor until the switch VDS was low enough to reduce the leakage current to a negligible level, raising the no-load output voltage. The data sheet says that a 500 µA minimum load is required, so a dummy load is advisable if the device will operate at high temperature. This load is small compared to the device's 2-A rating. Figure B shows the minimum load current specification from the ADP1740 data sheet.

ADP1740/ADP1741 Data Sheet

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
SENSE INPUT BIAS CURRENT (ADP1740)	SNS_{I-BIAS}	1.6 V ≤ V_{IN} ≤ 3.6 V		10		µA
OUTPUT NOISE	OUT_{NOISE}	10 Hz to 100 kHz, V_{OUT} = 0.75 V		23		µV rms
		10 Hz to 100 kHz, V_{OUT} = 2.5 V		65		µV rms
POWER SUPPLY REJECTION RATIO	PSRR	V_{IN} = V_{OUT} + 1 V, I_{OUT} = 10 mA				
		1 kHz, V_{OUT} = 0.75 V		65		dB
		1 kHz, V_{OUT} = 2.5 V		56		dB
		10 kHz, V_{OUT} = 0.75 V		65		dB
		10 kHz, V_{OUT} = 2.5 V		56		dB
		100 kHz, V_{OUT} = 0.75 V		54		dB
		100 kHz, V_{OUT} = 2.5 V		51		dB

[1] Minimum output load current is 500 µA.
[2] Accuracy when V_{OUT} is connected directly to ADJ. When V_{OUT} voltage is set by external feedback resistors, absolute accuracy in adjust mode depends on the tolerances of the resistors used.
[3] Based on an endpoint calculation using 10-mA and 2-A loads. See Figure 6 for typical load regulation performance.
[4] Dropout voltage is defined as the input to output voltage differential when the input voltage is set to the nominal output voltage. This applies only to output voltages above 1.6 V.
[5] Start-up time is defined as the time between the rising edge of EN to V_{OUT} being at 95% of its nominal value.
[6] Current-limit threshold is defined as the current at which the output voltage drops to 90% of the specified typical value. For example, the current limit for a 1.0-V output voltage is defined as the current that causes the output voltage to drop to 90% of 1.0 V, or 0.9 V.

***Figure B.** ADP1740 minimum load current specification.*

What if the data sheet doesn't explicitly specify a minimum load? In most cases, a minimum load is not required. It may not sound very convincing, but if a minimum load was required, the data sheet would certainly say so. The confusion often comes into play because data sheets will often include graphs showing the specifications over some operating range. Most of these graphs are logarithmic, allowing them to show multiple decades of load ranges, but a log scale cannot go to zero. Figure C shows the ADM7160 output voltage and ground current vs. load current over the 10-µA to 200-mA range. Other graphs, such as ground current vs. input voltage, show measurements at multiple load currents, but don't show data at zero current. In addition, parameters such as PSRR, line regulation, load regulation, and noise specify a certain load current range that does not include zero, as shown in Figure D. None of this means that a minimum load is required, though.

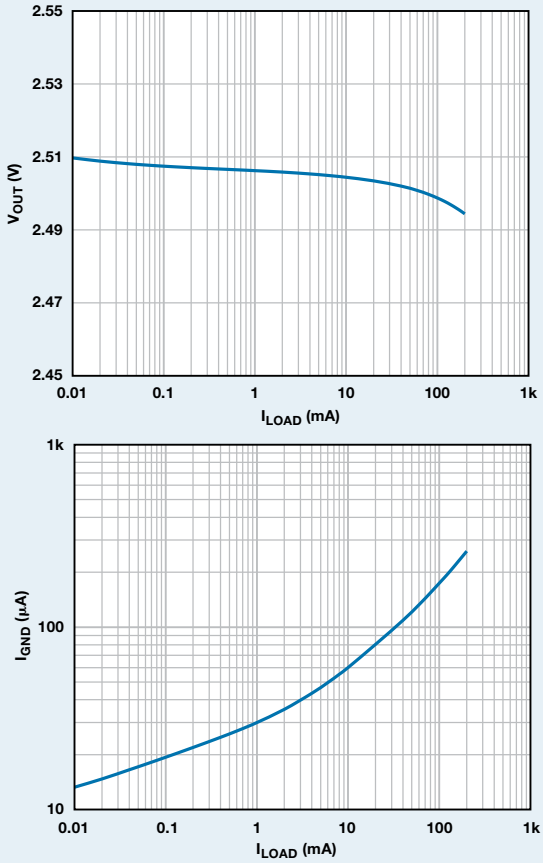

***Figure C.** ADM7160 output voltage and ground current vs. load current.*

LOAD REGULATION	$\Delta V_{OUT}/\Delta I_{LOAD}$				
V_{OUT} < 1.8 V		I_{LOAD} = 100 µA to 200 mA	0.006		%/mA
		I_{LOAD} = 100 µA to 200 mA, T_J = −40°C to +125°C		0.012	%/mA
V_{OUT} ≥ 1.8 V		I_{LOAD} = 100 µA to 200 mA	0.003		%/mA
		I_{LOAD} = 100 µA to 200 mA, T_J = −40°C to +125°C		0.008	%/mA

***Figure D.** ADM7160 load regulation.*

Users of switching regulators with power-saving mode (PSM) are often worried about operation at light loads because PSM reduces the operating frequency, skips pulses, provides a burst of pulses, or some combination of these. PSM reduces power consumption and increases efficiency at light loads. Its disadvantage is a noticeable increase in output ripple, but the device remains stable and can easily operate with no load.

As shown in Figure E, the ADP2370 high-voltage, low-quiescent-current buck regulator produces increased ripple due to PSM operation when the load switches between 800 mA and 1 mA. The fact that the test was done at 1 mA does not indicate that 1 mA is the minimum load.

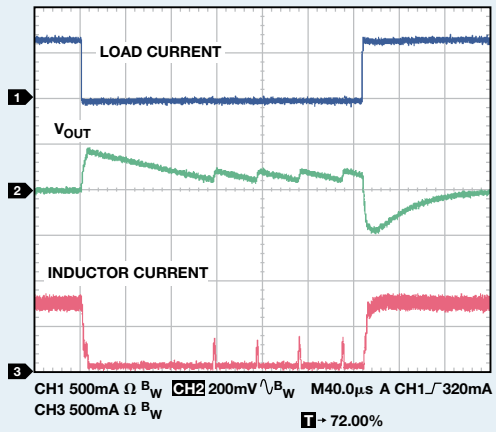

***Figure E.** ADP2370 load transient in power-saving mode.*

Figure F shows the ripple voltage changing with load current. In this case the graph goes all the way to zero, indicating both that the load can be zero and that the noise at no load may not be any worse than the noise at 1 mA or 10 mA.

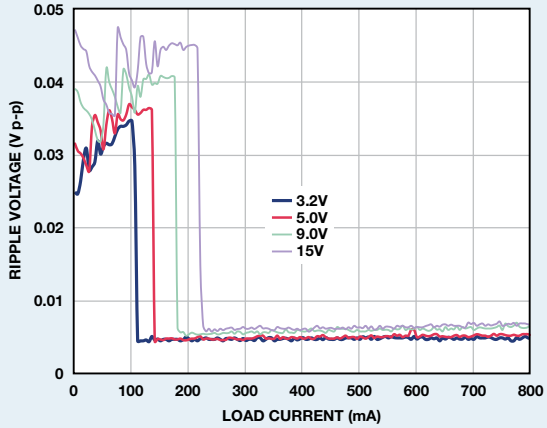

***Figure F.** ADP2370 output ripple vs. load current.*

Conclusion

Most modern regulators are stable with zero load current, but when in doubt, consult the data sheet. Be careful, though. Logarithmic graphs don't go to zero, and tests aren't always done with zero load current, so you shouldn't infer that the regulator won't work with no load even though no-load data isn't shown. With switching regulators, ripple in power-saving mode is normal, not a sign of instability.

References

Caveat Emptor

Linear Regulators

Switching Regulators

Patoux, Jerome. "Low-Dropout Regulators (Ask the Applications Engineer—37)," *Analog Dialogue*, Volume 41, Number 2, 2007.

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Glenn Morita [glenn.morita@analog.com] graduated from Washington State University with a BSEE in 1976. His first job out of school was at Texas Instruments, where he worked on the infrared spectrometer instrument for the Voyager space probe. Since then, Glenn has worked as a designer in the instrumentation, military and aerospace, and medical industries. In 2007, he joined ADI as an applications engineer with the Power Management Products Team in Bellevue, WA. He has over 25 years of linear and switch-mode power supply design experience at power levels ranging from microwatts to kilowatts. Glenn holds two patents for harvesting energy from body heat to power implantable cardio-defibrillators and an additional patent for extending battery life in external cardio-defibrillators. In his spare time, he enjoys collecting minerals, faceting gemstones, photography, and visiting the national parks.

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Also by this Author:

Noise-Reduction Network for Adjustable-Output Low-Dropout Regulators

Volume 48, Number 1

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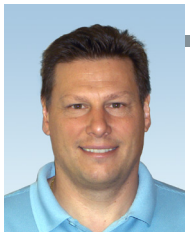

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