

Next-Generation SAR ADC Addresses Pain Points of Precision Data Acquisition Signal Chain Design

By **Maithil Pachchigar** and **Alan Walsh**

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Introduction

Many applications require a precision data acquisition signal chain in order to digitize analog data so that it can be collected and processed accurately. Precision system designers are continually pressed to find innovative ways to improve performance and reduce power dissipation while accommodating increased circuit density in a small PCB footprint. This article discusses the common pain points encountered in designing a precision data acquisition signal chain and how to address them using the next generation of 16-/18-bit, 2 MSPS, precision successive approximation register (SAR) ADCs. Designed using ADI's advanced technology, the [AD4000/AD4003](#) (16-/18-bit) ADC incorporates ease of use features that offer a multitude of system-level benefits that help to lower the signal chain power, reduce signal chain complexity, and enable higher channel density while pushing the performance level higher. This article will highlight data acquisition subsystem performance and design challenges and explain how this ADC family creates application level impact in multiple end markets.

Common Signal Chain Design Pain Points

Figure 1 shows a typical signal chain used in building precision data acquisition systems. Applications that require precision data acquisition systems such as automated test equipment, machine automation, industrial, and medical instrumentation have common trends that are typically considered technically conflicting. For example, system designers are forced to make performance trade-offs to keep a tight system power budget or small area on the board to achieve high channel density. System designers of these precision data acquisition signal chains face common challenges in terms of driving the SAR ADC inputs, protecting ADC inputs from overvoltage events, reducing the system power with single supplies, and achieving higher system throughput with low power microcontrollers and/or digital isolators.

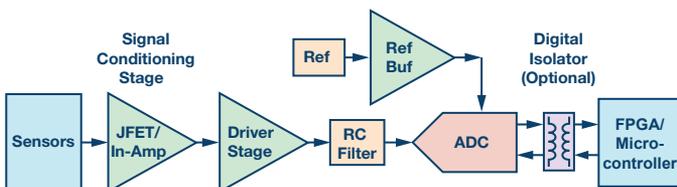


Figure 1. Typical precision data acquisition signal chain.

Driving high resolution precision SAR ADCs has been traditionally a tricky issue because of the switched capacitor inputs. System designers need to pay close attention to the ADC driver data sheet and look at the noise, distortion, input/output voltage headroom/footroom, bandwidth, and settling time specifications. Typically, high speed ADC drivers are required that are wide bandwidth, low noise, and high power in order to settle the switched capacitor kickback of the SAR ADC inputs within the available acquisition time. This significantly reduces the options available for amplifiers to drive the ADC and results in significant performance/power/area trade-

offs. Furthermore, selecting an appropriate RC filter to place between the driver and the ADC inputs imposes further constraints on amplifier choice and performance. The RC filter between ADC driver output and SAR ADC input is required to limit wideband noise and reduce the effects of charge kickback. Typically, the system designer needs to spend significant time to evaluate the signal chain to ensure that the selected ADC driver and RC filter can drive the ADC to achieve a desired performance.

In power sensitive applications like battery-powered instrumentation, it is often desirable to run the system from a single low voltage supply. This minimizes the power dissipation of the circuitry but introduces issues with headroom and footroom for the amplifier front end. This means it may not be possible to use the full ADC input range because the driving amplifier cannot drive all the way to ground or all the way to the upper end of the ADC input range, reducing the performance of the overall system. This can be remedied by increasing the supply voltage at the cost of higher power dissipation or accepting the lower dynamic range performance from the system.

Most ADC analog inputs, IN+ and IN-, have no overvoltage protection circuitry apart from ESD protection diodes. In applications where the amplifier rails are greater than V_{REF} and less than ground, it is possible for the output to go outside the input voltage range of the device. During an overvoltage event, the ESD protection diode between either analog input (IN+ or IN-) pin to REF forward biases and shorts the input pin to REF, potentially overloading the reference, causing damage to the device, or disturbing a reference that is shared among multiple ADCs. This results in having to add protection circuitry like Schottky diodes to the ADC input to prevent overvoltage conditions from harming the ADC. Unfortunately, Schottky diodes could add distortion and other errors due to leakage currents.

Precision applications have different needs in terms of the processors that interface to the ADC. Some applications need to be electrically isolated for safety reasons and use digital isolators between the ADC and processor to achieve this. This choice of processor or need for isolation puts constraints on the efficiency of the digital interface used to connect with the ADC. Typically, lower end processors/FPGAs or lower power microcontrollers have relatively low serial clock rates. This can result in lower than desired throughput from the ADC because of a long ADC conversion time delay before the conversion result can be clocked out. Digital isolators can also limit the maximum serial clock rate that can be achieved across the isolation barrier due to propagation delays in the isolator limiting the ADC throughput. In these scenarios an ADC that can achieve a higher throughput rate without a significant increase in serial clock rate is desirable.

AD4000/AD4003 Precision SAR ADC Family Solves Common Design Challenges

The AD4000/AD4003 family is a fast, low power, single-supply, 16-/18-bit precision ADC based on a SAR architecture.

The AD4000/AD4003 precision ADC family uniquely combines high performance with ease of use features that reduces system complexity, simplifies signal chain BOM, and significantly decreases time to market (see Figure 2). This family enables designers to solve the system-level technical challenges for their high precision data acquisition system without making significant trade-offs. For example, a combination of a long acquisition phase, high input impedance (Z) mode, and span compression mode of the AD4000/AD4003 ADC family reduces the design challenges associated with the ADC driver stage and increases the flexibility in ADC driver selection. This enables overall lower system power, higher density, and reduced customer design cycle time. Most of the ease of use features can be enabled/disabled through writing to the configuration register via an SPI interface. Note that AD4000/AD4003 ADC family is pin-compatible with the 10-lead AD798x/AD769x ADC family.

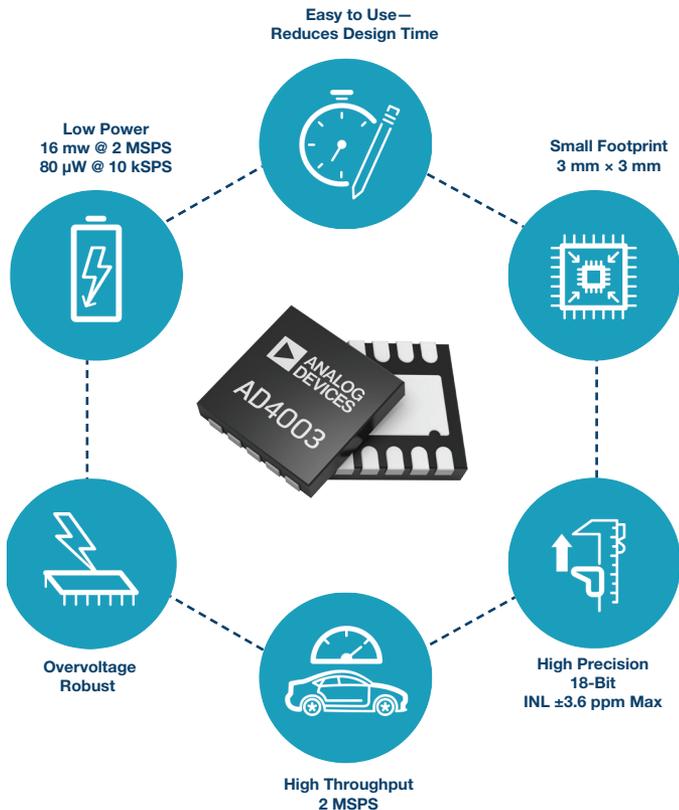


Figure 2. AD4000/AD4003 ADC key benefits.

AD4000/AD4003 ADC Ease of Use Features

Long Acquisition Phase

The AD4000/AD4003 ADC features a very fast conversion time of 290 ns and the ADC returns back to the acquisition phase 100 ns before the end of the ongoing conversion process. SAR ADC cycle time is comprised of conversion and acquisition phases. During the conversion phase, the ADC capacitor DAC is disconnected from the ADC inputs to perform the SAR conversion. The inputs are reconnected during the acquisition phase, and the ADC driver must settle the inputs to the correct voltage before the next conversion phase begins. A longer acquisition phase reduces the settling requirement on the driving amplifier and allows a lower RC filter frequency cutoff, which means a higher noise and/or lower power/bandwidth amplifier can be tolerated. A larger value of R can be used in the RC filter with a corresponding smaller value of C, reducing amplifier stability concerns without impacting distortion performance significantly. A larger value of R helps to protect the ADC inputs from overvoltage conditions. It also results in reduced dynamic power dissipation in the amplifier.

High Input Impedance Mode

To achieve the optimum data sheet performance from high resolution precision SAR ADCs, system designers are often forced to use a dedicated high power, high speed amplifier to drive the traditional switched capacitor SAR ADC inputs for their precision applications. This is one of the common pain points encountered in designing a precision data acquisition signal chain. The benefits of high-Z mode are low input current for slow (<10 kHz) or dc type signals and improved distortion (THD) performance over an input frequency range up to 100 kHz.

The AD4000/AD4003 ADC incorporates a high-Z mode that reduces the nonlinear charge kickback when the capacitor DAC switches back to the input at the start of acquisition. With high-Z mode enabled, the capacitor DAC is charged at the end of conversion to hold the previously sampled voltage. This process reduces any nonlinear charge effects from the conversion process affecting the voltage that is acquired at the ADC input prior to the next sample.

Figure 3 shows the input current of the AD4000/AD4003 ADC with high-Z mode enabled/disabled. The low input current makes the ADC a lot easier to drive than traditional SAR ADCs available in the market even with high-Z mode disabled. If you compare the input current in Figure 3 with high-Z mode disabled against that of the previous generation AD7982 ADC, the AD4003 has reduced the input current by 4× at 1 MSPS. The input current reduces further to submicroampere range when high-Z mode is enabled. High-Z mode should be disabled for input frequencies above 100 kHz or when multiplexing on the input.

With the reduced input current of the AD4000/AD4003 ADC, it is capable of being driven with a much higher source impedance than traditional SARs. This means the resistor in the RC filter can have 10× larger value than traditional SAR designs.

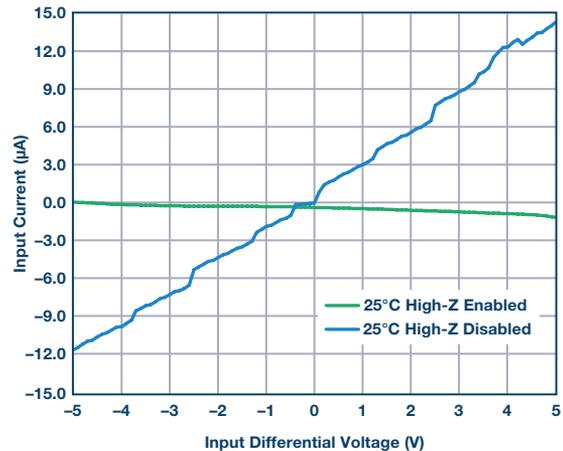


Figure 3. AD4003 ADC input current vs. input differential voltage with high-Z enabled/disabled.

As shown in Figure 4, the AD4000/AD4003 ADC allows a choice of lower power/bandwidth precision amplifiers with a lower RC filter cutoff to drive the ADC, removing the need for dedicated high speed ADC drivers, saving system power, size, and cost in precision, low bandwidth applications (signal bandwidths <10 kHz). Ultimately, the AD4000/AD4003 allows the amplifier and RC filter in front of the ADC to be chosen based on the signal bandwidth of interest and not based on the settling requirements of the switched capacitor SAR ADC inputs.

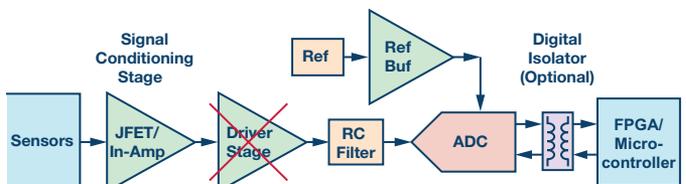


Figure 4. Traditional precision signal chain.

Figure 5 and Figure 6 show the AD4003 ADC's SNR and THD performance using the ADA4077 ($I_{\text{QUIESCENT}} = 400 \mu\text{A}/\text{amplifier}$), ADA4084 ($I_{\text{QUIESCENT}} = 600 \mu\text{A}/\text{amplifier}$), and ADA4610 ($I_{\text{QUIESCENT}} = 1.5 \text{ mA}/\text{amplifier}$) precision amplifiers when driving the AD4003 ADC at full throughput of 2 MSPS for both the high-Z enabled/disabled cases with various RC filter values. These amplifiers achieve 96 dB to 99 dB typical SNR and better than -110 dB typical THD with high-Z enabled for a 2.27 MHz RC bandwidth and 1 kHz input signal. THD is approximately 10 dB better with high-Z mode enabled even for large R values greater than 200Ω . SNR holds up close to 99 dB even with a very low RC filter cutoff.

With high-Z enabled, the ADC will consume around 2 mW/MSPS extra power, but this would be still significantly lower than using dedicated ADC drivers like the ADA4807-1 and results in PCB area and bill of material savings. For most systems, the front end usually limits the overall ac/dc performance achievable by the signal chain. It's evident from the selected precision amplifier's data sheet in Figure 5 and Figure 6 that its own noise and distortion performance dominates the SNR and THD specification at a certain input frequency. However, the AD4003 ADC with high-Z mode allows a greatly expanded choice of driver amplifier including precision amplifiers used in signal conditioning stages along with more flexibility in the RC filter choice. For example, when the AD4003 ADC's high-Z is enabled and using the ADA4084-2 driver amplifier with a wideband input filter of 4.42 MHz, the SNR performance is about 95 dB. With more aggressive filtering of the ADC driver's noise using a 498 kHz filter, SNR improves by 3 dB, to 98 dB. The AD7982 ADC's SNR performance at lower RC cutoff is degraded because the ADC input does not settle the kickback within its short acquisition time.

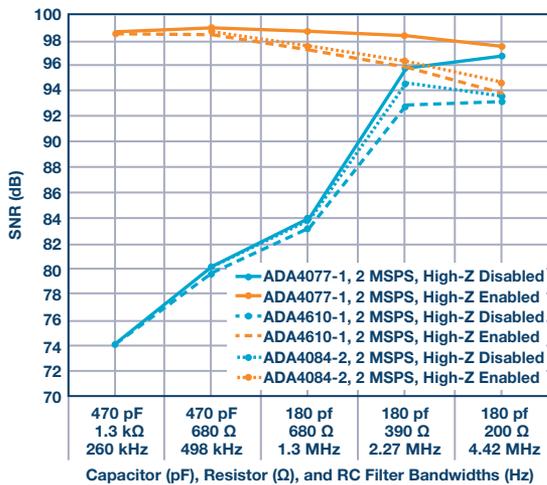


Figure 5. SNR vs. RC bandwidths using ADA4077, ADA4084, and ADA4610 precision amplifiers.

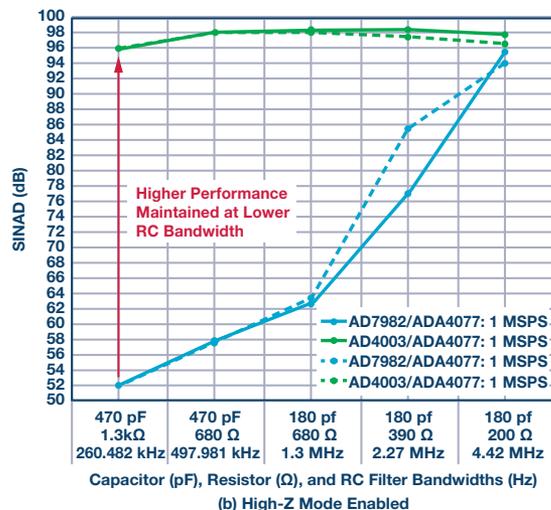
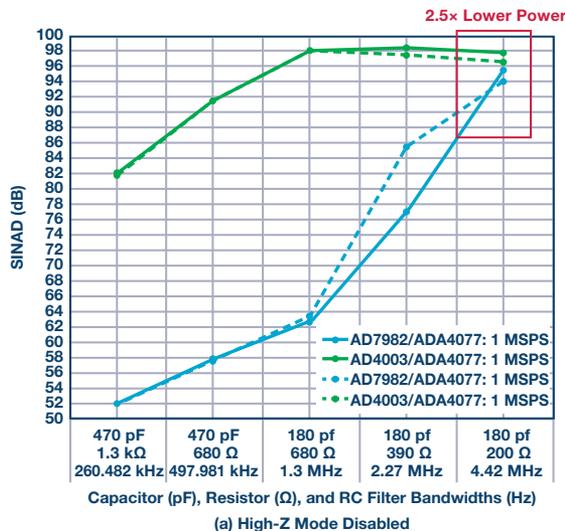


Figure 7. AD4003 ADC and AD7982 ADC amplifier driver comparison using ADA4077 and ADA4807: SINAD vs. RC bandwidths for high-Z mode disabled and enabled ($F_s = 1 \text{ MSPS}$, $f_{\text{IN}} = 1 \text{ kHz}$).

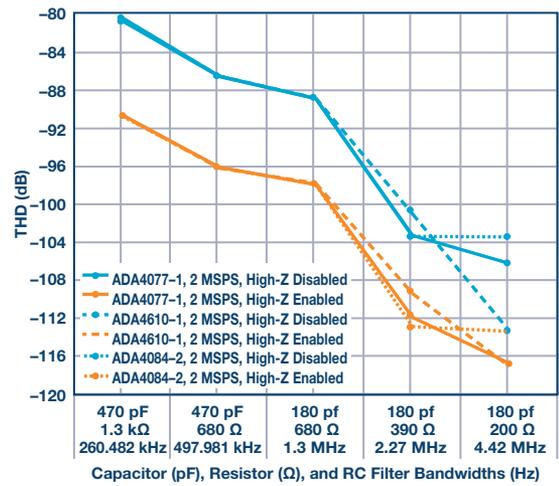


Figure 6. THD vs. RC bandwidths using ADA4077, ADA4084, and ADA4610 precision amplifiers.

Figure 7(a) shows that system designers can use the 2.5 \times lower power ADC driver ADA4077 (vs. the ADA4807), and the AD4003 ADC still achieves SINAD of about 97 dB (3 dB better than the AD7982 ADC) when high-Z mode is disabled. Even with a wider RC bandwidth of 2.9 MHz, the ADA4077 amplifier cannot drive the AD7982 ADC directly and achieve optimum performance. The driver cannot settle the ADC kickback within the available acquisition time with aggressive filtering at a lower RC bandwidth cutoff and hence the ADC SINAD performance is degraded. The AD4003 ADC's switched capacitor kickback with either high-Z mode disabled or enabled is much reduced and the acquisition time is 2.5 \times longer at 1 MSPS and hence its SINAD performance is still significantly better than that of AD7982 ADC.

With high-Z mode enabled, the AD4003 ADC's SINAD performance is better using both ADC drivers at lower RC filter cutoff, which helps remove more wideband noise coming from the upstream signal chain components when the signal bandwidth of interest is low. Without high-Z mode enabled there is a trade-off between RC filter cutoff and SINAD performance.

Span Compression

The AD4000/AD4003 ADC includes a span compression mode, which is useful for systems that only have a single positive supply to power the SAR ADC drivers. It eliminates the ADC driver's need for a negative supply while preserving the full resolution of the ADC, saving power and reducing power supply design complexity. As shown in Figure 8, the ADC performs a digital scaling function that maps zero-scale code from 0 V to $0.1 \text{ V} \times$

V_{REF} and full-scale code from V_{REF} to $0.9 \times V_{REF}$. The AD4000/AD4003 ADC's SNR takes a hit of about ~ 1.9 dB ($20 \times \log(4/5)$) for the reduced input range. As an example, for a subsystem operating from a single 5 V supply and a typical reference voltage of 4.096 V, the full-scale input range is now ~ 0.41 V to 3.69 V, which provides adequate headroom for powering the driving amplifier.

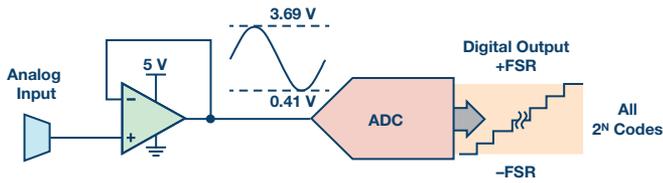


Figure 8. AD4000/AD4003 ADC span compression operation.

Overvoltage Clamp

In applications where the amplifier rails are greater than V_{REF} and less than ground it is possible for the output to violate the input voltage range of the part. When positive input is over-ranged, current flows through D1 into REF (see Figure 9), disturbing the reference. Even worse it could pull the reference above the absolute maximum reference value and hence could damage the part.

When the analog input exceeds the reference voltage by ~ 400 mV, the AD4000/AD4003 ADC's internal clamp circuit will turn on and the current will flow through the clamp into ground, preventing the input from rising further and potentially causing damage to the device.

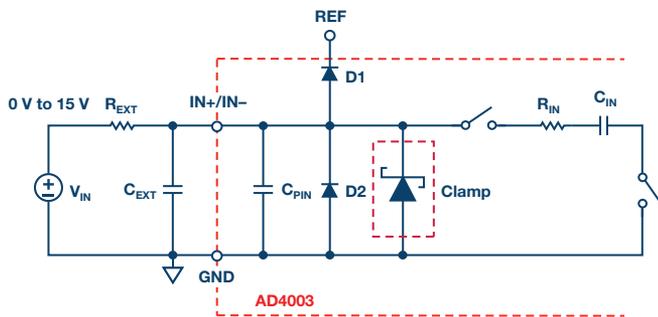


Figure 9. AD4003 ADC equivalent analog input circuit.

As shown in Figure 9, the AD4000/AD4003 ADC's internal overvoltage clamp circuit with a larger external resistor ($R_{EXT} = 200 \Omega$) eliminates the need for external protection diodes (and hence the need for additional board space). The clamp turns on before D1 and can sink up to 50 mA of current. The clamp prevents damage to the device by clamping the input voltage to a safe operating range and avoids disturbance of the reference, which is particularly important for systems that share the reference among multiple ADCs.

Efficient Digital Interface

The AD4000/AD4003 ADC has a flexible digital serial interface that offers seven different modes with register programmability. Its turbo mode allows the user to start clocking out the previous conversion results while the ADC is still converting, as shown in Figure 10. A combination of short conversion time and turbo mode allows a lower SPI clock rate and simplifies the isolation solution, resulting in reduced latency requirements on digital isolators and broadening a choice of processors including lower end processors/FPGAs or low power microcontrollers with relatively low serial clock rates. For example, the AD4003 ADC can use a $2.5 \times$ slower SPI clock rate (25 MHz vs. 66 MHz) than the AD7982 ADC when running at 1 MSPS. The user can write/read back the register bits to enable the AD4000/AD4003 ADC's ease

of use features and a 6-bit status word can be appended to the conversion result that allows diagnosis along with register read back. The serial interface is completely specified down to 1.8 V logic levels and can achieve the full 2 MSPS throughput under these conditions. A minimum SCK rate of 75 MHz is required to run the AD4003 ADC at 2 MSPS with turbo mode enabled.

AD4000/AD4003 ADC Performance

Operating from a 1.8 V supply, the AD4000/AD4003 ADC consumes typically 14 mW/16 mW at 2 MSPS and offers superior linearity of ± 1.0 LSB (± 3.8 ppm) max and guaranteed 18 bits no missing codes. Figure 11 shows the AD4003 ADC's typical INL vs. code performance. The AD4003 ADC achieves better SINAD performance than the AD7982 ADC over a wide range of input frequencies up to Nyquist (Figure 12), enabling system designers to develop wider bandwidth, higher precision instrumentation equipment. The AD4000/AD4003 ADC is available in a small 10-lead footprint (3 mm \times 3 mm, LFCSP and 3 mm \times 5 mm, MSOP options), and is pin-compatible with the AD798x/AD769x ADC family.

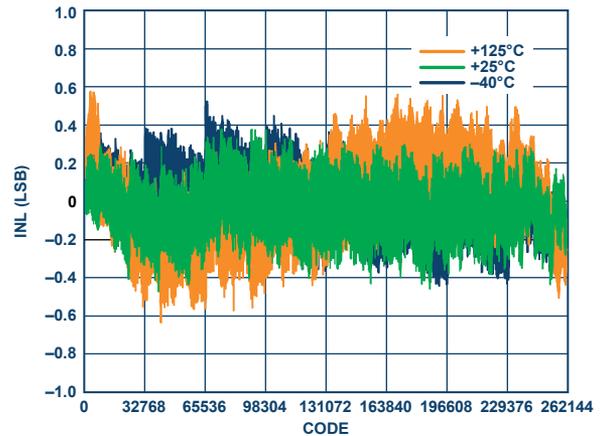


Figure 11. AD4003 ADC INL vs. code.

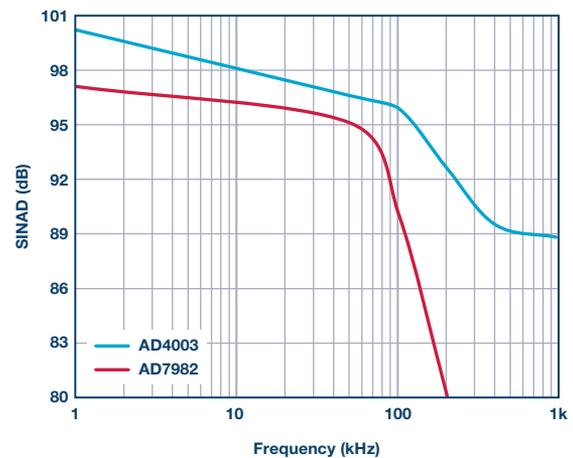


Figure 12. AD4003 ADC vs. AD7982 ADC SINAD vs. input frequency.

The AD4000/AD4003 ADC powers down automatically at the end of each conversion phase; therefore, its power scales linearly with the throughput as shown in Figure 13. This feature makes the device ideal for low sampling rates (even down to a few Hertz) and battery-powered portable and wearable systems. Even in low duty cycle applications, the first conversion result is always valid.

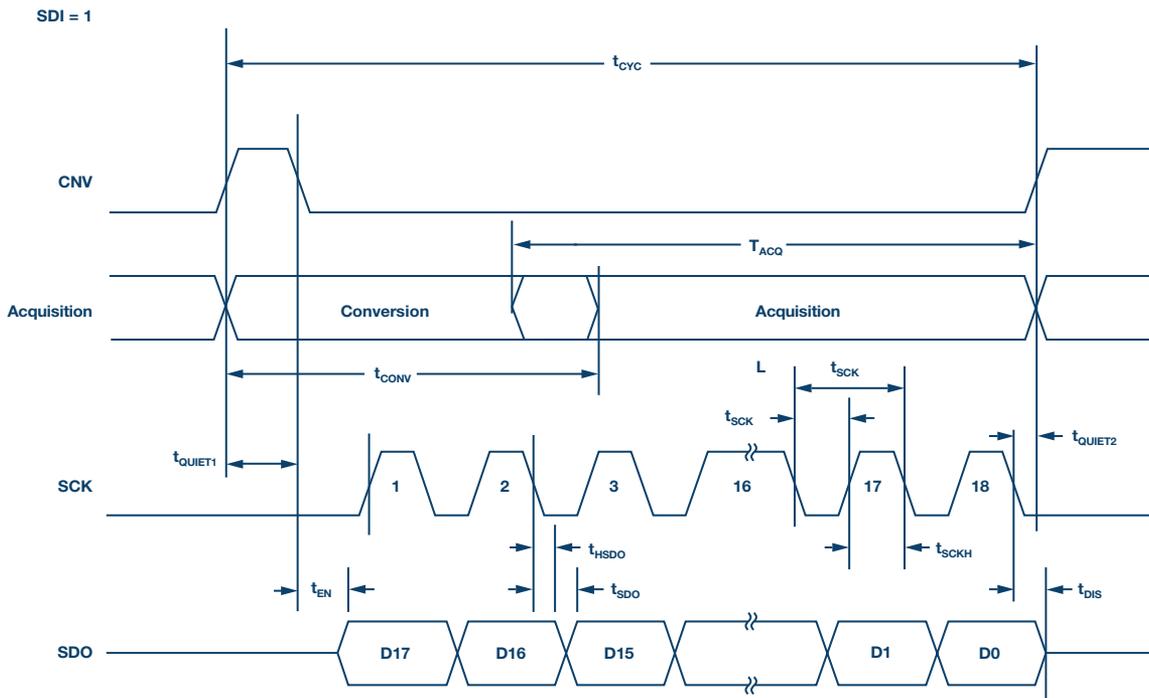


Figure 10. AD4003 ADC's turbo mode operation.

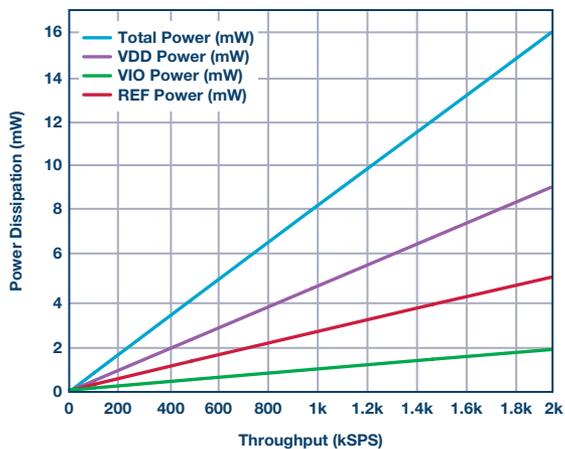


Figure 13. AD4003 ADC power dissipation vs. throughput.

System Applications

A combination of ease of use features and high performance, small footprint, and low power makes the AD4000/AD4003 ADC family a great solution for many precision control and measurement system applications as shown in Figure 14. The AD4000/AD4003 ADC reduces measurement uncertainty, increases repeatability, allows high channel density, and increases the throughput efficiency of automated test equipment, automated machine control equipment, and medical imaging equipment. This ADC is a good fit for systems that demand higher frequency performance to capture fast transients and time of flight information, such as power analyzer and mass spectrometer applications.

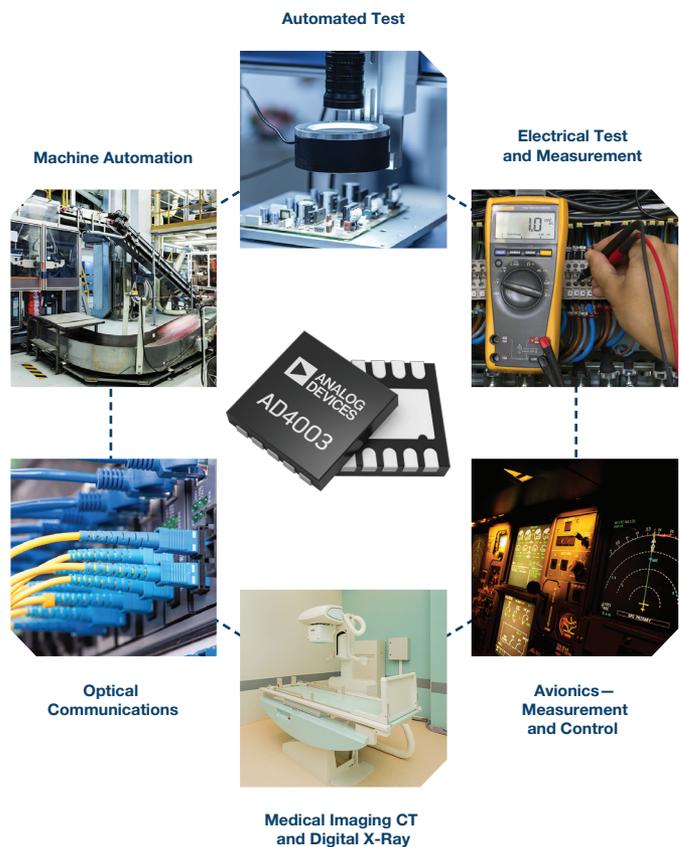


Figure 14. AD4000/AD4003 ADC end system applications.

Conclusion

The AD4000/AD4003 ADC family enables designers to solve the system-level technical challenges for their high precision data acquisition system without making significant trade-offs, reducing the total system design time. The AD4000/AD4003 ADC's high performance increases measurement accuracy and its small footprint coupled with low system-level thermal dissipation enables higher density.

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