Radically Extending Bandwidth to Crush the X-Band Frequencies Using a Track-and-Hold Sampling Amplifier and RF ADC

By **Rob Reeder**

Abstract

There are applications where raw analog bandwidth is paramount above all else and with the advent of GSPS or RF ADCs, Nyquist zones have grown by 10 fold in just a few years, reaching multi-GHz spans. This has helped these applications reach further into seeing over the horizon, but to reach X-band (12 GHz frequencies), more bandwidth is still required. The employment of a track-and-hold sampling amplifier (THA) in the signal chain can radically extend the bandwidth well beyond the ADCs sample bandwidth and provide the requirements needed by those designs that desire bandwidth the most. In this article, we will prove that designers can achieve 10 GHz bandwidth when using a THA in front of one of our newest RF market converters.

Introduction

With all the buzz surrounding GSPS converters due to their advantages in shortening both the RF signal chain and creating more resource fabric in the FPGA to be available—for example, when eliminating mix down stages on the front end and inclusion of digital downconverters (DDCs) on the back end, respectively—there is still the need for high frequency raw analog bandwidth (BW) in some applications that is well beyond what these RF converters can achieve. In these applications, most notably in the defense and instrumentation industry (with wireless infrastructure following suit), there still is an interest in fully extending the bandwidth out to or even past 10 GHz—covering beyond the C-band and fully encompassing the X-band if possible. As high speed ADC technology improves, so does the need to resolve very high intermediate frequencies (IF) accurately at high speeds in the GHz region, giving way to baseband Nyquist zones of more than 1 GHz wide and rapidly climbing. That statement might be out of date by the time this gets published, as developments in this area are extremely quick.

This poses two challenges: the converter design itself and the front-end design that couples the signal content to the converter—for example, the amplifier, balun, and PCB design. Even if the converter's performance is excellent, the front end must be capable of preserving the signal quality, too. These applications demand the use of high speed GSPS converters with resolutions of 8 bits to 14 bits—but remember, there are many parameters that need to be met in order to satisfy the match of the particular application.

Wideband, as defined in this article, is the use of signal bandwidths greater than 100s of MHz and ranging from near dc out into the 5 GHz to 10 GHz frequency region. In this article, the use of wideband THAs or active sampling networks will be discussed in order to achieve bandwidths to infinity and beyond (sorry, no *Toy Story* emoji available at this time), as well as highlighting its background theory, which enables a bandwidth extension of the RF ADC that might not have the capability on its own. Lastly, considerations and optimization techniques will be revealed in order to help designers realize a workable wideband solution in the multi-GHz region.

Laying the Foundation

It is natural to gravitate to GSPS converters for applications such as radar, instrumentation, and communication observation, because this presents a wider frequency spectrum, offering an extension of range in the system. However, a wider frequency spectrum poses even more challenges on the internal sample-and-hold of the ADC itself, as it is typically not optimized for ultrawideband operation and the ADC generally has limited bandwidth and degraded high frequency linearity/SFDR in these higher analog bandwidth regions.

Therefore, the use of a separate THA in front of the ADC is one possible solution to give rise to sampling at very high analog/RF input signals at a precise time instant. The process results in signal sampling by one low jitter sampler and reduces the ADC's dynamic linearity requirements over a wider range of bandwidth, as the sampled value is held constant during the RF analog-to-digital conversion process.

The result is a radical extension in analog input bandwidth, as well as a substantial improvement in high frequency linearity and improved high frequency SNR for the THA-ADC assembly, as compared to the performance of the RF ADC alone.

THA Characteristics and Overview

THAs offer precision signal sampling over 18 GHz bandwidth, with 9-bit to 10-bit linearity from dc to beyond 10 GHz input frequencies, 1.05 mV noise, and <70 fs random aperture jitter. The device can be clocked to 4 GSPS with minimal dynamic range loss—such cases include the HMC661 and HMC1061. These THAs can be used to expand the bandwidth and/or high frequency linearity of high speed analog-to-digital conversion and signal acquisition systems.

The single rank THA has one THA (such as HMC661) and produces an output that consists of two segments. In the track mode interval of the output waveform (positive differential clock voltage), the device behaves as a unity-gain amplifier that replicates the input signal at the output stage, subject to the input bandwidth and the output amplifier bandwidth limitations. At the positive to negative clock transition of the device, it samples the input signal with a very narrow sampling time aperture and holds the output relatively constant during the negative clock interval at a value that is representative of the signal at the instant of sampling. The single rank device (as opposed to its brother, the dual rank THA HMC1061) is often preferable for front-end sampling with ADCs, because most high speed ADCs already have a THA internally integrated—usually with much less bandwidth. Hence, the addition of a THA in front of the ADC forms a composite, dual rank assembly (or triple rank if the dual rank HMC1061 is used) with the THA in front of the converter. For equal technologies and designs, a single rank device will usually have better linearity and noise than a dual rank device, since the single rank has fewer stages. Hence, the single rank device is often the optimum choice for front-end sampling with high speed ADCs.

Delay Mapping the THA and ADC

One of the most difficult tasks in developing a track-and-hold and ADC signal chain is setting up the proper timing delay between the instant that the THA captures the sampled event and when it should be moved onto the ADC to resample the event. The process around setting up this perfect delta in time between two effective sampling systems is called delay mapping.

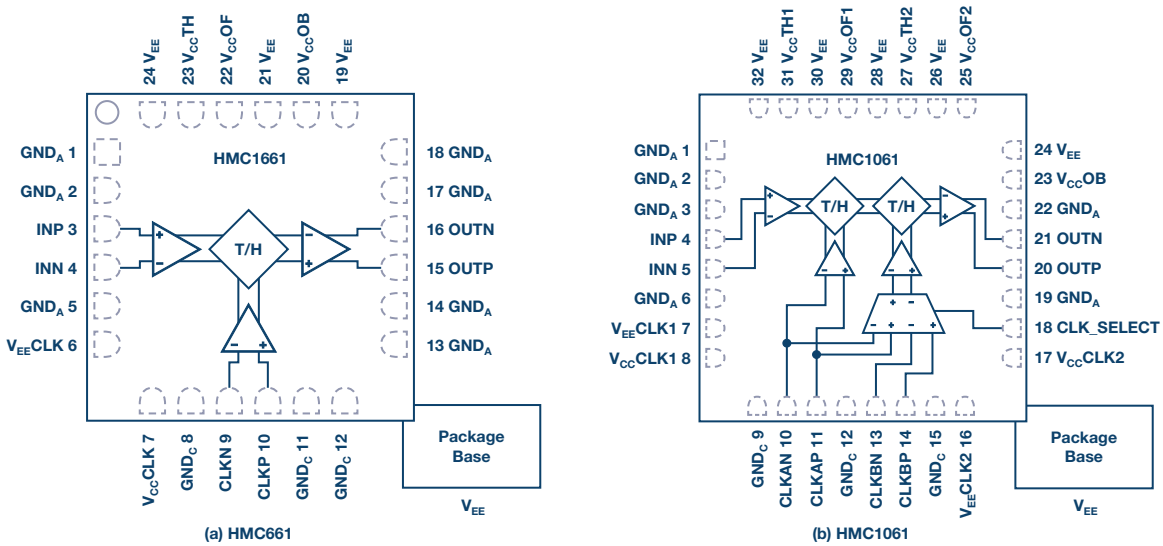

Figure 1. Track-and-hold topologies: (1a) single rank, (1b) dual rank.

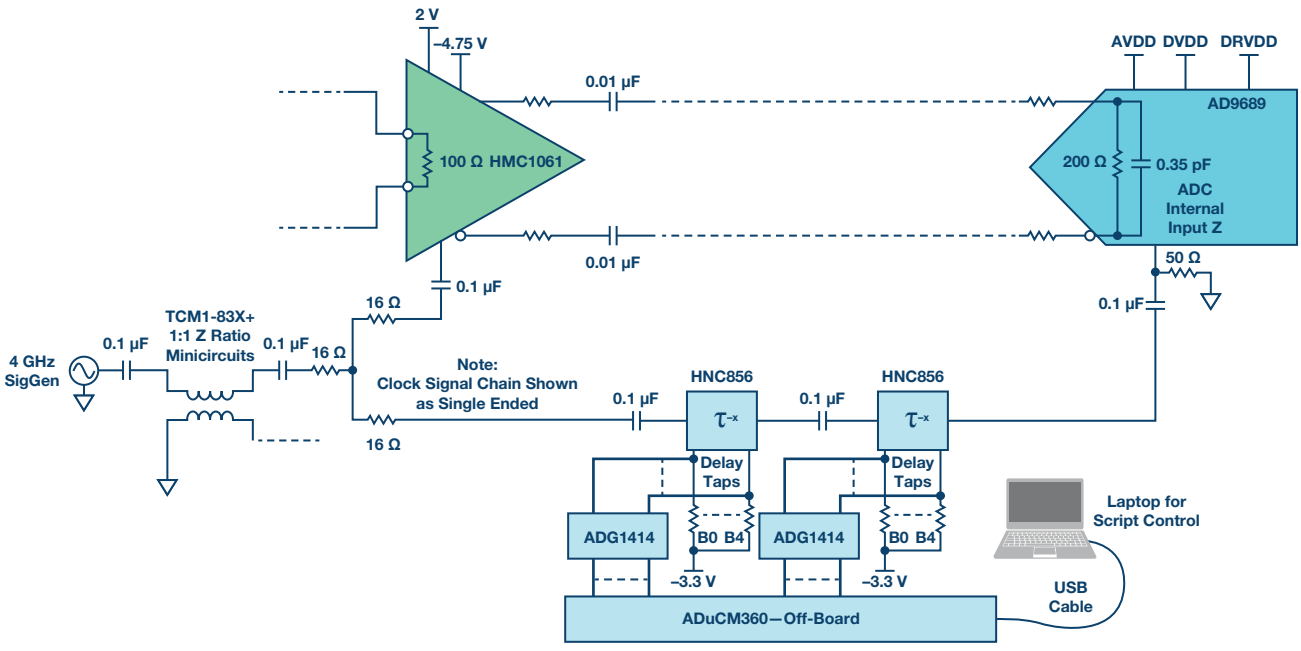

Figure 2. Delay mapping circuit.

The process can be tedious to accomplish on the board, because a paper analysis might not factor in the appropriate delays due to clock trace propagation intervals on the PCB board, internal device group delays, ADCs aperture delay, and the associated circuitry involved to split the clock into two different segments (one clock trace for the THA and one clock trace for the ADC). One way to set the delay between the THA and ADC is to use a variable delay line. These devices can be active or passive in order to properly time align the THA sampling process and handing it over to the ADC to sample. This guarantees that the ADC samples the settled hold-mode portion of the output waveform from the THA, yielding accurate representation of an incoming signal.

As shown in Figure 2, the HMC856 can be used to initiate the delay. This is a 5-bit/pin strappable device that has an inherent delay of 90 ps, a variable delay step size of 3 ps steps or 2^5, and 32 possible stepped delays. The disadvantage of a pin strap device is setting/moving through each delay setting. Each bit pin on the HMC856 would need to be pulled to a negative voltage to enable a new delay setting. Therefore, soldering in a pulldown resistor over 32 combinations to find the optimum delay setting can be a tedious task—so the use of an automated circuit was developed to help the delay setting process go faster, using serial controlled SPST switches and an off-board microprocessor.

In order to capture the best delay setting, a signal is applied to the THA and ADC combination, which should be outside the range of the ADC's bandwidth. In this case, we chose a ~10 GHz signal and applied a level captured on the FFT display of –6 dBFS. The delay settings are now swept in a binary stepped fashion, holding the signal constant at level and frequency. The FFT is now displayed and captured during the sweeping process, collecting the fundamental power and spurious-free dynamic range (SFDR) numbers at each delay setting.

As the results show in Figure 3a, the fundamental power, SFDR, and SNR will vary as each setting is applied. As shown, when the sample position is placed more optimally between the time the THA throws the sample over to the ADC, the fundamental power will be at its highest level, while the SFDR should be at its best performance (that is, lowest). Here a zoomed in view of the delay mapping sweep is shown in Figure 3b, outlining a delay setpoint of 671, which is the window/position where the delay should be kept fixed. Keep in mind that the delay mapping procedure is only valid with an associated sample frequency of the system, and would need to be reswept if the design calls for a different sample clock. In this case, the sample frequency is 4 GHz, which is the highest sample frequency for the THA device used in this signal chain.

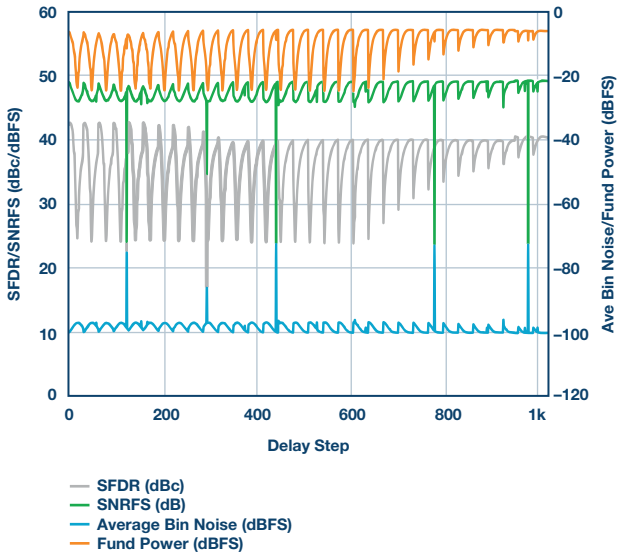

Figure 3a. Mapping results of signal amplitude and SFDR performance over each delay setting.

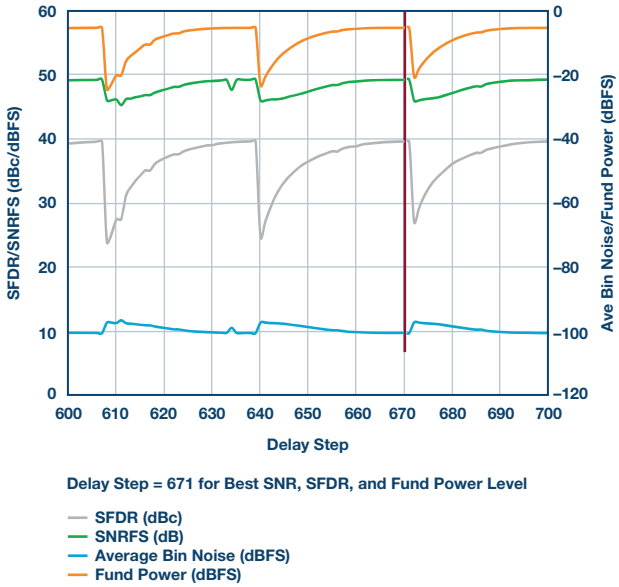

Figure 3b. Mapping results of signal amplitude and SFDR performance over each delay setting (zoomed in).

Designing Front Ends for Gobs of Raw Analog Bandwidth

First off, when the key goal in your application is swallowing 10 GHz of bandwidth, we obviously start to think in RF terms. Please be wary, the ADC is still a voltage type device and does not *think* in terms of power. So the word *match* is a term that should be used wisely in this case. It was found almost impossible to match a converter front end at every frequency with 100 MSPS converters—multi-GHz RF ADCs won't be much different, but the challenge is still there. The term match should be positioned to mean optimization, yielding the best results given for the front-end design. This would be an all-inclusive term where input impedance, ac performance (SNR/SFDR), signal drive strength or input drive, and bandwidth and its pass-band flatness yield the best results for that particular application.

These parameters altogether define the match for the system's application in the end. When embarking on a wideband front-end design, layout can be key, as well as minimizing the number of components necessary to create less loss between the two adjoining ICs. Both will be paramount in order to achieve the best performance. Careful attention needs to be given when tying the analog input networks together. Trace length and matching trace lengths are most important, along with the minimizing the number of vias, as seen in Figure 4.

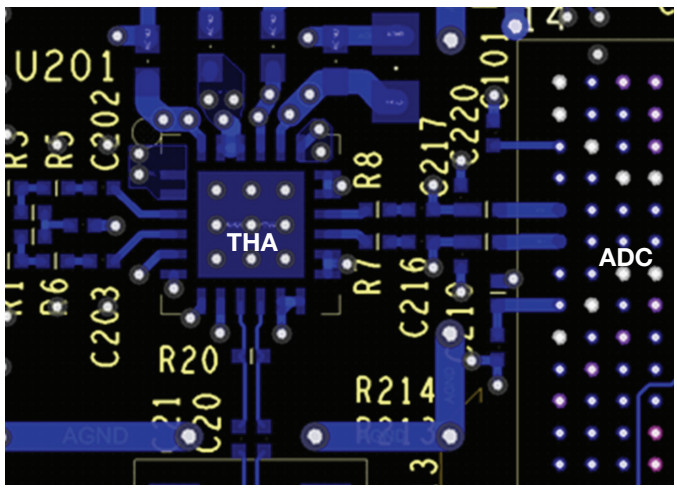

Figure 4. THA and ADC layout.

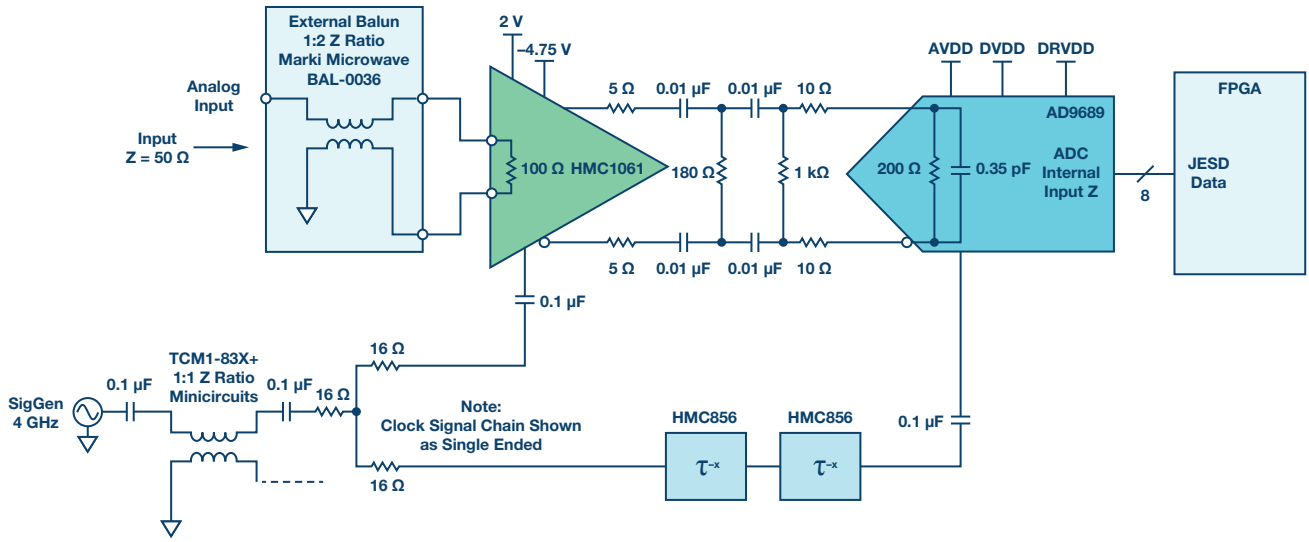

Figure 5. THA and ADC front-end network and signal chain.

These two differential analog inputs need to be brought together and connected to the THA outputs to form a single front-end network. To minimize the number of vias and overall length, careful attention was given here to pull the vias out of the two analog input paths, and to help offset any stubbing in the trace connections as well.

In the end, the final design is fairly simple with only a couple of points to note, as shown in Figure 5. The 0.01 µF capacitors used are broadband type and help to keep the impedance flat over a wide frequency range. Typical off-the-shelf type 0.1 µF capacitors just cannot give a flat impedance response and can cause some more ripple in the pass-band flatness response. The 5 Ω and 10 Ω series resistors on the outputs of the THA and inputs of the ADC help to reduce peaking on the THA outputs and minimize distortion caused by any residual charge injection from the ADC's own internal sampling capacitor network. However, these values need to be chosen wisely, otherwise this increases signal attenuation and forces the THA to drive harder, or the design might not be able to take advantage of the entire full scale of the ADC.

Lastly, let's discuss the differential shunt termination. These are paramount when it comes to connecting two or more converters together. Typically a light type load, in this case 1 kΩ at the inputs, helps with linearity and keeps the reverberating frequencies at bay. The 120 Ω shunt load at the split does just the same, but creates a more real load, in this case 50 Ω, which is exactly what the THA wants to see and is optimized for.

Now for the results! Looking at the signal-to-noise ration or SNR in Figure 6, it can be seen that 8 bits of ENOB (effective number of bits) can be achieved over a 15 GHz span. This is pretty good, considering you might have paid $120k for a 13 GHz oscilloscope with the same performance. The integrated bandwidth (that is, noise) and jitter limitations start to become a big factor in why a roll-off in performance is seen as the frequency moves through L-, S-, C-, and X-bands.

It should also be noted that, in order to keep the levels constant between the THA and ADC, the ADC's full-scale input was changed internally via an SPI register to 1.0 V p-p. This helps keep the THA within its linear region, since it has a maximum output of 1.0 V p-p differential.

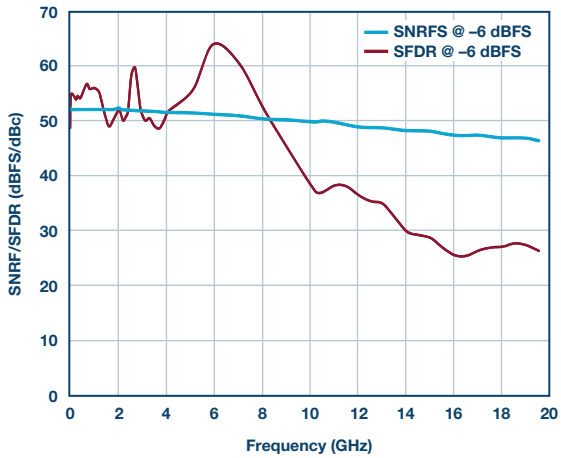

Figure 6. SNRFS/SFDR performance results at –6 dBFS.

The linearity results, or SFRD, are shown, too. Here, the linearity is above 50 dBc out to 8 GHz and hitting 40 dB out to 10 GHz. The design here was optimized using the AD9689 analog input buffer current setting features, via SPI control registers, in order to reach the best linearity over such a wide set of frequencies.

In Figure 7, the pass-band flatness is shown, proving that 10 GHz of bandwidth can be achieved by adding a THA in front of the RF ADC, fully extending the analog bandwidth of the AD9689.

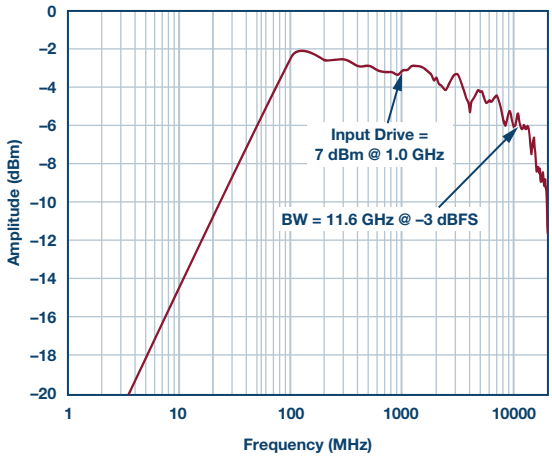

Figure 7. THA and ADC network and signal chain—bandwidth results.

Summary

For those applications that require best performance over multi-GHz analog bandwidths, the use of a THA is almost necessary, at least for today! RF ADCs are catching up fast. It is easy to see that GSPS converters offer ease of use, in theory, when it comes to sampling wider bandwidth to cover multiple bands of interest. This relives a mix down stage, or multiple thereof, on the front-end RF strip. However, achieving bandwidth in these higher ranges can pose design challenges and maintaining performance.

When using a THA in the system, make sure the position of the sampling point is optimized between the THA and ADC. Using a delay mapping procedure as described in this article will yield the best performance results overall. Understanding the procedure is tedious but it is paramount. Lastly, keep in mind matching a front end really means achieving the best performance given a set of performance needs per the application. The *Lego effect*—simply bolting 50 Ω impedance blocks together—just might not be the best approach when sampling at X-band frequencies.

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Acknowledgements

The author would like to thank Mike Hoskins, designer of the HMC661 and HMC1061 THAs, for his background knowledge, as well as Chas Frick and John Jefferson for scripting and running most of the data in the lab.

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