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The Interleaved Inverting Charge Pump—Part 1: A New Topology for Low Noise Negative Voltage Supplies

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Introduction

Noise must be minimized in precision instrumentation or radio frequency (RF) circuits, but reducing noise comes with a number of challenges due to the nature of these systems. For instance, these systems must often operate over a wide input voltage while meeting strict electromagnetic interference (EMI) and electromagnetic compatibility (EMC) requirements. Furthermore, systems are crowded with electronics, making them space-constrained and heat sensitive. The increasing complexity of integrated circuits (ICs) has led to an increase in the number of power supply voltage rails that these systems require. Generating all these rails, meeting the above requirements, and keeping the entire system low noise can be daunting.

Analog Devices offers a wide variety of solutions for producing low noise power. Most of these solutions are designed to produce positive voltage rails, with fewer dedicated ICs for generating negative voltages. This can be particularly limiting when the negative voltage needs to power low noise devices, such as RF amplifiers, switches, and data converters (ADCs and DACs).

In Part 1 of this article series, we introduce a new method to generate this low noise negative rail from a positive supply. It starts with a general understanding of how negative rails are typically generated and where they are used. Then we discuss the standard inverting charge pump before introducing an interleaved inverting charge pump (IICP) topology. A short derivation of the input and output voltage ripple for the IICP emphasizes its unique advantages for low noise systems.

Part 2 of the series gives a practical example of an IICP implementation with Analog Devices' new ADP5600. We first compare this part to a standard inverting charge pump by measuring voltage ripple and radiated emissions. Then we use the equations from Part 1 to optimize the IICP performance and develop a complete solution for powering a low noise RF circuit.

Traditional Negative Voltage Generation Methods

To create a negative voltage, one of two methods is commonly employed: use an inductive switching regulator or use a charge pump. Inductive switchers use an inductor or transformer to generate the negative voltage. Examples of these magnetic converter topologies are: inverting buck, inverting buck-boost, and Ćuk. Each of these has its own set of advantages and disadvantages regarding solution size, cost, efficiency, noise generation, and control loop complexity.[1, 2] In general, the magnetics-based converters are best suited when higher output currents are required (> 100 mA).

For applications requiring less than 100 mA of output current, charge pump positive-to-negative (inverting) dc-to-dc converters can be very small and feature low EMI because no inductors or control loops are required. They simply require moving charge between capacitors via switches—supplying the resulting charge to the output.

Because charge pumps use no magnetics (inductors or transformers), they typically feature lower EMI than inductive switching topologies. Inductors tend to be much larger than capacitors, and unshielded inductors act like antennas by broadcasting radiated emissions. In contrast, the capacitors used in a charge pump do not produce any more EMI than a typical digital output. They can be easily routed in short traces to reduce antenna area and capacitive coupling, resulting in lower EMI.

Table 1 compares inductor-based switching regulator and switched capacitor inverting topologies.

Table 1. Comparison of Magnetic and Inverting Charge Pumps

Features	Inductor-Based Switching Regulator	Switched Capacitor Voltage Converter
Design Complexity	Moderate to high	Low
Cost	Moderate to high	Low to moderate
Noise	Low to moderate	Low
Efficiency	High	Low to moderate
Thermal Management	Best	Moderate to good
Output Current	High	Low
Requires Magnetics	Yes	No
Limitations	Size and complexity	V_{IN}/V_{OUT} ratio

Traditional Inverting Charge Pump

The configuration of the traditional inverting charge pump is shown in Figure 1.

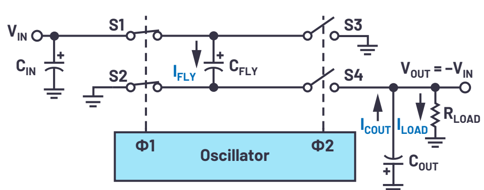

Figure 1. Inverting charge pump schematic.

The output impedance, R_{OUT}, of the charge pump is defined as the equivalent resistance of the charge pump mechanism from input to output. It is found by measuring the input to output voltage difference and dividing by the load current:

$$R_{OUT} = \frac{V_{IN} - GAIN \times V_{OUT}}{I_{LOAD}} \tag{1}$$

where GAIN = –1 for an inverting charge pump.

Alternatively, the equivalent output resistance can be calculated as a function of switching frequency, switch resistance, and flyback capacitor size—generally simplified as:

$$R_{OUT} = \frac{1}{f_{OSC} \times C_{FLY}} + 2 \times \sum_1^4 R_{ON} \tag{2}$$

where $\sum_1^4 R_{ON}$ is the summation of the four switches' resistance.

Each of the four switches operates at the same frequency, f_{OSC}, and they are on for one half of the switching period, T, where $T = 1/f_{OSC}$. Operation can be separated into two phases based on the two halves of the switching period, as shown in Figure 2.

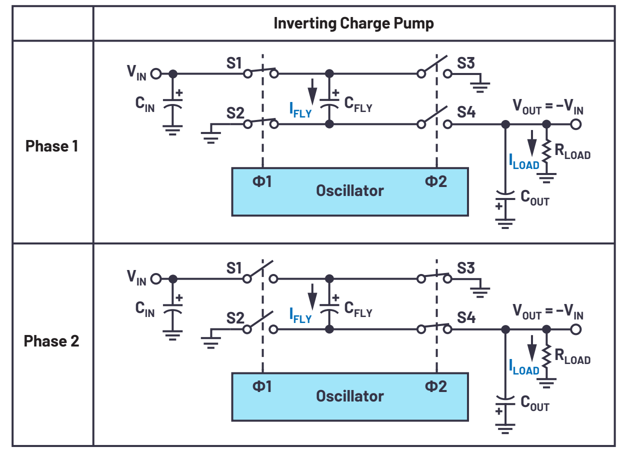

Figure 2. Inverting charge pump during each phase of operation.

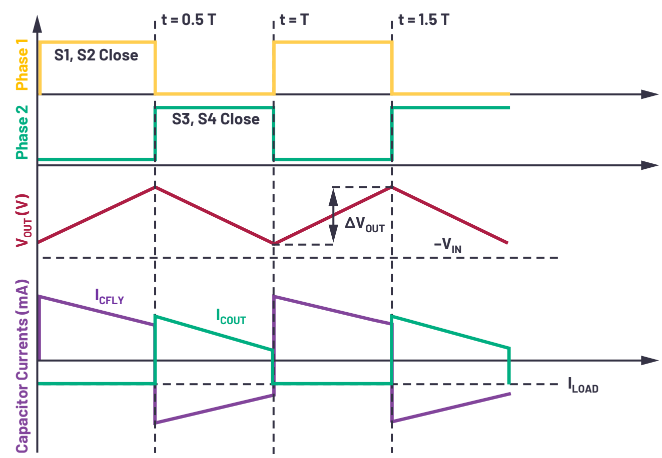

Figure 3. Timing diagram for inverting charge pump.

Figure 3 gives the voltages and currents for each phase of the charge pump's operation. In Phase 1, S1 and S2 are closed and S3 and S4 are open. This charges the flying capacitor (C_{FLY}) to a voltage of $+V_{IN}$. In Phase 2, the energy from C_{FLY} is discharged into the output by opening S1 and S2 and closing S3 and S4. The two distinct phases of operation means that discontinuous current flows into C_{FLY} from V_{IN}, and discontinuous current flows out of C_{FLY} into C_{OUT}. This leads to voltage ripple on C_{IN} and C_{OUT}, which can be calculated:

$$I_{LOAD} = C_{OUT} \frac{\Delta V_{OUT}}{\Delta t} \tag{3}$$

Solving for output voltage ripple gives:

$$\Delta V_{OUT} = \frac{I_{LOAD}}{C_{OUT} \times 2 \times f_{OSC}} \tag{4}$$

Similarly, the input voltage ripple is:

$$\Delta V_{IN} = \frac{I_{LOAD}}{C_{IN} \times 2 \times f_{OSC}} \tag{5}$$

Equation 4 and Equation 5 illustrate that, for a standard inverting charge pump, the voltage ripple is a function of switching frequency and input (or output) capacitance. Higher frequency and higher capacitance reduce this ripple in a 1:1 relationship. However, there are practical impediments to increasing frequency: namely increasing current consumption of the chip, which decreases efficiency.

Similarly, cost and PCB area often restrict the maximum input and output capacitance of an inverting charge pump. Also note that the flyback capacitor plays no role in the charge pump's voltage ripple.

To reduce ripple, input and output filters could be constructed around the charge pump, but this again increases complexity and the charge pump's output resistance. However, these issues can be addressed with a novel improvement to the standard inverting charge pump inverter: an interleaved inverting charge pump (IICP).

Interleaved Inverting Charge Pump (IICP)

Phase interleaving is widely used in inductive switching regulators (that is, polyphase operation) to reduce output voltage ripple.[3] A 2-phase buck converter interleaved at exactly 50% duty cycle produces, in theory, 0 mV of output voltage ripple. Of course, the duty cycle of a regulated buck converter changes with input and output voltage, so the 50% case is only realized when $V_{IN} = 2\ V_{OUT}$. Charge pumps usually operate at exactly 50% duty cycle, so an interleaved charge pump inverter is interesting to consider.

Interleaving charge pumps are sometimes used within ICs when a very low current negative rail is required on the die, but right now there is no commercially available dedicated IICP inverting dc-to-dc converter. The construction of an IICP requires two charge pumps and two flying capacitors. The second charge pump operates the switches 180° out of phase with the first charge pump. Let's look at the setup and the output ripple of an IICP and highlight how to optimize its performance. The setup is shown in Figure 4 with the timing diagram in Figure 5.

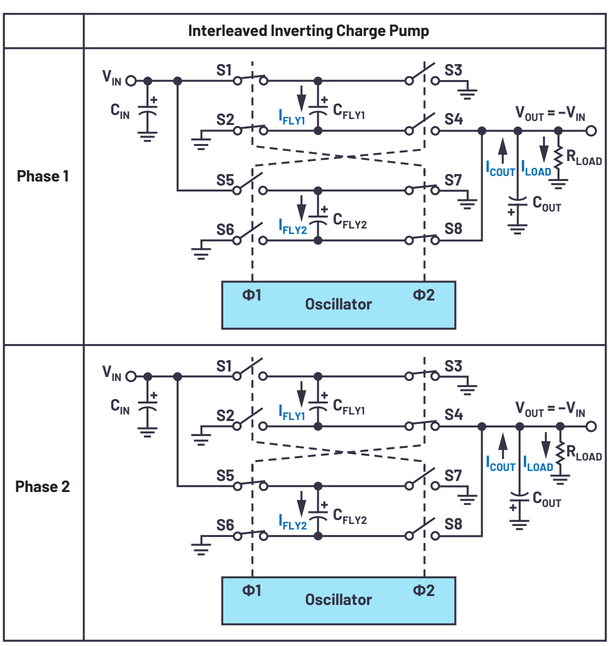

Figure 4. Interleaved inverting charge pump.

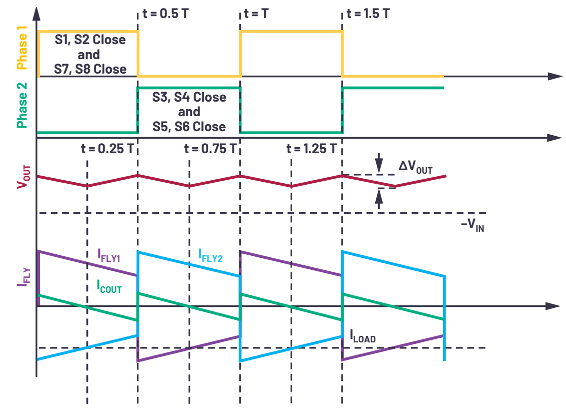

Figure 5. Timing diagram for interleaved inverting charge pump.

In each phase of the oscillator, one of the flying capacitors is connected to V_{IN} and the other is connected to V_{OUT}. At first glance, one might think that the addition of the second capacitor would only reduce the voltage ripple by half. However, this is an inaccurate oversimplification. In fact, the input and output voltage ripple can be far less than a standard inverter, because a capacitor is always charging from the input and discharging to the output. This can be better understood from the derivation of the IICP's output voltage ripple.

IICP Output Voltage Ripple Derivation

Since the IICP always has one of the flying capacitors supplying current to the output, its output stage can be simplified, as shown in Figure 6.

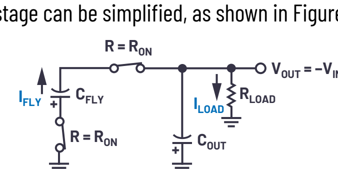

Figure 6. Simplified IICP output stage.

Furthermore, the IICP's output resistance, as defined in Equation 1, can be approximated by:

$$R_{OUT} \approx \frac{1}{8 \times f_{OSC} \times C_{FLY}} + 0.5 \times \Sigma_1^8 R_{ON} \quad (6)$$

where $\Sigma_1^8 R_{ON}$ is the summation of the switch resistances.

Summing the currents into I_{LOAD}, we arrive at:

$$I_{LOAD} = C_{OUT}\frac{dV_{OUT}}{dt} + C_{FLY}\frac{dV_{CFLY}(t)}{dt} \quad (7)$$

Where dt is equal to a quarter of the switch period (T/4, or $1/(4 \times f_{OSC})$). The output voltage ripple, ΔV_{OUT}, is dV_{OUT} and $V_{CFLY}(t)$ is the voltage difference across C_{FLY}. We can make the reasonable assumption that output voltage ripple is small relative to the flying capacitor voltage ripple. Then to calculate ΔV_{OUT}, we need an understanding of $V_{CFLY}(t)$. From Figure 6, note that I_{FLY} is equal to the current through the two on switches. And each of those switches has a resistance of R_{ON}. Therefore:

$$C_{FLY}\frac{dV_{CFLY}(t)}{dt} = \frac{V_{CFLY}(t) - |V_{OUT}|}{2 \times R_{ON}} \quad (8)$$

To solve this differential equation for $V_{CFLY}(t)$, at least one initial condition must be known. This condition can be found via inspection of the timing graphs in Figure 5. Note that from t = 0 to t = T/4, both C_{FLY} capacitors contribute current to I_{LOAD} and charge C_{OUT}. Then, from t = T/4 to t = T/2, C_{FLY} and C_{OUT} contribute to the output load current. So, right at t = T/4 (and similarly t = 3/4 T), the contribution to I_{LOAD} from C_{OUT} is exactly 0. Therefore, at this moment, I_{LOAD} is equal to I_{FLY}, and the voltage of V_{CFLY} is given by:

$$V_{CFLY}(t = T/4) = |V_{OUT}| + I_{FLY} \times 2 \times R_{ON} \quad \text{where } V_{OUT} = -V_{IN} + R_{OUT} \times I_{LOAD} \tag{9}$$

Using Equation 8 and Equation 9, we can differentially solve for $V_{CFLY}(t)$:

$$V_{CFLY}(t) = |V_{OUT}| + |I_{LOAD}| \times (R_{OUT} - 2 \times R_{ON}) \times \beta^{1.5} \quad \text{where } \beta = e^{1/8fRC} \quad \text{where } f \text{ is } f_{OSC},\ R \text{ is } R_{ON},\ \text{and } C \text{ is } C_{FLY} \tag{10}$$

To find the delta in V_{CFLY} for Equation 7, take two points (for example, t = 0 and t = T/4), and solve Equation 10 for each of those points. The result simplifies to:

$$\Delta V_{CFLY} = I_{LOAD} \times (R_{OUT} - 2 \times R_{ON}) \times \frac{\beta - 1}{\sqrt{\beta}} \tag{11}$$

Combining Equation 11 and Equation 7, and solving for ΔV_{OUT} gives:

$$\Delta V_{OUT} = \frac{I_{LOAD}}{4 \times f_{OSC} \times C_{OUT}} - I_{LOAD} \times (R_{OUT} - 2 \times R_{ON}) \times \frac{C_{FLY}}{C_{OUT}} \times \frac{\beta - 1}{\sqrt{\beta}} \tag{12}$$

The impact of Equation 12 may not be initially obvious. It may help to first simplify it by considering the case of an ideal switch (R_{ON} = 0 Ω). Doing so brings the second term to nearly zero, leaving only the first term. That first term is very similar to the standard inverting charge pump ripple (Equation 4), but the dual flying capacitors of the IICP increase the denominator by 2×. Twice the charge pumps yields half the ripple. This result is consistent with intuition.

However, the important part of Equation 12 lies in the second half. Note the minus sign for the second term, meaning that this portion reduces the output voltage ripple. Focus on the switch resistance (R_{ON}) and the flying capacitor (C_{FLY}). In a standard inverting charge pump, these terms play no role in reducing the output voltage ripple. But in an IICP, the switch resistance acts to smooth out the charge and discharge current. The dual flying capacitors allow this charge/discharge action to happen uninterrupted.

Output Voltage Ripple Confirmation

We can use circuit simulation to check the accuracy of Equation 12 and the validity of the assumptions used to derive it. This is easily accomplished using LTspice®. The schematic for this simulation is shown in Figure 7, and the file is available for download.

A comparison was performed for a variety of conditions, with a summary of the results in Table 2.

Table 2. Comparison of Theoretical vs. LTspice Simulation Results for Various Configurations

V_{IN} (V)	I_{LOAD} (mA)	f_{OSC} (kHz)	C_{OUT} (µF)	C_{FLY} (µF)	R_{ON} (Ω)	V_{OUT} Ripple (mV)	
						Equation	LTspice
10	50	1000	4.7	2.2	2	0.038	0.038
5	100	1000	4.7	2.2	2	0.076	0.075
5	50	1000	1	1	2	0.393	0.390
5	50	1000	1	1	3	0.261	0.260
7.8	37	532	2.4	0.5	4	0.430	0.425
5	100	1000	10	2.2	3	0.024	0.024
5	50	200	4.7	1	10	0.418	0.415
12	50	500	10	1	10	0.031	0.033
12	20	500	4.7	1	3	0.089	0.089

Table 2 shows that Equation 12 closely matches simulation, validating the assumptions made in simplifying the equations. Now we can use that equation to make trade-offs in the IICP implementation.

It's also instructive to compare the voltage ripple between an IICP and a standard charge pump. In Part 2 of this series, we will show bench test data of these differences. But for now, our LTspice model in Figure 8 can illustrate the difference in output voltage ripple.

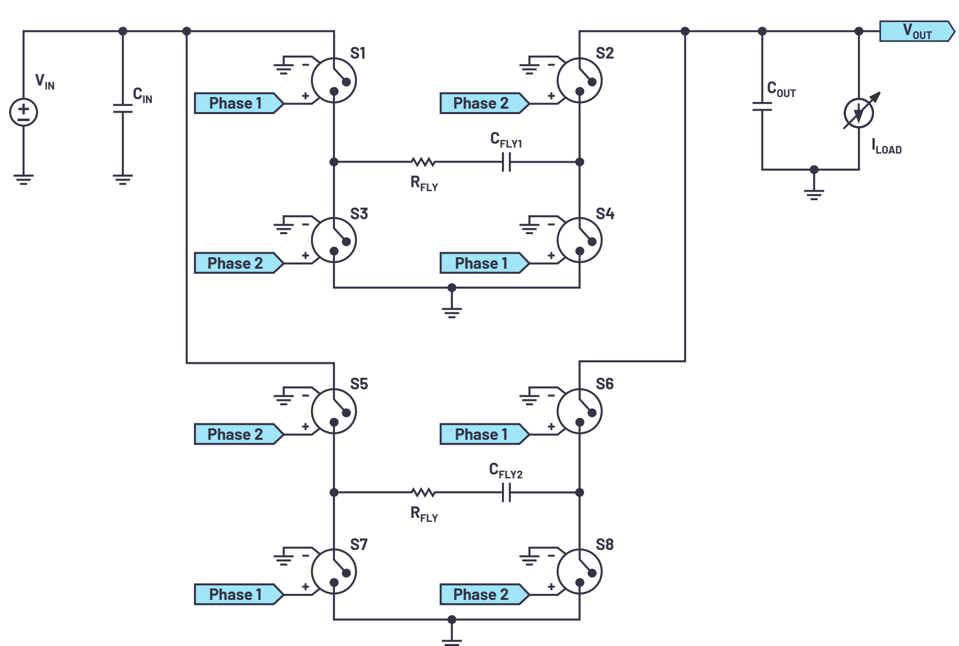

Figure 7. Interleaved inverting charge pump in LTspice.

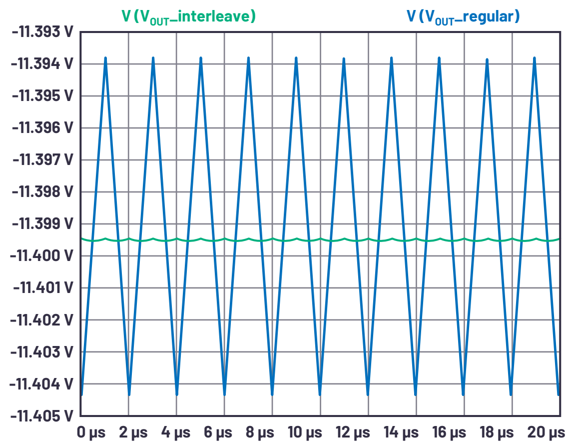

Figure 8. Output voltage ripple of an IICP vs. a regular charge pump: V_{IN} = 12 V, I_{LOAD} = 50 mA, C_{FLY} = 2.2 µF, C_{OUT} = 4.7 µF, R_{ON} = 3 Ω. To make the comparison fair to the regular charge pump, its R_{ON} was halved and C_{FLY} was doubled.

Optimization of IICP Topology

Having derived the IICP equations and proved their validity, there are two primary conclusions:

For the IICP, the switch resistance (R_{ON}) reduces both input and output voltage ripple, a desired result. In contrast, in a standard inverting charge pump, the switch resistance is entirely undesirable, as it increases the R_{OUT} of the charge pump and provides no ripple voltage reduction. In fact, we could further augment the switch resistance by placing a resistor in series with the flyback capacitor. This gives us a knob to reduce input and output voltage ripple at the expense of increased charge pump resistance. We'll explore this knob further when we discuss use cases of the IICP in Part 2 of this series.

Secondly, the value of the flying capacitors, and their ratio with C_{OUT}, can be optimized to further optimize the ripple. For example, a large output capacitor value may be difficult to find in a small package, and subject to a significant capacitance derating at higher voltages. But by reducing C_{OUT}, and then increasing C_{FLY}, the same output voltage ripple can be obtained for more attainable values of capacitance. For example, instead of C_{FLY} = 1 µF and C_{OUT} = 10 µF, if they were all set to 2.2 µF, then nearly the same output voltage ripple is attained. 2.2 µF/25 V capacitors are more readily available in small packages than 10 µF/25 V capacitors. An example application in Part 2 explores this.

Conclusion

This concludes Part 1 of the 2-part series on the interleaved inverting charge pump topology. This part covers the general concepts behind an IICP topology, including input/output voltage ripple calculations. The derivation of the equations governing input/output ripple yields important insights into how to optimize the performance of an IICP solution.

In Part 2 of the series, we unveil the ADP5600, an integrated solution for the IICP topology. We measure its performance and compare to a standard inverting charge pump. Finally, we'll put it all together to power a low noise phased array beamforming solution.

References

[1] Jaino Parasseril. "How to Produce Negative Output Voltages from Positive Inputs Using a µModule Step-Down Regulator." Linear Technology.

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[3] Majing Xie. "High Power, Single Inductor, Surface-Mount Buck-Boost µModule Regulators Handle 36 V_{IN}, 10 A Loads." Linear Technology, March 2008.

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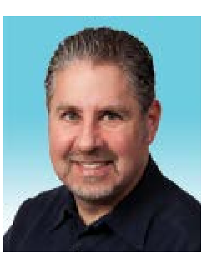

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