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Optimizing Power Systems for the Signal Chain—Part 2: High Speed Data Converters

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Introduction

In Part 1 of this power system optimization series, we examined how power supply noise sensitivity can be quantified and how these quantities can be connected to real effects in the signal chain. The question was asked: What are the real noise limits to achieve superior performance of high performance analog signal processing devices? Noise is just one measurable parameter in designing a power distribution network (PDN). As noted in Part 1, a pure focus on minimizing noise can come at the cost of increased size, higher cost, or lower efficiency. Optimizing a power distribution network improves these parameters, while lowering noise to necessary levels.

This article builds on the generalized overview of the effects of power supply ripple in high performance signal chains. Here, we dive deeper into the details of optimizing power distribution networks for high speed data converters.

We compare a standard PDN to an optimized PDN to see where gains can be made in space, time, and cost. Subsequent articles will explore specific optimization solutions for other signal chain devices, such as RF transceivers.

Power System Optimization for the AD9175 Dual 12.6 GSPS High Speed Digital-to-Analog Converter

The AD9175 is a high performance, dual, 16-bit digital-to-analog converter (DAC) that supports DAC sample rates up to 12.6 GSPS. The device features an 8-lane, 15.4 Gbps JESD204B data input port; a high performance, on-chip DAC clock multiplier; and digital signal processing capabilities targeted at single-band and multiband direct to radio frequency (RF) wireless applications.
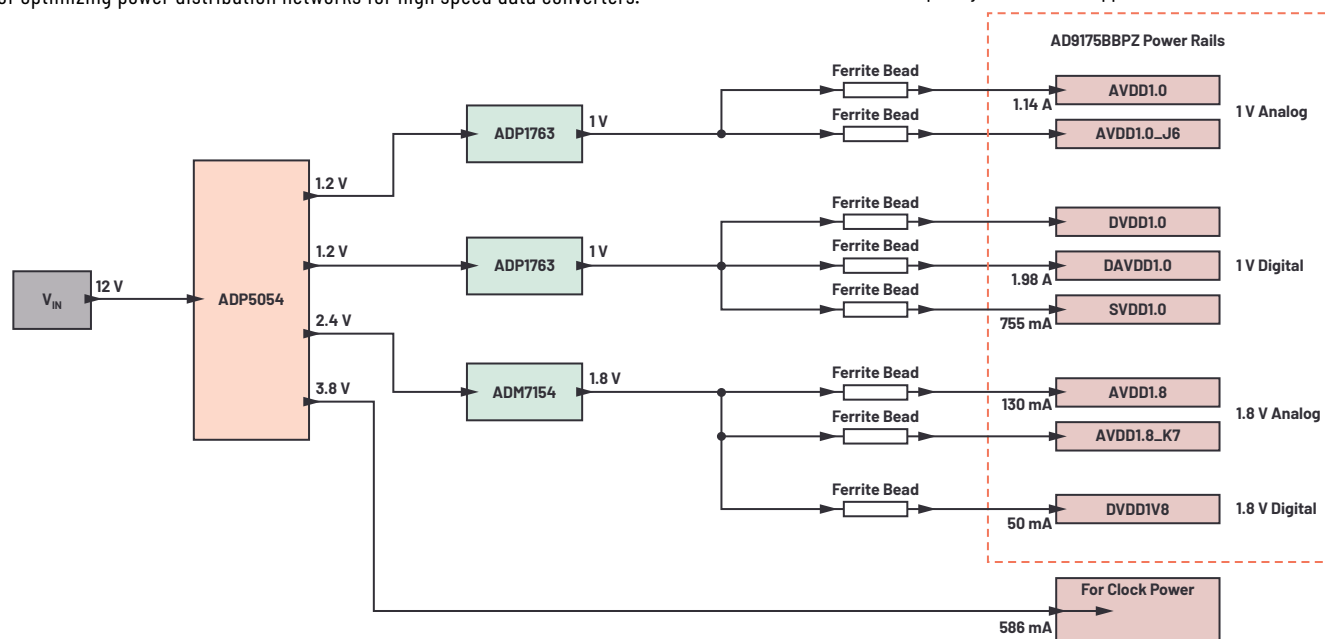

Figure 1. Standard PDN of an AD9175 high speed DAC, which comes on the off-the-shelf evaluation board.

Let's look at optimizing a PDN for this dual high speed DAC. Figure 1 shows the standard power distribution network for the AD9175 high speed DAC as installed on the off-the-shelf evaluation board. The PDN comprises an ADP5054 discrete quad switcher and three low dropout (LDO) postregulators. The goal is to see if this PDN can be improved and simplified, while ensuring its output noise does not cause any significant degradation in the DAC performance.

The AD9175 requires eight power rails, which can be collected into four groups, namely:

▶ 1 V analog (two rails)
▶ 1 V digital (three rails)
▶ 1.8 V analog (two rails)
▶ 1.8 V digital (one rail)

Analysis: Noise Requirements

Before we can optimize anything, we must understand the power supply sensitivity of these rails. We will focus on the analog rails, as they tend to be more sensitive to noise than the digital rails.

The power supply modulation ratio (PSMR) of the analog rails is shown in Figure 2. Note that the 1 V analog rails are relatively more sensitive at the 1/f frequency region, while the 1.8 V analog rails are more sensitive in the range of switching converter operating frequencies (100 kHz to around 1 MHz).
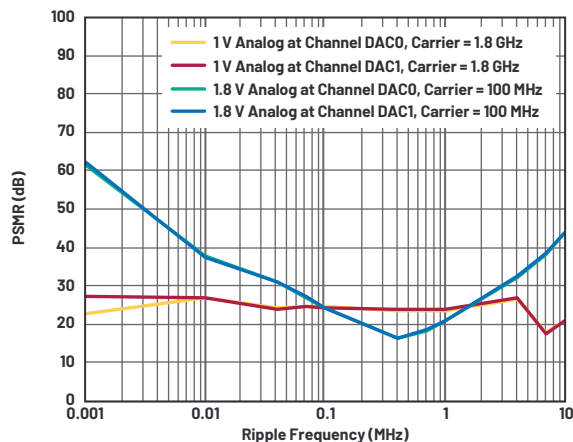
Figure 2. AD9175 high speed DAC PSMR at 1 V analog and 1.8 V analog rails.

One approach to optimization is to use a low noise switching regulator with an LC filter. Figure 3 shows the conducted spectral output of the LT8650S Silent Switcher® regulator (with and without an LC filter) with spread spectrum frequency modulation (SSFM) mode off. As discussed in Part 1, SSFM reduces the switching frequency noise amplitude but introduces noise peaks in the 1/f region due to the triangular modulation frequency. This added noise would exceed the maximum allowable ripple threshold for this rail as the 1/f noise already has a small margin from that threshold. Thus, SSFM is not recommended to be used in this case. The maximum allowable voltage ripple threshold represents the power supply ripple level at which when exceeded, sideband spurs in the DAC carrier signal appear above the 1 μV p-p noise floor of the DAC output spectrum.

It can be seen from these results that the 1/f noise of the switching regulator does not exceed the maximum allowable ripple threshold of the 1 V analog rail. Also, an LC filter is sufficient to knock down the fundamental switching ripple and harmonics of LT8650S below the maximum allowable ripple threshold.
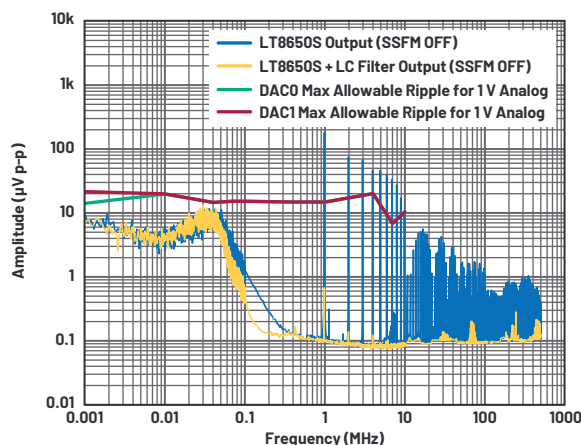
Figure 3. LT8650S conducted spectral output vs. maximum allowable ripple threshold for the 1 V analog rail.

Figure 4 shows the conducted spectral output of the LT8653S (with and without an LC filter). Also shown is the maximum allowable voltage ripple for the 1.8 V rail that will not produce spurs in the 1 μV p-p noise floor of the AD9175 output spectrum. It can be seen that the 1/f noise of the LT8653S does not exceed the maximum allowable ripple threshold, and an LC filter is sufficient to knock down the fundamental switching ripple and harmonics of LT8653S below the maximum allowable ripple threshold.
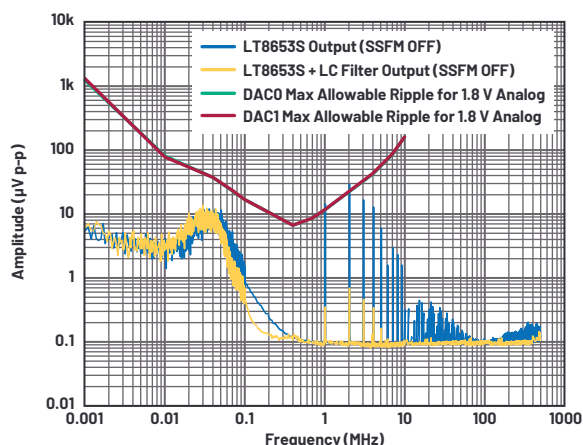
Figure 4. LT8653S conducted spectral output vs. maximum allowable ripple threshold for the 1.8 V analog rail.

Results: Optimized PDN

Figure 5 shows an optimized power distribution network of AD9175. The goal is to raise efficiency and reduce space requirements and power loss over the PDN in Figure 1 while achieving AD9175 superior dynamic performance. The noise goals are based on the maximum allowable ripple threshold shown in Figure 3 and Figure 4.

The optimized power distribution network consists of LT8650S and LT8653S Silent Switcher regulators followed by LC filters on the analog power rails. In this PDN, the 1 V analog rail is powered by the V_{OUT1} of the LT8650S followed by an LC filter; the 1 V digital rail is directly powered by the V_{OUT2} of the same LT8650S, no LC filter required. For the AD9175, the digital rails are less sensitive to power supply noise, so directly powering these rails is possible without degrading the DAC dynamic performance. The LT8653S with LC filter directly powers the 1.8 V analog and 1.8 V digital rails.

Table 1 compares the performance of the optimized PDN to the standard PDN shown in Figure 1—a quad buck switcher with three LDO regulators. The component area reduction of the optimized solution is 70.2% over the standard. Furthermore, efficiency is increased to 83.4% (from 69.2%) with an overall power saving of 1.0 W.

Table 1. Comparison of an AD9175 Optimized PDN to the Standard PDN

	Standard PDN (Figure 1)	Optimized PDN (Figure 5)	Improvement of the Optimized PDN from the Standard PDN
Component Area	142.4 mm²	42.4 mm²	70.2%
Overall Efficiency	69.2%	83.4%	14.2%
Power Loss	1.8 W	0.8 W	1.0 W

To verify that the noise performance of the optimized PDN did not degrade the dynamic performance of the DAC, the AD9175 is evaluated in terms of phase noise and inspecting the DAC output spectrum of sideband spurs around the carrier.[1] Phase noise results are comparable between the standard PDN and optimized PDN, as shown in Table 2. The output spectrum of AD9175 has a clean carrier frequency with no visible sideband spurs, as shown in Figure 6.
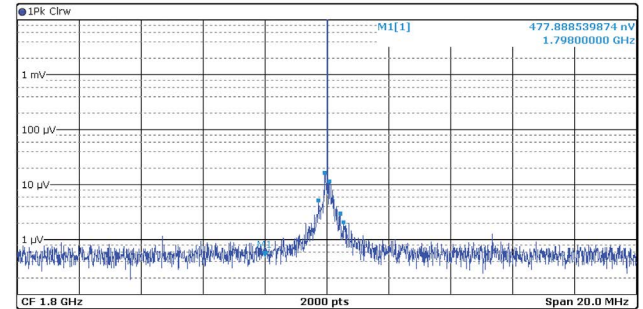

Figure 6. AD9175 output spectrum (at 1.8 GHz, –7 dBFS carrier) using the optimized PDN.

Table 2. AD9175 Phase Noise Performance Using the Standard PDN and Optimized PDN

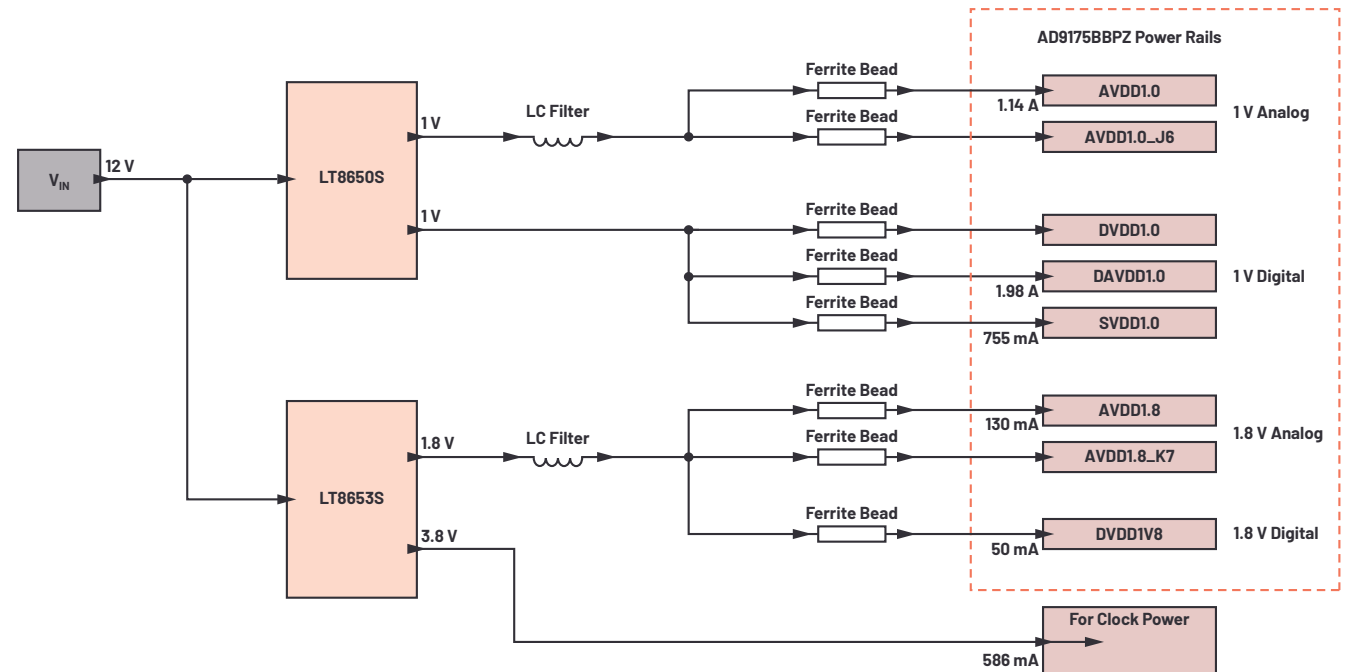| Frequency Offset	Phase Noise (dBc/Hz)			
	Standard PDN (Figure 1)		Optimized PDN (Figure 5)	
	DAC0	DAC1	DAC0	DAC1
1.0 kHz	–91	–91	–91	–91
10.0 kHz	–99	–99	–99	–99
100.0 kHz	–110	–110	–110	–110
600.0 kHz	–125	–125	–125	–125
1.2 MHz	–134	–134	–134	–134
1.8 MHz	–137	–137	–137	–137
6.0 MHz	–148	–148	–148	–148

Figure 5. Optimized PDN for an AD9175 high speed DAC.

Power System Optimization for the AD9213 10.25 GSPS High Speed Analog-to-Digital Converter

The AD9213 is a single, 12-bit, 6 GSPS or 10.25 GSPS, radio frequency (RF) analog-to-digital converter (ADC) with a 6.5 GHz input bandwidth. The AD9213 supports high dynamic range frequency and time domain applications requiring wide instantaneous bandwidth and low conversion error rates (CER). The AD9213 features a 16-lane JESD204B interface to support maximum bandwidth capability.

Figure 7 shows a standard power distribution network for the AD9213 high speed ADC—as found on the off-the-shelf evaluation board—consisting of an LTM4644-1 µModule® quad switcher and two linear regulators. This solution is fairly space efficient and energy efficient, but can it be improved? As noted throughout this series, the first step to optimization is quantifying the sensitivity of AD9213—that is, realistically setting the limits of PDN output noise so it does not cause significant degradation in the ADC performance. Here we'll look at an alternate PDN solution using two µModule regulators and compare its performance against the standard off-the-shelf solution.

The AD9213 10 GSPS ADC requires 15 different power rails, collected into four groups:

- 1 V analog (three rails)
- 1 V digital (six rails)
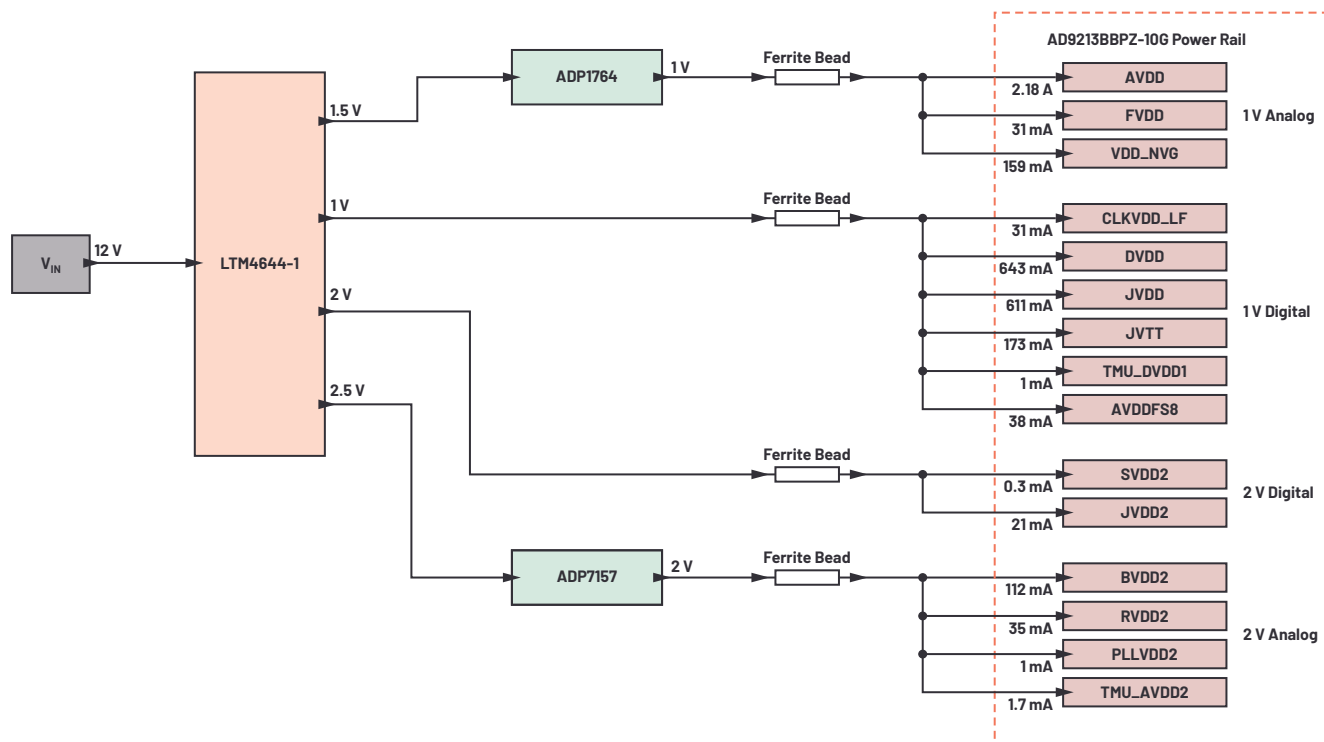- 2 V analog (two rails)
- 2 V digital (four rails)

Analysis: Noise Requirements

The optimized solution we're exploring replaces an LTM4644-1 µModule quad switcher and two linear regulators with two µModule regulators, the LTM8024 and the LTM8074, and a single LDO postregulator.

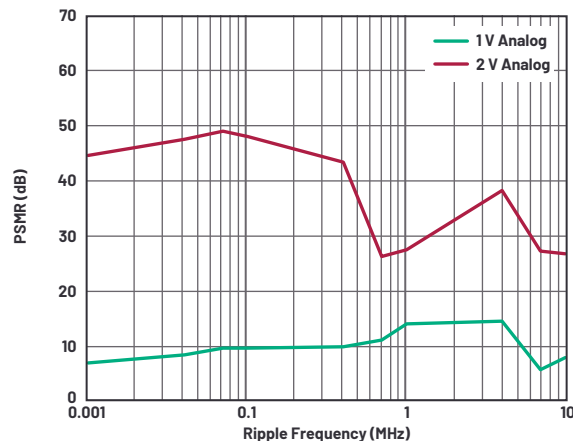Figure 8. AD9213 high speed ADC PSMR of 1 V analog and 2 V analog rails at a 2.6 GHz carrier frequency.

Figure 8 shows the PSMR results for 1 V analog and 2 V analog power rails of the AD9213 at a 2.6 GHz carrier frequency. The 1 V analog rail is more sensitive than the 2 V analog rail due to a lower PSMR.

Figure 7. Standard PDN of an AD9213 high speed ADC, which comes on the off-the-shelf evaluation board.

Figure 9 shows the spectral output of the LTM8024 (with and without an LDO regulator) in forced continuous mode (FCM). Also shown is an overlay of the maximum allowable voltage ripple threshold that will not produce spur in the –98 dBFS noise floor of the AD9213 output spectrum. The unfiltered 1/f noise and fundamental switching spur of LTM8024 output exceed the maximum allowable ripple threshold when directly powering the 1 V analog rail.

Adding an ADP1764 LDO postregulator to the LTM8024 reduces the 1/f noise and fundamental switching ripple and its harmonics down to the maximum allowable ripple threshold, which is also shown in Figure 9. Some overhead voltage is required at the input of the linear regulator. In this case, a 1.3 V output is used from the LTM8024 to the input of the postregulator. This 300 mV meets the recommended headroom voltage specification of the LDO regulator while minimizing power loss in it; this is slightly better than the 500 mV in the standard solution.
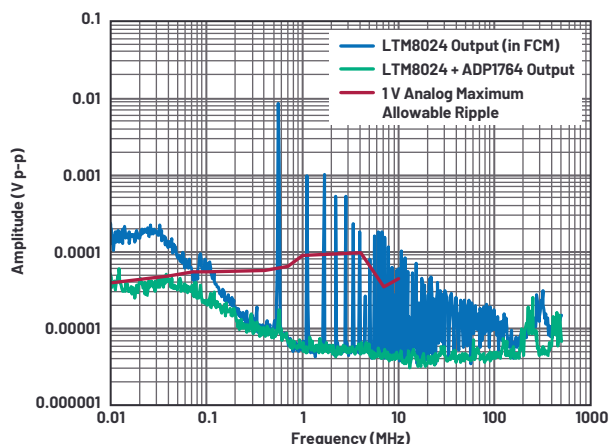

Figure 9. The LTM8024 spectral output vs. the maximum allowable ripple threshold for the 1 V analog rail.

Addressing the 2 V rails: Figure 10 shows the spectral output of the LTM8074 µModule regulator (with and without an LC filter) in FCM. The maximum allowable voltage ripple threshold is also shown. This threshold represents the power supply ripple level at which when exceeded, sideband spurs in the ADC carrier signal appear above the –98 dBFS noise floor of the AD9213 output spectrum. Here, similar to the 1 V analog rail, the regulator switching spurs exceed the maximum allowable ripple threshold when directly powering the 2 V analog rail. An LDO regulator is not required, though. Instead, an LC filter at the LTM8074 output reduces the switching spur below the maximum allowable ripple threshold.
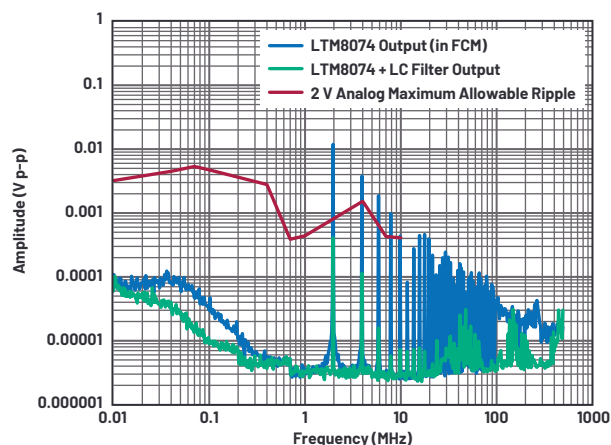

Figure 10. The LTM8074 spectral output vs. the maximum allowable ripple threshold for the 2 V analog rail.

Results: Optimized PDN

Figure 11 shows the optimized power distribution network resulting from the power supply sensitivity evaluation results. Like the standard solution, it uses three power ICs; in this case, an LTM8024, LTM8074, and ADP1764. In this solution, the LTM8024 µModule regulator V_{OUT1} is postregulated by the ADP1764 to power the relatively sensitive 1 V analog rail. The 1 V digital rail is directly powered by V_{OUT2} of LTM8024. Much like the AD9175 DAC, the AD9213's digital rails are less sensitive to power supply noise, so directly powering these rails is possible without degrading the ADC dynamic performance. The LTM8074 with LC filter powers the 2 V analog and 2 V digital rails.
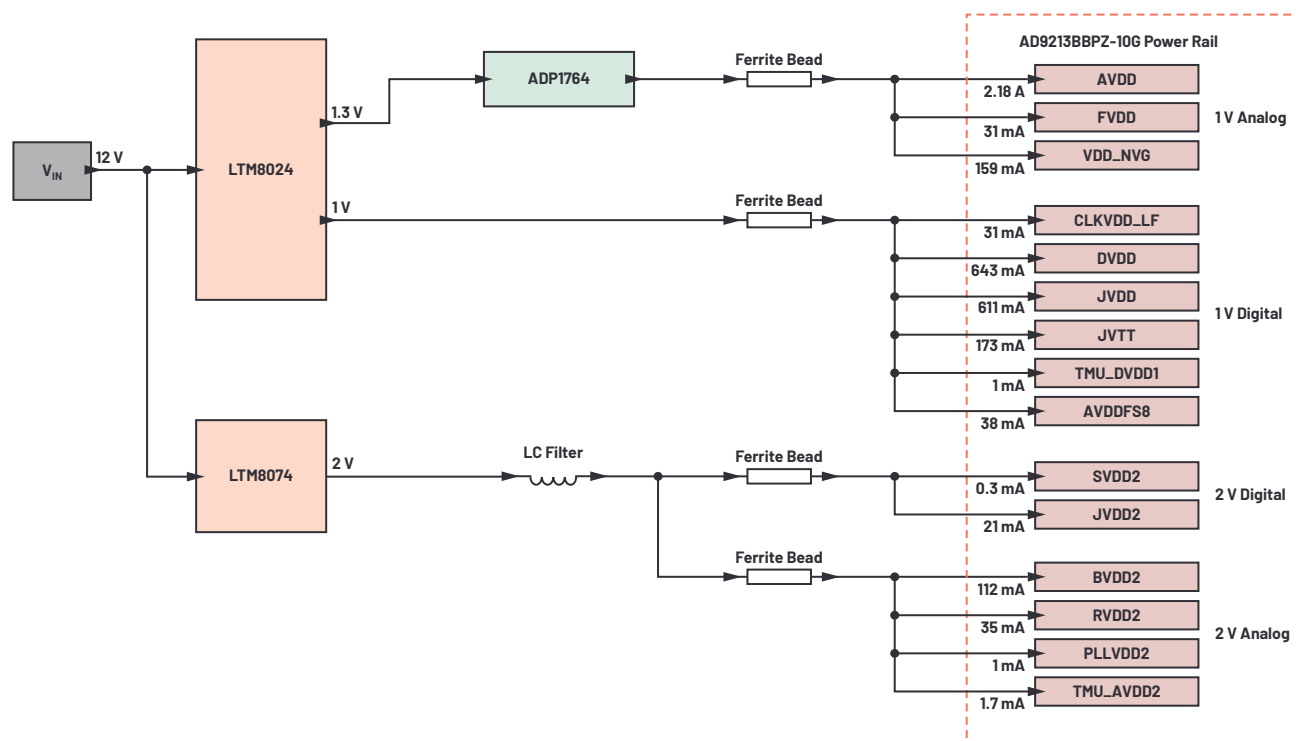

Figure 11. Optimized PDN for an AD9213 high speed ADC.

Table 3 compares the performance of the optimized PDN to the standard off-the-shelf PDN. As shown in Figure 7, the standard PDN uses a quad buck switcher with two LDO regulators. The component area reduction is 15.4% and the efficiency has increased to 73.5% (from 63.1%) with an overall power saving of 1.0 W.

Table 3. An Optimized PDN vs. a Standard PDN for the AD9213 High Speed ADC

	Standard PDN (Figure 7)	Optimized PDN (Figure 11)	Improvement of the Optimized PDN from the Standard PDN
Component Area	153.0 mm²	129.5 mm²	15.4%
Overall Efficiency	63.1%	73.5%	10.4%
Power Loss	2.5 W	1.5 W	1.0 W

To verify the performance of the optimized PDN, the AD9213 is evaluated in terms of SFDR and SNR, and by inspecting the FFT output spectrum of the sideband spurs around the carrier. The SNR and SFDR performance show results that are within data sheet specifications limits, as shown in Table 4. Figure 12 shows the FFT output spectrum of AD9213, and features a clean carrier frequency with no visible sideband spurs.

Table 4. AD9213 Dynamic Performance at 2.6 GHz Carrier Using the Optimized PDN of Figure 11

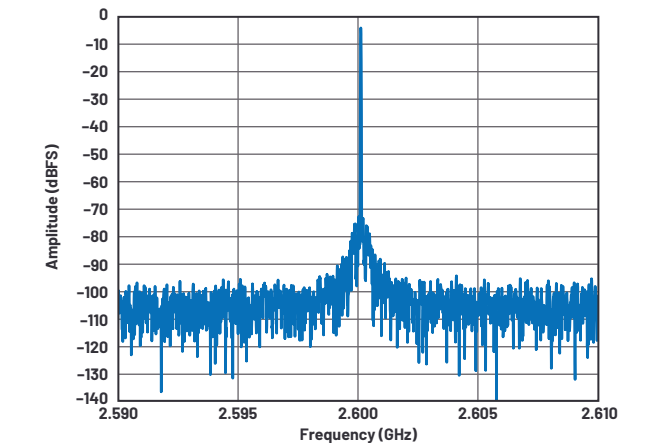| ADC Parameter	Evaluation Results	Data Sheet Specifications		
		Min	Typ	Max
SNR (dBFS)	52.6	50.1	52.3	—
SFDR (dBFS)	72.0	60.0	76.0	—

Figure 12. The FFT spectrum for the AD9213 (at 2.6 GHz, –1 dBFS carrier) using the optimized PDN of Figure 11.

Conclusion

Off-the-shelf evaluation boards for high performance data converters are set up with power distribution networks designed to meet the noise requirements of these signal processing ICs. Even with the careful considerations made in the design of the evaluation board, there is room for improvement of the power distribution networks. Here we examined two PDNs: one for a high speed DAC and one for a high speed ADC. We made improvements in space requirements, efficiency, and the especially important thermal performance over the standard PDNs. Further improvements could be made in certain parameters with alternate designs or currently unavailable devices. Stay tuned for further entries in this power system optimization series, including PDN optimization for RF transceivers.

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About the Author

Patrick Errgy Pasaquian has been at Analog Devices for seven years. He joined ADI in 2014 and works as senior applications engineer focusing on aerospace and defense (ADEF) power systems. He has handled various engineering roles in applications development, design evaluation, power attached to ADEF signal chains, and customer support through EngineerZone and Who's Who. He has authored and showcased several papers and projects at the ADI General Technical Conference (GTC), Asia Technical Symposium (ATS), and ADI Philippines Technical Symposium (ADTS). He received his bachelor's degree in electronics engineering at Central Philippine University in Iloilo City, Philippines. He can be reached at patrick.pasaquian@analog.com.

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