Vol 55, No 4—October 2021

ANALOG DEVICES
AHEAD OF WHAT'S POSSIBLE™

AnalogDialogue

# The Easy Steps to Calculate Sampling Clock Jitter for Isolated, Precision High Speed DAQs

**Lloben Paculanan**, Staff Applications Development Engineer and
**John Neeko Garlitos**, Product Applications Engineer

## Introduction

Many data acquisition (DAQ) applications require an isolated DAQ signal chain path for robustness, safety, high common-mode voltage, or to eliminate ground loops that can introduce an error into a measurement. ADI's precision, high speed technology enables system designers to achieve high AC and DC accuracy with the same design, without having to trade off DC accuracy for higher sampling rates. However, to achieve high AC performance, such as signal-to-noise ratio (SNR), the system designer needs to take into account the error introduced by jitter on the sampling clock signal or convert-start signal that controls the sample-and-hold (S&H) switch in the ADC. Jitter on the signal controlling the S&H switch becomes a more dominant error as the signal of interest and sample rates increase.

When the DAQ signal chain is isolated, the signal for controlling the S&H switch typically comes from the backplane for multichannel, synchronized sampling. It is crucial that a system designer selects a digital isolator that has low jitter so that the resultant control signal going to the ADC's S&H switch has low jitter. LVDS is the preferred interface format for precision, high speed ADCs because of the high data rate requirements. It also creates minimal disturbance on the DAQ power and ground planes. This article will explain how to interpret the jitter specifications on Analog Devices' LVDS digital isolators and which specifications are important when interfacing to precision, high speed products such as the ADAQ23875 DAQ µModule® solution. The guidance outlined in this article is applicable when using other precision, high speed ADCs with an LVDS interface. The approach for calculating the expected impact on the SNR will also be explained in the context of the ADAQ23875 when used in conjunction with the ADN4654 gigabit LVDS isolator.

## How Jitter Impacts the Sampling Process

Typically, a clock source has jitter in the time domain. Understanding how much jitter the clock source has is important when designing a DAQ system.

Figure 1 shows the typical output frequency spectrum of a nonideal oscillator with the noise power in a 1 Hz bandwidth as a function of frequency. Phase noise is defined as the ratio of the noise in a 1 Hz bandwidth at a specified frequency offset, $f_m$, to the oscillator signal amplitude at the fundamental frequency, $f_o$.

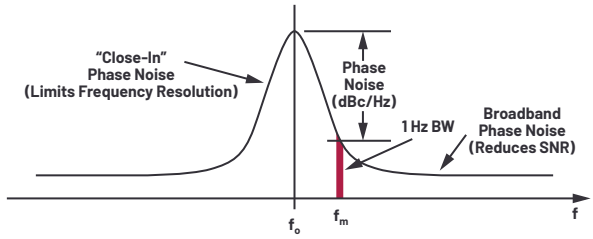


*Figure 1. Oscillator power spectrum due to phase noise.*

The sampling process is a multiplication of the sampling clock and the analog input signal. This multiplication in the time domain is equivalent to convolution in the frequency domain. Therefore, during ADC conversion, the spectrum of the ADC sampling clock is convolved with the pure sine wave input signal, and, thus, jitter on the sampling clock or phase noise will appear in the FFT spectrum of the ADC output data, as shown in Figure 2.

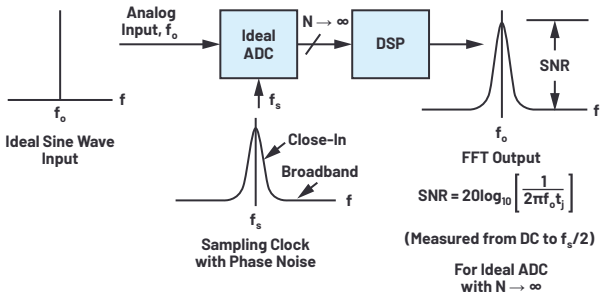


*Figure 2. The effect of sampling an ideal sine wave with a phase noise sampling clock.*

## Isolated Precision, High Speed DAQ Application

An example of an isolated precision, high speed DAQ application is a multiphase power analyzer. Figure 3 illustrates the typical system architecture with channel-to-channel isolation, and a common backplane for communication with a system compute or controller module. In this example we selected the ADAQ23875 precision, high speed DAQ solution due to its small solution footprint—making it easy to fit multiple isolated DAQ channels in a small form factor, thus reducing the weight of a mobile instrument for field testing use cases. The DAQ channel is isolated from the main chassis backplane by an LVDS gigabit isolator (ADN4654).

Isolating each of the DAQ channels enables each channel to be connected directly to sensors with significantly different common-mode voltages without damaging the input circuitry. The ground of each isolated DAQ channel tracks the common-mode voltage with a certain voltage offset. Enabling the DAQ signal chain to track the common-mode voltage associated with the sensor eliminates the need for the input signal conditioning circuitry to accommodate large input common-mode voltages and remove that high common-mode voltage for the downstream circuitry. The isolation also provides safety to the user and removes ground loops, which can impact the measurement accuracy.

Synchronizing the sampling event across all DAQ channels is crucial in a power analyzer application because mismatch in the time domain information associated with the sampled voltage will impact the follow-on calculations and analysis. To synchronize the sampling event across channels, the ADC sampling clock comes from the backplane through the LVDS isolator.

In the isolated DAQ architecture shown in Figure 3, the following jitter error sources contribute to the total jitter on the sampling clock controlling the S&H switch in the ADC.

### 1. Reference Clock Jitter

The first source of sampling clock jitter is the reference clock. This reference clock passes through the backplane to connect to each isolated precision, high speed DAQ module and other measurement modules plugged into the backplane. It serves as a timing reference for the FPGA; thus, the timing accuracy of all the events, digital blocks, PLL, etc. inside the FPGA are dependent on the reference clock's accuracy. In some applications without a backplane, an on-board clock oscillator is used as a reference clock.

### 2. FPGA Jitter

The second source of sampling clock jitter is the jitter added by the FPGA. It is important to remember that there's a trigger-to-execution path inside the FPGA, and the jitter specification of the PLL and other digital blocks inside the FPGA contribute to the overall jitter performance of the system.

### 3. LVDS Isolator Jitter

The third source of sampling clock jitter is the LVDS isolator. LVDS isolators have additive phase jitter that contributes to the overall jitter performance of the system.

### 4. ADC's Aperture Jitter

The fourth source of sampling clock jitter is the ADC's aperture jitter. This is inherent to the ADC and defined on the data sheet.

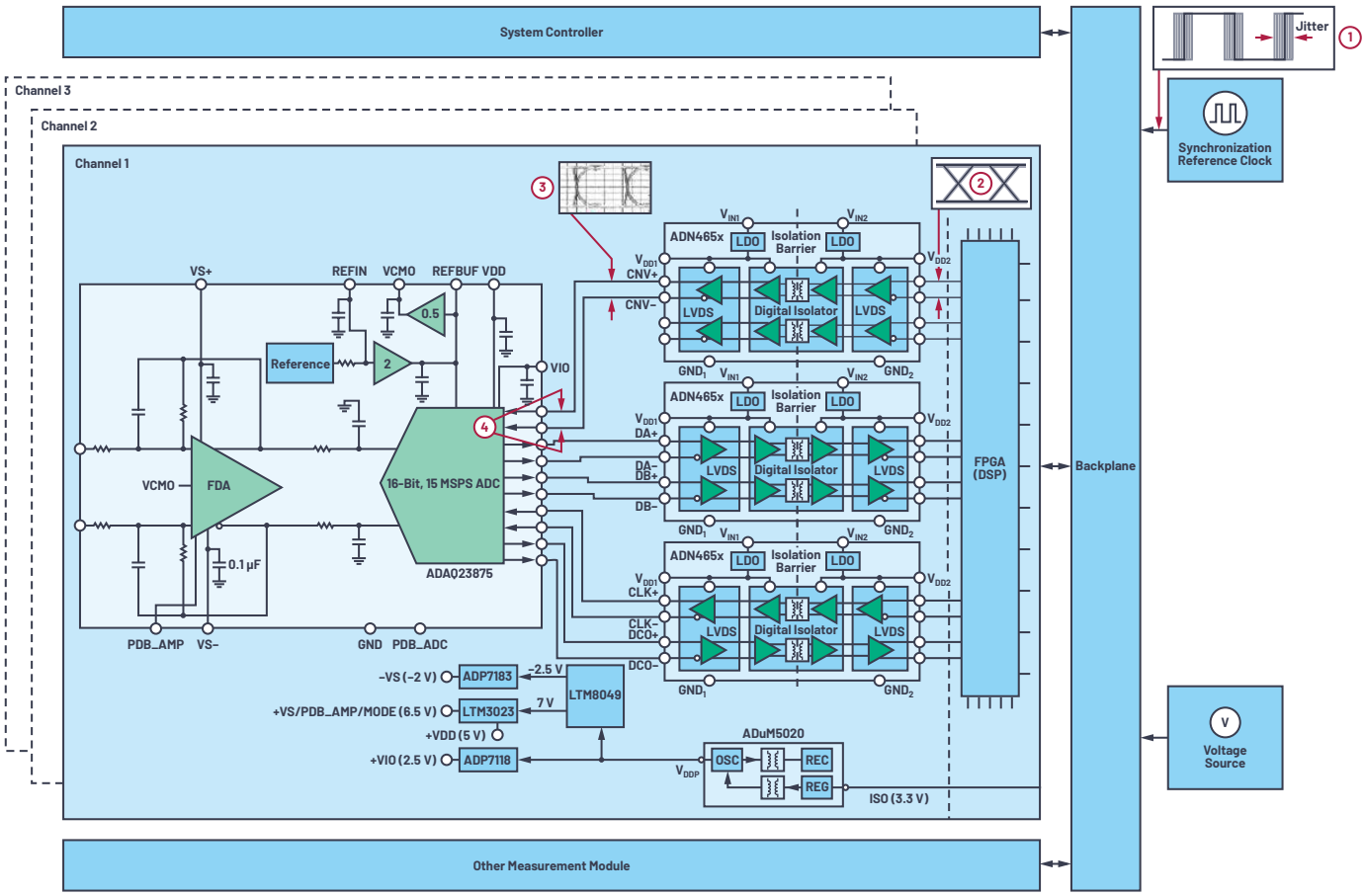


*Figure 3. Channel-to-channel, isolated DAQ architecture.*

There are reference clock and FPGA jitter specifications that are given in terms of phase noise. To calculate the jitter contribution to the sampling clock, the phase noise specification in the frequency domain needs to be converted to a jitter specification in the time domain.

## Calculating Jitter from Phase Noise

The phase noise curve is somewhat analogous to the input voltage noise spectral density of an amplifier. Like amplifier voltage noise, low 1/f corner frequencies are highly desirable in an oscillator. Oscillators are typically specified in terms of phase noise, but to relate phase noise to ADC performance, the phase noise must be converted into jitter. To make the graph in Figure 4 relevant to modern ADC applications, the oscillator frequency (sampling frequency) is chosen to be 100 MHz for discussion purposes, and a typical graph is shown in Figure 4. Notice that the phase noise curve is approximated by several individual line segments, and the endpoints of each segment are defined by data points.

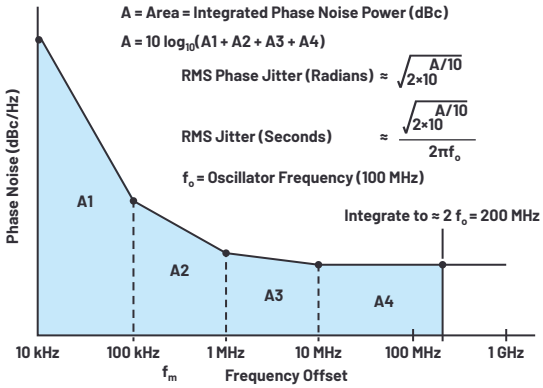


*Figure 4. Calculating jitter from phase noise.*

The first step in calculating the equivalent rms jitter is to obtain the integrated phase noise power over the frequency range of interest—that is, the area of the curve, A. The curve is broken into several individual areas (A1, A2, A3, and A4), each defined by two data points. The upper frequency range for the integration should be twice the sampling frequency, assuming there is no filtering between the oscillator and the ADC input. This approximates the bandwidth of the ADC sampling clock input. Selecting the lower frequency for the integration also requires some judgment. In theory, it should be as low as possible to get the true rms jitter. In practice, however, the oscillator specifications generally will not be given for offset frequencies less than 10 Hz or so—however, this will certainly give accurate enough results in the calculations. A lower frequency of integration of 100 Hz is reasonable in most cases if that specification is available. Otherwise, use either the 1 kHz or 10 kHz data point. One should also consider that the close-in phase noise affects the spectral resolution of the system, while the broadband noise affects the overall system SNR. Probably the wisest approach is to integrate each area separately and examine the magnitude of the jitter contribution of each area. The low frequency contributions may be negligible compared to the broadband contribution if a crystal oscillator is used. Other types of oscillators may have significant jitter contributions in the low frequency area, and a decision must be made regarding their importance to the overall system frequency resolution. The integration of each individual area yields individual power ratios. The individual power ratios are then summed and converted back into dBc. Once the integrated phase noise power is known, the rms phase jitter in radians is given by:

$$RMS\ Phase\ Jitter\ (Radians) = \sqrt{2 \times 10^{A/10}} \quad (1)$$

and dividing by $2\pi f_0$ converts the jitter in radians to jitter in seconds:

$$RMS\ Phase\ Jitter\ (Seconds) = \frac{\sqrt{2 \times 10^{\frac{A}{10}}}}{2\pi f_O} \quad (2)$$

See "MT-008 Tutorial: Converting Oscillator Phase Noise to Time Jitter" for further details.

## Quantifying the Reference Clock Jitter

The reference clock typically used in a high performance DAQ system is a crystal oscillator since it offers the best jitter performance when compared to other clock sources.

The jitter specifications of crystal oscillators are typically defined in a data sheet by the example shown in Table 1. Phase jitter is the most important specification when quantifying the jitter contribution from the reference clock. Phase jitter is usually defined as the deviation in edge location with respect to mean edge location.

**Table 1. Example Data Sheet Jitter Specification for a Crystal Oscillator**

| Symbol | Parameter | Test Condition | | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $J_{PER}$ | Period jitter, rms | LVDS | | – | XXX | – | ps |
| | | LVPECL | | – | XXX | – | |
| | | LVCMOS | $f_{OUT}$ = 125 MHz | – | XXX | – | |
| $R_J$ | Random jitter, rms | LVDS | | – | XXX | – | ps |
| | | LVPECL | | – | XXX | – | |
| | | LVCMOS | $f_{OUT}$ = 125 MHz | – | XXX | – | |
| $D_J$ | Deterministic jitter | LVDS | | – | XXX | – | ps |
| | | LVPECL | | – | XXX | – | |
| | | LVCMOS | $f_{OUT}$ = 125 MHz | – | XXX | – | |
| $T_J$ | Total jitter | LVDS | | – | XXX | – | ps |
| | | LVPECL | | – | XXX | – | |
| | | LVCMOS | $f_{OUT}$ = 125 MHz | – | XXX | – | |
| $f_{JITTER}$ | Phase jitter (12 kHz to 20 MHz) | LVDS | | – | XXX | – | fs |
| | | LVPECL | | – | XXX | – | |
| | | LVCMOS | $f_{OUT}$ = 125 MHz | – | XXX | – | |

On the other hand, there are some crystal oscillators that specify the phase noise performance instead of jitter. If the oscillator data sheet defines the phase noise performance, it can be converted to jitter as discussed in the "Calculating Jitter from Phase Noise" section.

## Quantifying the Jitter from the FPGA

The main role of the reference clock in an FPGA is to provide a trigger signal to start different parallel events programmed inside the FPGA. In other words, the reference clock orchestrates all the events inside the FPGA. To provide a better time resolution of the timing, the reference clock is usually passed to a PLL inside the FPGA to increase its frequency—thus, small time interval events will be possible. It is also important to know that there is a trigger-to-execution path inside the FPGA where the reference clock is passed to clock buffers, counters, logic gates, etc. When handling jitter sensitive repetitious events—such as providing an LVDS convert-start signal to an ADC via isolation—it is important to quantify the jitter contribution from the FPGA to properly estimate the impact on the overall system jitter to the high speed data acquisition performance.

The jitter performance of the FPGA is usually defined on the FPGA data sheet. It can also be found in the static timing analysis (STA) of most FPGA software tools, as shown in Figure 5. The timing analysis tool can calculate the clock uncertainty from the source and destination of a datapath and combine them together to form the total clock uncertainty. In order to automatically compute the contribution of the reference clock jitter in the STA, it must be added as **Input Jitter Constraint** in the FPGA project.

```
Paths for end point sar_adc_capture/input_shift_reg_4 (SLICE_X13Y24.AX), 1 path
--------------------------------------------------------------------------------
Slack (setup path):     8.362ns (requirement - (data path - clock path skew + uncertainty))
  Source:               sar_adc_capture/input_shift_reg_3 (FF)
  Destination:          sar_adc_capture/input_shift_reg_4 (FF)
  Requirement:          10.000ns
  Data Path Delay:      1.448ns (Levels of Logic = 0)
  Clock Path Skew:      -0.155ns (0.679 - 0.834)
  Source Clock:         sar_spi_clk_delay falling at 5.000ns
  Destination Clock:    sar_spi_clk_delay falling at 15.000ns
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: sar_adc_capture/input_shift_reg_3 to sar_adc_capture/input_shift_reg_4
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X11Y26.DQ      Tcko                  0.391   sar_adc_capture/input_shift_reg<3>
                                                       sar_adc_capture/input_shift_reg_3
    SLICE_X13Y24.AX      net (fanout=2)        0.994   sar_adc_capture/input_shift_reg<3>
    SLICE_X13Y24.CLK     Tdick                 0.063   sar_adc_capture/input_shift_reg<7>
                                                       sar_adc_capture/input_shift_reg_4
    -------------------------------------------------  -------------------
    Total                                      1.448ns (0.454ns logic, 0.994ns route)
                                                       (31.4% logic, 68.6% route)

--------------------------------------------------------------------------------
```

*Figure 5. A static timing analysis (STA) example view.*

## Quantifying the Jitter from Digital Isolation

The most basic method of viewing jitter is to measure an LVDS signal pair with a differential probe and trigger on both rising and falling edges, with the oscilloscope set to infinite persistence. This means that high-to-low and low-to-high transitions are superimposed, allowing measurement of the crossover point. The width of the crossover corresponds to the peak-to-peak jitter or time interval error (TIE) measured so far. Compare the eye diagram and histogram shown in Figure 6 and Figure 7. Some jitter is due to random sources (for example, thermal noise), and this random jitter (RJ) means that the peak-to-peak jitter seen on the oscilloscope is limited by the run time (the tails on the histogram will grow as the run time increases).

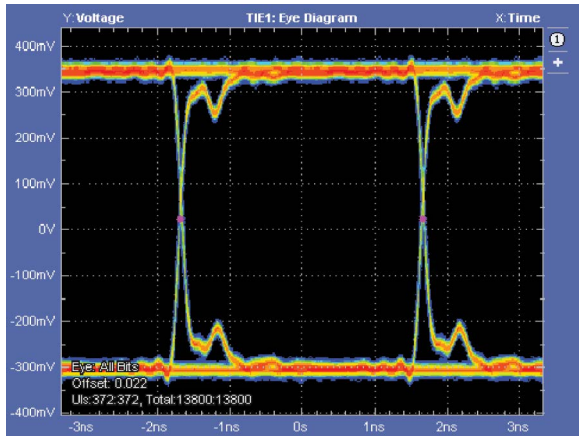


*Figure 6. Eye diagram for ADN4651.*

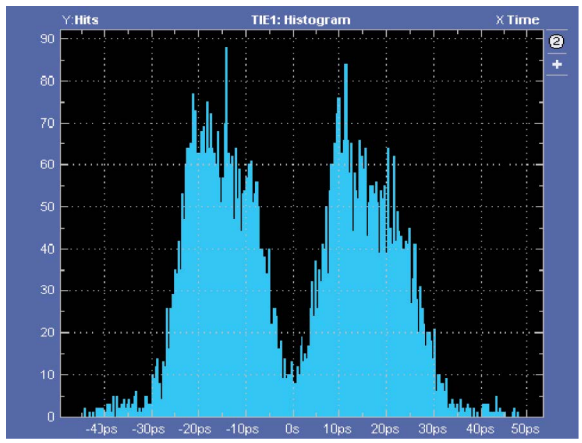


*Figure 7. Eye diagram histogram for ADN4651.*

By contrast, sources of deterministic jitter (DJ) are bounded, such as jitter due to pulse skew, data dependent jitter (DDJ), and intersymbol interference (ISI). Pulse skew arises due to a difference between high-to-low and low-to-high propagation delays. This is visualized by an offset crossover such that at 0 V, the two edges are separated (easily seen by the separation in the histogram in Figure 7). DDJ arises from a difference in propagation delay across operating frequency, while ISI is due to the influence of previous transition frequencies on the current transition (for example, edge timing will typically be different after a train of 1s or 0s vs. a 1010 pattern).

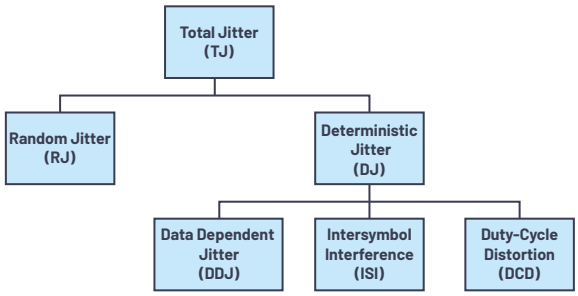


*Figure 8. Total jitter contribution.*

Figure 8 shows how to fully estimate the total jitter for a given bit error rate (TJ@BER). RJ and DJ can be calculated based on model-fitting to a TIE distribution from measurement. One such model is the dual-Dirac model, which assumes a Gaussian random distribution convolved with a dual-Dirac delta function (the separation between the two Dirac delta functions corresponding to the DJ). For TIE distributions with significant deterministic jitter, the distribution will visually approximate this model. One complication is that some DJ can contribute to the Gaussian component, meaning that the dual-Dirac model can underestimate DJ and overestimate RJ. However, the two combined will still allow an accurate estimate of the total jitter for a given BER.

RJ is specified as a 1 sigma rms value from the modeled Gaussian distribution, meaning that to extrapolate to longer run lengths (low BERs), one simply chooses the appropriate multiple sigma to move far enough along the tails of the distribution (for example, 14 sigma for $1 \times 10^{-12}$ bit errors). DJ is then added to provide the TJ@BER estimate. For multiple elements in a signal chain—rather than adding multiple TJ values, which will overestimate jitter—RJ values can be geometrically summed and DJ values algebraically summed, allowing a more reasonably complete TJ@BER estimate for a complete signal chain.

RJ, DJ, and TJ@BER are all specified separately for the ADN4654, with maximums provided for each based on statistical analysis of multiple units to guarantee these jitter values across power supply, temperature, and process.

Figure 9 illustrates an example of the jitter specification for the ADN4654 LVDS isolator. In the case of an isolated DAQ signal chain, additive phase jitter is the most important jitter specification. The additive phase jitter, together with other jitter sources, adds to the ADC's aperture jitter that causes sample time imprecision.

| Parameter | Symbol | Min | Typ | Max[1] | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|---|
| JITTER[5] | | | | | | See Figure 39, for any $D_{OUTx+}/D_{OUTx-}$ |
| Random Jitter, RMS[6] (1σ) | $t_{RJ(RMS)}$ | | 2.6 | 4.8 | ps rms | 0.55 GHz clock input |
| Deterministic Jitter, Peak to Peak[7,8] | $t_{DJ(PP)}$ | | 50 | 116 | ps | 1.1 Gbps, $2^{23} - 1$ pseudorandom bit stream (PRBS) |
| With Crosstalk | $t_{DJC(PP)}$ | | 50 | | ps | 1.1 Gbps, $2^{23} - 1$ PRBS |
| Total Jitter at Bit Error Rate (BER) $1 \times 10^{-12}$ | $t_{TJ(PP)}$ | | 90 | 171 | ps | 0.55 GHz, 1.1 Gbps, $2^{23} - 1$ PRBS[9] |
| Additive Phase Jitter | $t_{ADDJ}$ | | 387 | | fs rms | 100 Hz to 100 kHz, output frequency ($f_{OUT}$) = 10 MHz[10] |
| | | | 288 | | fs rms | 12 kHz to 20 MHz, $f_{OUT}$ = 0.55 GHz[11] |

*Figure 9. ADN4654 jitter specification.*

## Quantifying the ADC's Aperture Jitter

Aperture jitter is inherent within the ADC. It is due to the sample-to-sample variation in aperture delay, which corresponds to an error voltage in the sampling event. This sample-to-sample variation in the instant the switch opens is called aperture uncertainty, or aperture jitter, and usually measured in rms picoseconds.

In an ADC, as shown in Figure 10 and 11, the aperture delay time is referenced to the input of the converter; the effects of the analog propagation delay through the input buffer, $t_a$; and the digital delay through the switch driver, $t_{dd}$. Referenced to the ADC inputs, aperture time, $t_a'$, is defined as the time difference between the analog propagation delay of the front-end buffer, $t_{da}$, and the switch driver digital delay, $t_{dd}$, plus one-half the aperture time, $t_a/2$.

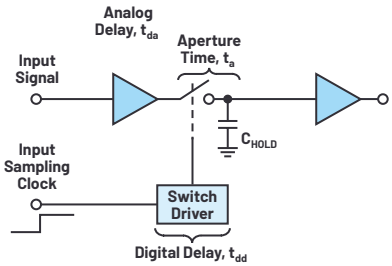


*Figure 10. ADC's sample-and-hold input stage.*

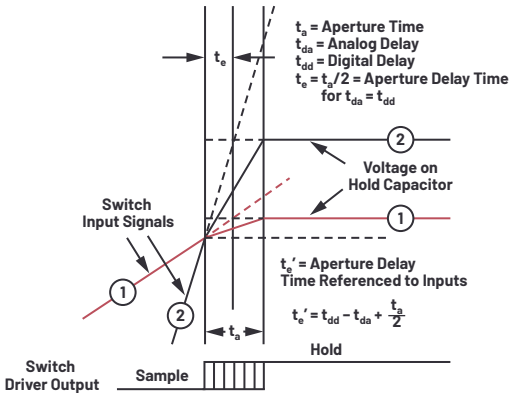


*Figure 11. Sample-and-hold waveforms and definitions.*

In the case of the ADAQ23875, the aperture jitter is only around 0.25 $ps_{RMS}$ as shown in Figure 12. This specification is guaranteed by design and not subject to test.

ADAQ23875 Data Sheet

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit[3] |
|---|---|---|---|---|---|
| Aperture Delay[9] | | | 0 | | ns |
| Aperture Jitter[9] | | | 0.25 | | $ps_{RMS}$ |

*Figure 12. ADAQ23875 aperture jitter.*

## Overall Sampling Clock Jitter

After quantifying the individual jitter contribution of the four major blocks shown in Figure 3, the overall jitter performance of the signal (or clock) controlling the S&H switch can be calculated by taking the root sum of squares (RSS) of the four jitter sources.

$$Sampling\ Clock_{Jitter} = \sqrt{\begin{matrix}(Reference\ Clock_{Jitter})^2 + (FPGA_{Jitter})^2 \\ + (Isolator_{Jitter})^2 + (ADC's_{Jitter})^2\end{matrix}} \quad (3)$$

On the other hand, if STA was used, the simplified clock jitter equation would be:

$$Sampling\ Clock_{Jitter} = \sqrt{\begin{matrix}(STA_{Jitter})^2 + (Isolator_{Jitter})^2 \\ + (ADC's_{Jitter})^2\end{matrix}} \quad (4)$$

## Effects of Sampling Clock Jitter on SNR

Having quantified the overall jitter on the signal controlling the S&H switch, we can now quantify how much that jitter will impact the SNR performance of the DAQ signal chain.

Figure 13 illustrates the error due to jitter on the sampling clock.

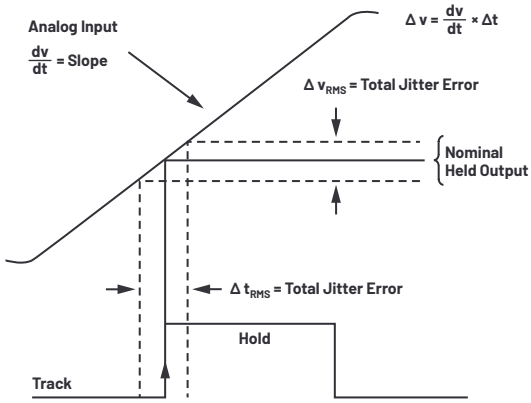


*Figure 13. The effects of sampling clock jitter.*

The effects of sampling clock jitter on an ideal ADC's SNR can be predicted by the following simple analysis.

Assume an input signal given by:

$$v(t) = V_o \sin(2\pi ft) \quad (5)$$

The rate of change of this signal is given by:

$$\frac{dv}{dt} = 2\pi f V_o \cos(2\pi ft) \quad (6)$$

The rms value of dv/dt can be obtained by dividing the amplitude, $2\pi fV_0$, by $\sqrt{2}$.

Now let $\Delta V_{rms}$ = the rms voltage error and $\Delta t$ = the rms aperture jitter $t_j$, and substitute these $\left.\frac{dv}{dt}\right|_{rms} = \frac{2\pi f V_o}{\sqrt{2}}$ values:

$$\frac{\Delta V_{rms}}{t_j} = \frac{2\pi f V_o}{\sqrt{2}} \quad (7)$$

And solving for $\Delta V_{rms}$:

$$\Delta V_{rms} = \frac{2\pi f V_o t_j}{\sqrt{2}} \quad (8)$$

The rms value of the full-scale input sine wave is $V_0/\sqrt{2}$. Therefore, the rms signal to rms noise ratio (expressed in dB) is given by frequencies:

$$SNR = 20\log_{10}\left[\frac{V_o/\sqrt{2}}{\Delta V_{rms}}\right] = 20\log_{10}\left[\frac{V_o/\sqrt{2}}{2\pi f V_o t_j/\sqrt{2}}\right] = 20\log_{10}\left[\frac{1}{2\pi f t_j}\right] \quad (9)$$

This equation assumes an infinite resolution ADC where aperture jitter is the only factor in determining the SNR. This equation is plotted in Figure 14 and shows the serious effects of aperture and sampling clock jitter on SNR and ENOB, especially at higher input/output.

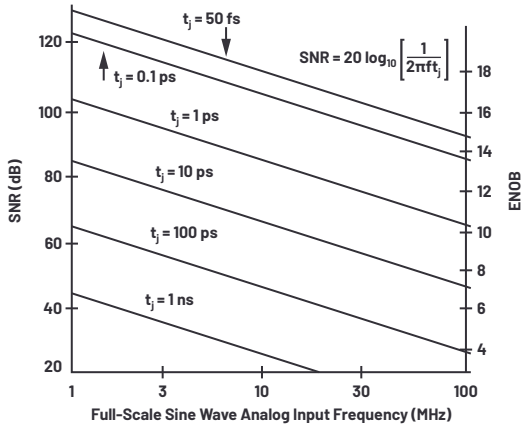


*Figure 14. Theoretical data converter SNR and ENOB due to jitter vs. full-scale sine wave input frequency.*

## ADAQ23875 and ADN4654 Sampling Clock Jitter Ideal SNR Calculation

The ADAQ23875 has an aperture jitter of 250 fs rms (typical), while the ADN4654 has an additive phase jitter of 387 fs rms ($f_{OUT}$ = 1 MHz). In this case, we'll not yet consider the jitter contribution of the reference clock and of the FPGA.

Now, from the jitter specification of our ADC and isolator we can calculate the total rms jitter by:

$$J_{TOTAL} = \sqrt{(387\text{ fs})^2 + (250\text{ fs})^2} = 460.72\text{ fs rms} \quad (10)$$

Figures 14 and 15 illustrate the calculated maximum SNR and ENOB performance of the isolated precision, high speed DAQ system. The SNR and ENOB degrade along with input frequency, which aligns with the profile in the theoretical SNR plot in Figure 13.

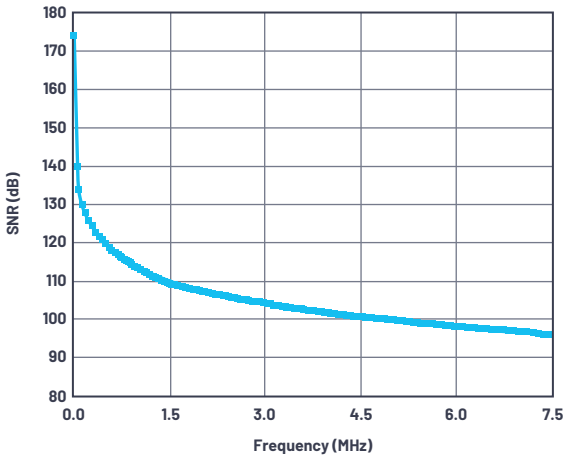


*Figure 15. ADAQ23875 and ADN4654 maximum calculated SNR.*

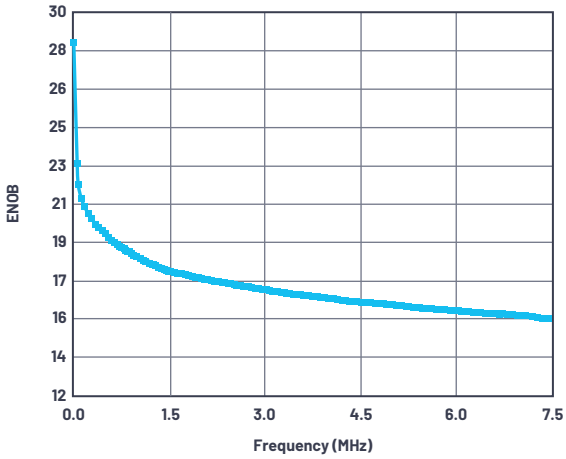


*Figure 16. ADAQ23875 and ADN4654 maximum calculated ENOB.*

## Conclusion

Jitter in the signal (or clock) controlling the S&H switch in an ADC impacts the SNR performance of precision, high speed DAQ signal chains. Understanding the error sources that contribute to the overall jitter is important when selecting the various components that are part of the clock signal chain.

When the application requires the DAQ signal chain to be isolated from the backplane, selecting a digital isolator that has a low additive jitter is crucial to maintaining optimum SNR performance. ADI has lower jitter LVDS isolators that enable system-level designers to achieve high SNR performance in an isolated signal chain architecture.

The reference clock is the first source of sampling clock jitter, and it is important to use a low jitter reference clock to achieve the best performance of an isolated, high speed DAQ. It is also important to ensure the signal integrity of the path between the FPGA and reference clock to avoid additional error from the path itself.

## Acknowledgements

The authors would like to thank Michael Hennessy and Stuart Servis for their technical contributions to this article.

## References

Boser, B. E., and B. A. Wooley. "The Design of Sigma-Delta Modulation Analog-to-Digital Converters." *IEEE Journal of Solid-State Circuits*, Vol. 23, No. 6, December 1988.

Harris, Steven. "The Effects of Sampling Clock Jitter on Nyquist Sampling Analog-to-Digital Converters, and on Oversampling Delta-Sigma ADCs." *Journal of the Audio Engineering Society*, Vol. 38, No. 7/8, July/August 1990.

Kester, Walt. "MT-007 Tutorial: Aperture Time, Aperture Jitter, Aperture Delay Time—Removing the Confusion." Analog Devices, Inc., 2008.

Kester, Walt. "MT-008 Tutorial: Converting Oscillator Phase Noise to Time Jitter." Analog Devices, Inc., 2009.

Redmayne, Derek, Eric Trelewicz, and Alison Smith. "Understanding the Effect of Clock Jitter on High Speed ADCs." Analog Devices, Inc., 2006.

## About the Author

Lloben Paculanan is a product applications engineer at Analog Devices in GT, Philippines. He joined Analog Devices in 2000 where he worked in various test hardware development and applications engineering roles. He has been working on precision, high speed signal chain µModule development. He graduated from Ateneo de Cagayan Xavier University with a bachelor's degree in industrial engineering technology and from Enverga University with a bachelor's degree in computer engineering. He can be reached at lloben.paculanan@analog.com.

## About the Author

John Neeko Garlitos is a product applications engineer for signal chain µModule solutions at Analog Devices. He works on signal chain µModule development, as well as embedded software for Circuits from the Lab and reference circuits. He started working at Analog Devices in 2017 in GT, Philippines. He received his B.Sc. in electronics engineering from Technological University of the Philippines – Visayas, and M.Eng. in electrical engineering from University of the Philippines Diliman. He can be reached at johnneeko.garlitos@analog.com.