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How to Effectively Compare the Performance of CMOS Switches with Solid-State Relays

Stephen Nugent, Product Applications Engineer

Abstract

Off capacitance between the source and drain, $C_{DS(OFF)}$, is a measure of the ability of an off switch to block a signal on the source from coupling to the drain. It is a common specification seen in solid-state relays (also known as PhotoMOS®, OptoMOS®, photorelays, or MOSFET relays), and it is often referred to as output capacitance, C_{OUT}, in solid-state relay data sheets. CMOS switches do not usually include this specification, but the off-isolation spec is a different method to characterize the same phenomenon—that is, the amount of a signal that is presented to the source of an off switch that couples to the drain. This article will discuss how to derive C_{OUT} from off isolation and how this can be used to compare the performance of solid-state relays and CMOS switches more effectively. This is important as CMOS switches are a fit for many applications where solid-state relays are used, such as switching DC and high speed AC signals.

How to Derive $C_{DS(OFF)}$ from Off Isolation

Figure 1 shows the off isolation vs. frequency typical performance plot of the ADG5412. This plot shows that as the frequency of the signal on the source increases, the off isolation decreases.

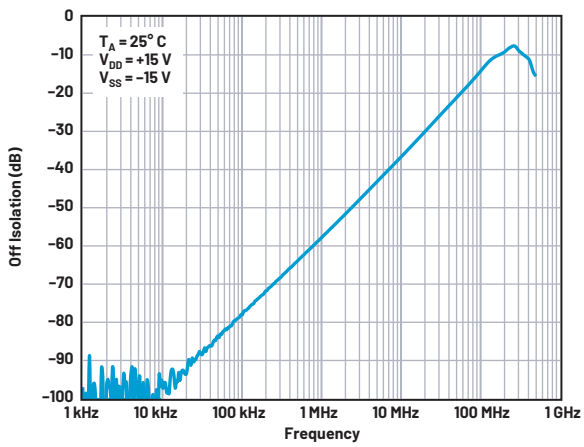

Figure 1. ADG5412 off isolation vs. frequency, ±15 V dual supply.

This means that more of the signal present on the source will appear on the drain of an off switch as the frequency of the signal increases. This is not surprising when you investigate the equivalent circuit for a switch in the off condition, as shown by the test circuit in Figure 2. When a switch is open there is a parasitic capacitance between source and drain, shown as $C_{DS(OFF)}$ in the figure. This parasitic capacitance enables high frequency signals to pass, and to characterize this is the purpose of the off-isolation plot.

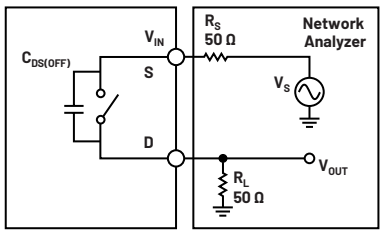

Figure 2. Off-isolation measurement test circuit.

Off isolation is calculated by taking V_S and V_{OUT} from the Figure 2 test circuit and inserting them into the following equation:

$$Off\ Isolation = 20 \log_{10} \frac{V_{OUT}}{V_S}$$

Using the results of the off-isolation plot combined with the equivalent circuit of an open switch, $C_{DS(OFF)}$ can be calculated in a CMOS switch. First if we consider the off-switch channel and the load we can equivalate the circuit to a high-pass filter, as shown in Figure 3.

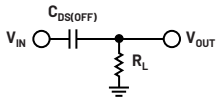

Figure 3. $C_{DS(OFF)}$ and R_L high-pass filter.

The transfer function of the circuit shown can then by derived by:

$$\frac{V_{OUT}(s)}{V_{IN}(s)} = \frac{R_L}{R_L + \frac{1}{C_{DS(OFF)}s}} = \frac{R_L C_{DS(OFF)}s}{1 + R_L C_{DS(OFF)}s}$$

Next is to consider the source voltage, V_S, and its impedance from Figure 2. The source impedance, R_S, is 50 Ω and this matches the load impedance, R_L, of 50 Ω. If we assume the ideal case where $C_{DS(OFF)}$ is a short circuit, then V_S is double V_{IN}, as the impedances are equal. This means when the transfer function is calculated in relation to V_S, the overall transfer function is doubled.

Therefore, the transfer function of the whole system is:

$$H(s) = \frac{V_{OUT}(s)}{V_S(s)} = \frac{2R_L C_{DS(OFF)}s}{1 + R_L C_{DS(OFF)}s}$$

This transfer function can then be substituted into the off-isolation equation to give:

$$Off_{iso} = 20 \log_{10}\left(\frac{2R_L C_{DS(OFF)}s}{1 + R_L C_{DS(OFF)}s}\right)$$

$$= 20 \log_{10}\left(\frac{2j2\pi f R_L C_{DS(OFF)}}{1 + j2\pi f R_L C_{DS(OFF)}}\right) \text{ as } s = j2\pi f$$

This equation can then be rearranged to make $C_{DS(OFF)}$ the subject:

$$C_{DS(OFF)} = \frac{1}{2\pi f R_L\left(\frac{2}{10^{\,offiso/20}} - 1\right)}$$

This means that if we know R_L, the frequency of the input signal, f, and the off-isolation specification value in dB, the $C_{DS(OFF)}$ can be calculated. These values can be found in the data sheet of switch or multiplexer products in the Analog Devices portfolio. The following example will outline how it can be done.

$C_{DS(OFF)}$ Calculation Example

The SPI controlled, quad SPST switch, the ADGS1612, will be used in this example. The off-isolation specification of the ADGS1612 is −65 dB, and this can be read from Table 1 of the data sheet. From the test conditions section of the off-isolation specification, R_L is given as 50 Ω and the signal frequency, f, is stated as 100 kHz. By putting these values into the $C_{DS(OFF)}$ equation, the capacitance value can be calculated.

$$C_{DS(OFF)} = \frac{1}{2\pi f R_L\left(\frac{2}{10^{\,offiso/20}} - 1\right)}$$

$$= \frac{1}{2\pi(100 \times 10^3)(50)\left(\frac{2}{10^{-65/20}} - 1\right)} \approx 9 \text{ pF}$$

Note, the measurement circuit for off isolation for switches and multiplexers may contain an additional 50 Ω termination before the source pin of the switch channel, as shown in Figure 4. The $C_{DS(OFF)}$ equation can still be used with off-isolation specifications that were measured in this way. However, 6 dB has to be added to the off-isolation specification from the data sheet when a 50 Ω termination was used at the source pin before using it in the $C_{DS(OFF)}$ equation. This is to compensate for the fact that the 50 Ω termination at the source decreases the voltage by half, which is equivalent to −6 dB.

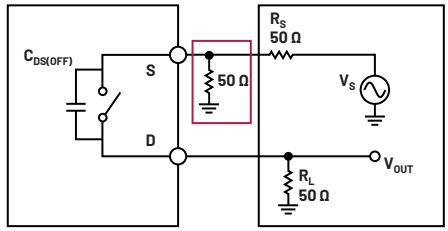

Figure 4. Off-isolation test circuit with a 50 Ω termination on the source.

CMOS Switches vs. Solid-State Relays

Table 1 shows the $C_{DS(OFF)}$ values for a selection of switch products in the Analog Devices portfolio. The ADG54xx and ADG52xx families can handle signal voltages with up to a 44 V swing, while the ADG14xx and ADG12xx families can pass signal voltages with up to a 33 V swing. This comparable signal ranges to 30 V and 40 V solid-state relays. The last column on the table also shows how the $C_{DS(OFF)}$ can be used in conjunction with the switch on resistance to calculate the R_{ON}, $C_{DS(OFF)}$ product, which is used as an order of merit in solid-state relays. The R_{ON}, $C_{DS(OFF)}$ product indicates how little a switch will attenuate a signal when it is on and combined with how well a switch can block high speed signals when the switch is off. The table shows that the ADG1412 has an R_{ON}, C_{OFF} product of less than 5, which is extremely competitive to solid-state relays on the market.

Table 1. $C_{DS(OFF)}$ for a Selection of SPST × 4 Switches in the Analog Devices Portfolio

	Max Supply Voltage	Off Isolation	$C_{DS(OFF)}$	On Resistance	R × C
ADG5412	±22 V, +40 V	−78 dB @ 100 kHz	4 pF	9.8 Ω	39.2
ADG5212	±22 V, +40 V	−80 dB @ 1 MHz	0.32 pF	160 Ω	51.2
ADG1412	±16.5 V, +16.5 V	−80 dB @ 100 kHz	3.2 pF	1.5 Ω	4.8
ADG1212	±16.5 V, +16.5 V	−80 dB @ 1 MHz	0.32 pF	120 Ω	38.4

There are also many advantages of CMOS switches compared to solid-state relays. These include:

- Easier to Drive Switch Logic

The typical digital input current for most Analog Devices' CMOS switches is 1 nA, while the recommended forward current for the diode in solid-state relays is 5 mA. This means that CMOS switches can be easily controlled directly by the GPIOs on microcontrollers.

- Faster Switching Speeds

The ADG1412 has a typical turn-on time of 100 ns compared to solid-state relays, which have turn-on times in the region of hundreds of milliseconds.

- More Switches per Package

For example, the ADGS1414D has eight switch channels with 1.5 Ω on resistance and 5 pF $C_{DS(OFF)}$ in a 5 mm × 4 mm package. That is one switch per 2.5 mm^2 of package area.

Conclusion

The ability of a switch to block signals when in the off state is key. In solid-state relays, the C_{OFF} specification is a measure of the capacitance across the switch, which allows the coupling of signals from the input to the output of the closed switch. In CMOS switches this capacitor is not directly measured; however, the effect of this capacitor is measured through the off-isolation specification. The off-isolation value in dB, the frequency of the input signal, and the load resistance can be used to determine the $C_{DS(OFF)}$ by deriving the transfer function of an open switch. The $C_{DS(OFF)}$ is important in comparing CMOS switches to the C_{OUT} specification of solid-state relays. Furthermore, $C_{DS(OFF)}$ can also be used to calculate the R_{ON}, $C_{DS(OFF)}$ product, which is an order of merit that is used to show the overall off isolation and signal lost performance of a switch. This allows for direct competition between CMOS switches and solid-state relays when selecting a switch for an application. CMOS switches also have many benefits over solid-state relays—namely, easier to drive switch logic, faster switching speeds, and the ability to have more switches in a package.

About the Author

Stephen Nugent is an applications engineer in the Automatic Test Equipment Group at Analog Devices. He graduated from Queen's University Belfast in 2014 with a master's degree in electrical and electronic engineering. Stephen joined Analog Devices in 2014 supporting the analog switch and multiplexer product portfolio. He can be reached at stephen.nugent@analog.com.