Vol 56, No 4—December 2022

ANALOG DEVICES
AHEAD OF WHAT'S POSSIBLE™

AnalogDialogue

Power Optimization Techniques for Low Power Signal Chain Applications

Lluis Beltran Gil, Product Applications Engineer

Abstract

This article presents precision low power signal chain solutions and techniques for attaining optimized power efficiency in low power signal chain applications. It will explain techniques (beyond selecting low power products, which isn't always sufficient) such as power scaling, power cycling, and duty cycling to further reduce system power consumption. It will also discuss how to use on-chip features such as channel sequencers, FIFOs, and voltage monitoring blocks that reduce the system design complexity and enable power savings in the host controller side and at the overall system level.

Introduction

To keep going and going was an obsession for that little drum playing bunny in the advertisements decades ago. When designing a battery-powered measurement system for applications such as field instruments (sensing temperature, pressure, or flow) or remote vital sign monitoring devices, low power signal chains are critical. Even for mains powered systems, minimizing the environmental impact or the energy costs pushes hardware designers to improve system power efficiency. A low power design may have indirect benefits like a smaller solution size, if enabling to reduce the number of battery cells in parallel. A further advantage to the low power design is the lower IC die temperature due to the lower energy the system consumes. This extends product lifetimes.

Precision low power signal chains are a great starting point for getting a low power hardware design done in a short time. Beyond choosing low power components, several power optimization techniques such as power scaling, power cycling, and duty cycling can be implemented to further reduce the system power consumption. Also, design choices like appropriate resistor values or the use of memories can be a great differentiator for achieving stringent low power targets and optimal battery life.

For example, identifying building blocks in the signal chain that can be eliminated or powered down momentarily when certain conditions are met makes it possible to implement low power techniques. This will require a good timing analysis[1,2] and staging

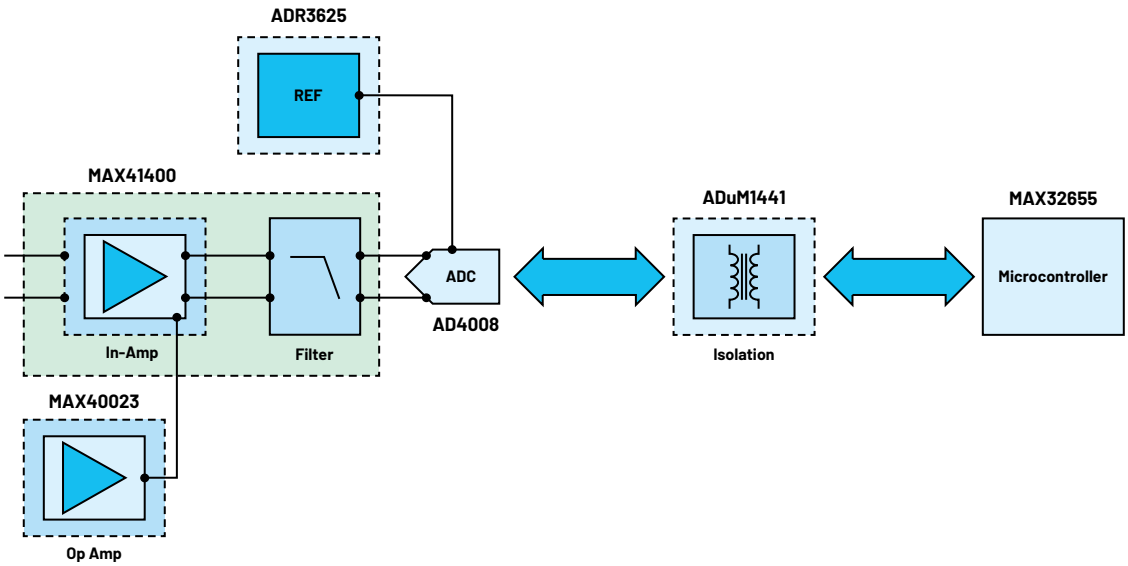

Figure 1. Single-channel voltage, current measurement in SAR ADC signal chain.

or duty cycling the operation. If several building blocks are idling for the greatest portion of the time, then these can be placed into shutdown mode or directly switched off. Note that fully power cycling a device will have some implications in terms of power and timing, compared to using shutdown modes when available.

Once this timing is properly implemented, major system-level power consumption improvements can be achieved even further by minimizing the microcontroller interaction. This will require the use of memories, either external or internal, that can store data while the host controller is shut down.

There are some differences on how to apply power saving techniques at the system level, depending on the type of ADC used for digitizing the sensor information, among SAR and sigma-delta, as detailed in the following sections. Also, hardware design decisions like digital comms pull-up/pull-down resistors, resistive dividers, and gain setting resistors will make a difference on the overall signal chain power consumption.

Pin naming may vary from device to device. For consistency, we will refer to AV_{DD} for analog supply, V_{IO} for digital supply, and V_{REF} for reference voltage.

Power Optimization on a SAR ADC-Based Signal Chain

SAR ADCs perform conversions on demand—that is, they toggle from sample mode to hold mode[3] after assertion of the CONVERSION START command. The conversion process starts and, once completed, it toggles back to sample mode in order to acquire the signal. SAR ADCs like the AD4008 converter used in the signal chain shown in Figure 1 consume most of the power during the conversion phase, whereas consumption is minimal during the acquisition phase as shown in Figure 2. So, despite being capable of throughputs as high as a few MSPS, power can be greatly optimized by running these converters at the minimum speed required by the application.

SAR ADC: Power Scaling with Throughput

In many low power applications, sensor information is not needed continuously but at much lower rates, in the order of kSPS or tens of kSPS. In these cases, power consumption of the SAR ADC can be scaled down with throughput, both for analog and digital supply rails.

Table 1. Common Sampling Frequencies at Different End Applications

Application	Common Sampling Frequency
Field Instruments	60 SPS to 600 SPS
Condition-Based Monitoring	1 kSPS to 10 kSPS
Vital Sign Monitoring	<1 kSPS

Most precision SAR ADCs have an internal clock that manages the conversion process, so the conversion time (t_{CONV}) is fixed. With t_{CONV} being fixed, the lower the throughput and longer the cycle time (t_{CYC}), the longer the acquisition time

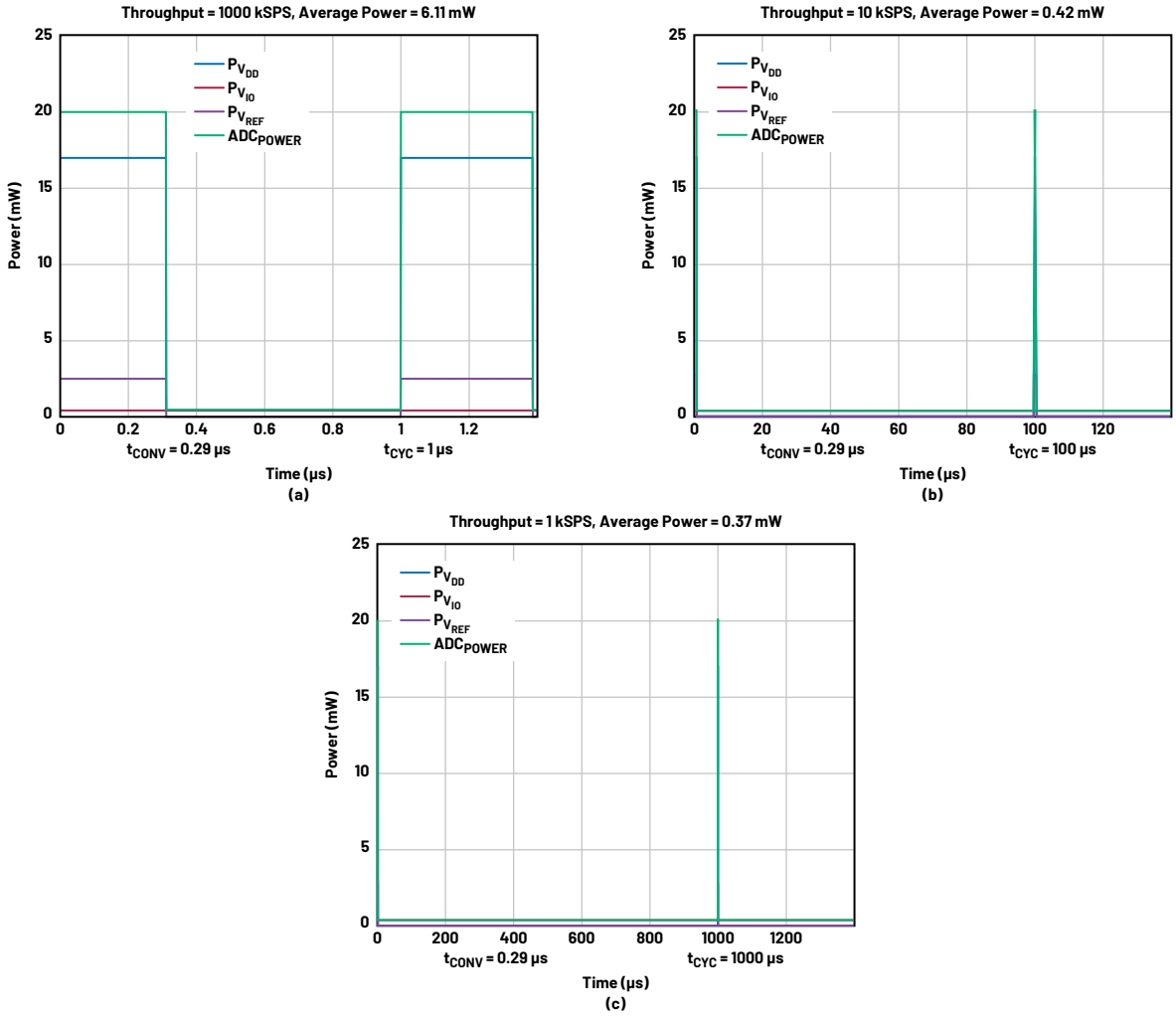

Figure 3. AD4008 SAR ADC timing diagram and power consumption during one cycle. The longer the cycle time, the lower the average power consumption: (a) avg. power = 6.1113 mW at 1 µs, (b) avg. power = 0.93756 mW at 10 µs, (c) avg. power = 0.36845 mW at 1 ms.

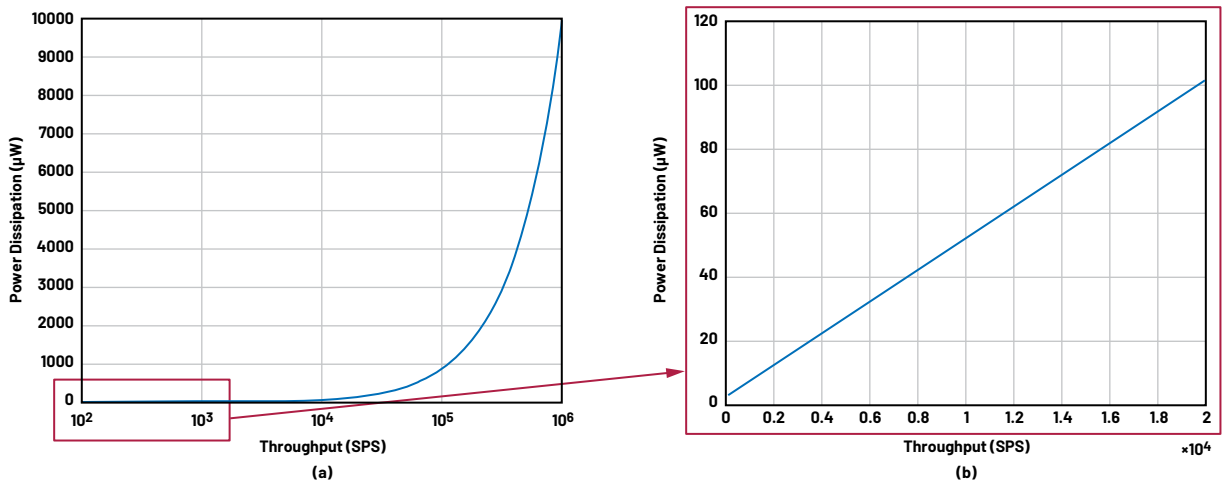

Figure 4. (a) AD4008's power scaling with throughput, graphical representation of (b) zooming in for the frequency range of interest—that is, under 10 kSPS.

(t_{ACQ}), which is the period where the ADC minimizes its power consumption. In other words, the lower the throughput rate, the lower the power consumption per sample acquired.

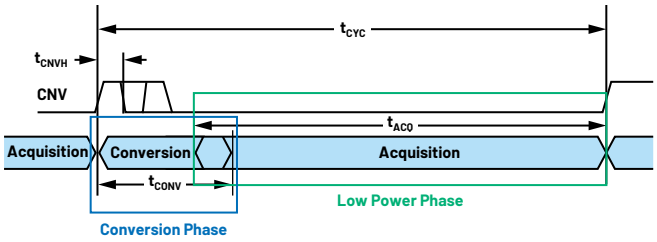

Figure 2. An SAR ADC timing diagram.

As conversions are triggered externally through a digital signal, the conversion speed can be tightly controlled. A slower sampling rate results in a longer acquisition phase and therefore a lower average power consumption. This can be observed in Equation 1:

$$ADC_{POWER} = P_{V_{DD}} + P_{V_{IO}} + P_{V_{REF}} =$$

$$= V_{DD} \times \frac{I_{DD} \times t_{CONV} + I_{STDBY} \times (t_{CYC} - t_{CONV})}{t_{CYC}} + \quad (1)$$

$$+ V_{IO} \times I_{IO} \times \frac{n_{BITS} \times t_{SCLK}}{t_{CYC}} + V_{REF} \times I_{REF} \times \frac{1/max\_tput}{t_{CYC}}$$

Where:

- t_{CONV} is the conversion time
- t_{CYC} is the inverse of the sampling rate
- V_{DD} is the analog supply
- V_{IO} is the digital supply
- n_{BITS} is the resolution of the ADC
- t_{SCLK} is the serial clock period time ($1/f_{SCLK}$)
- V_{REF} is the reference voltage and I_{REF} is the current at maximum throughput (max_tput)

So the ADC average analog power consumption will be inversely proportional to the sampling rate, according to Equation 1 and as seen graphically in Figure 4, if t_{CYC} is extended while t_{CONV} remains constant.

The power consumption of the ADC shown in Figure 1 is dominated by the analog supply during its conversion phase, as shown in Figure 2. For example, in a strain gage sensing circuit, the data acquisition rate can be as low as 1 kSPS, which allows the reduction of power consumption by 20-fold compared to running the AD4008 at maximum sampling speed.

Table 2. AD4008 Power Scales with Throughput

AD4008 Throughput Rate	Total Power Consumption
1 kSPS	300 µW
10 kSPS	400 µW
1 MSPS	6 mW

A graphical representation of Equation 1 shows how the power increases exponentially with throughput, as shown in Figure 4.

Reducing the ADC sampling rate results in longer acquisition time, which reduces the bandwidth requirements of the ADC driver amplifier, allowing a larger base of devices to choose from. Lower bandwidth amplifiers tend to have comparatively lower quiescent current. So lower ADC sampling rates not only lower ADC power consumption but also lower power requirements for companion amplifiers.

$$P_Q = I_Q \times (V_+ - V_-) \quad (2)$$

Table 3. Operational Amplifier Bandwidth vs. Current Consumption and Noise Performance; Bandwidth and Power Are Inversely Proportional

Op Amp	Bandwidth	I_Q	e_N
ADA4897-1	90 MHz	3 mA	1 nV/√Hz
ADA4610-1	16 MHz	1.6 mA	7.3 nV/√Hz
MAX40023	80 kHz	17 µA	32 nV/√Hz

However, selecting a lower bandwidth operational amplifier has its trade-offs. The lower bandwidth means a lower quiescent current (I_Q) but it comes at the expense of increasing the voltage noise density (e_N), as shown in Table 3. As a rule of thumb, lowering the quiescent current implies that the noise density increases at a ratio of $1/\sqrt{I_Q}$. However, note that the rms noise will be filtered by the adjusted bandwidth. In other words, a hardware designer might trade off power consumption (or battery life) vs. rms noise performance for the given sample rate, amplifier, and RC net bandwidth.

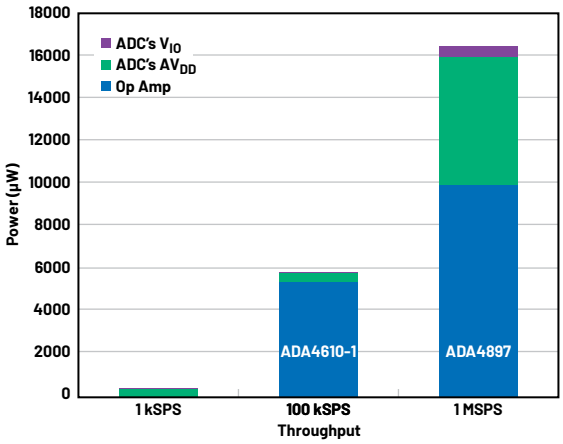

Figure 5. Power distribution per supply rail (op amp, analog, and digital rail), at various throughputs; different amplifiers were used depending on the bandwidth needs, as per Table 3.

Furthermore, the feedback resistors used to set the operational amplifier gain will impact power consumption as well: the larger these resistors are, the less power they will consume. This, again, comes with a noise trade-off as larger resistors generate more noise. A good design practice is to make the resistors as large as possible but not large enough that their contribution to the total noise is substantial. As individual noise contributions are root sum squared for obtaining total noise, following a common rule of thumb would lead us to set a maximum limit for resistor noise rms of 1/3 of that of the op amp, in order to keep their noise contribution less than 5% of the total. This would keep op amp noise dominant.

In some applications, where low frequency input signals are sampled at low throughput rates (a few kSPS), like the ones shown in Table 1, the driver amplifier could be removed, as long as no signal conditioning like a gain stage or low output impedance is needed. In higher speed applications, newer ADCs like the AD4000 or AD4696 families offer high input impedance (high-Z) modes that allow lower bandwidth (and lower power) amplifiers to drive the analog inputs, sometimes even eliminating the driver altogether. Removing this op amp will also contribute to minimizing total power consumption by eliminating its contribution, as indicated by the blue bar portion shown in Figure 5. This results in significant power savings compared to the use of traditional SAR ADCs that almost always requires a driver amplifier. In the case of the AD4696, a 16-channel device, this power savings is multiplied by 16 times. The reference high-Z mode feature also reduces the reference input current, and hence the overall system power consumption.

SAR ADC Signal Chain: AFE Dynamic Power Scaling

As described in the previous section, SAR ADC power consumption inherently scales with sample rate, but this is not true for other signal chain components. Amplifiers and voltage references consume constant quiescent current while they are powered up. Power cycling these components between ADC samples reduces the average power consumption of the signal chain. Having to wait for signals to be settled on every power cycle limits the time left for powering the system on and off. This is well explained in "What Are the Most Important Timing Factors for Low Power Precision Signal Chain Applications? Part 1" and "What Are the Most Important Timing Factors for Low Power Precision Signal Chain Applications? Part 2" (although an accurate analysis for each particular signal chain design is recommended).

Using highly integrated ADCs, with more analog front-end (AFE) blocks on chip, enables faster power-up and power-down transitions without compromising the performance. However, in many scenarios, a design may end up using discrete components for optimal performance. An example is shown in Figure 6.

This signal chain is multichannel and is comprised of one MAX41400 plus one anti-aliasing filter per channel, feeding into a 16-channel SAR ADC (the AD4696) with an ADR3425 precision reference.

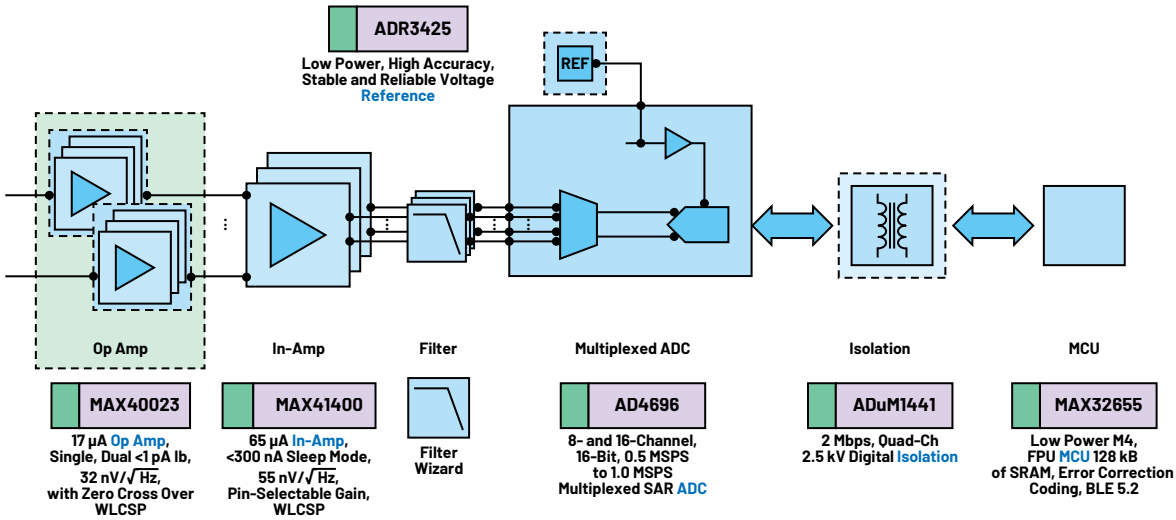

Figure 6. A multichannel measurement signal chain.

As shown in the previous section, running the ADC at the lowest acceptable throughput reduces its power consumption. Beyond that, if the idle time is large enough, the MAX41400 can be put into shutdown mode during a portion of the acquisition time, given that for a multiplexed system like this, only one amplifier needs to be powered up at a time. The frequency at which the amplifier, MAX41400, needs to be powered up is t_{CYC}/L_{SEQ}, where L_{SEQ} is length of sequence, which is 10 in the example given in FIgure 7. For example, if running conversions at 1 kSPS per channel and the conversion time is a maximum of 415 ns, that means the MAX41400 on each channel can be placed into shutdown mode for around 10% of the cycle time.

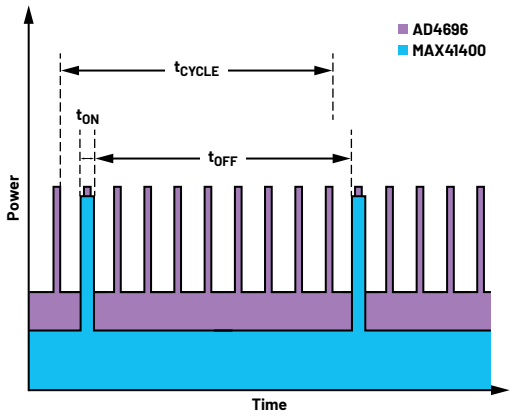

Figure 7. Power cycling the MAX41400 in a multichannel multiplexed application, based on the AD4696 ADC (assuming only 10 channels are in use for easier visualization).

The quiescent current (I_{Q_ON}) of the MAX41400 is 65 µA when fully powered up, but it can be reduced to 0.1 µA when placed into shutdown mode (I_{Q_OFF}). By powering it down in between samples, the average current consumed (I_{AVG}) by the amplifier can be scaled with throughput.

$$I_{AVG} = I_{Q\_ON} \times \frac{t_{ON}}{t_{CYC}} + I_{Q\_OFF} \times \frac{t_{CYC} - t_{ON}}{t_{CYC}} \quad (3)$$

Once again, the slower the throughput, the higher the t_{CYC} and lower the I_{AVG}. t_{ON} is the time during which the amplifier is turned on. When the ADC switches from acquisition to conversion phase, the amplifier can be powered off, as extending t_{ON} longer than the minimum required does not yield any benefit. This off-time ($t_{OFF} = t_{CYC} - t_{ON}$) should be maximized for minimum power consumption, just not to the extent of compromising SNR or THD. Finding the right timing will depend on the application, the devices used, and the throughput rates. In fact, t_{ON} and throughput are maybe inversely proportional: lower throughputs lead to longer idle time, and longer idle time requires longer t_{ON} to power the amplifier back up. Based on the data sheet, the typical conversion time of the AD4696 is 415 ns. This conversion time plus the 100 µs required to power up the MAX41400 after shutdown will add up to the minimum t_{ON} time. So the average current consumption will be:

$$I_{AVG} = 65\ \mu A \times \frac{100.5\ \mu s}{1000\ \mu s} + 0.1\ \mu A \times \frac{899.5\ \mu s}{1000\ \mu s} = 6.62\ \mu A \quad (4)$$

Compared to an amplifier that is always enabled, the shutdown modes and fast power-up time of the MAX41400 result in a 10× reduction in current consumption.

For a more general view, besides power savings calculated on the examples shown so far at a given throughput rate, all these equations can be represented graphically as in Figure 9, with the specifications taken from the data sheets (assuming reference and analog input high-Z mode are enabled).

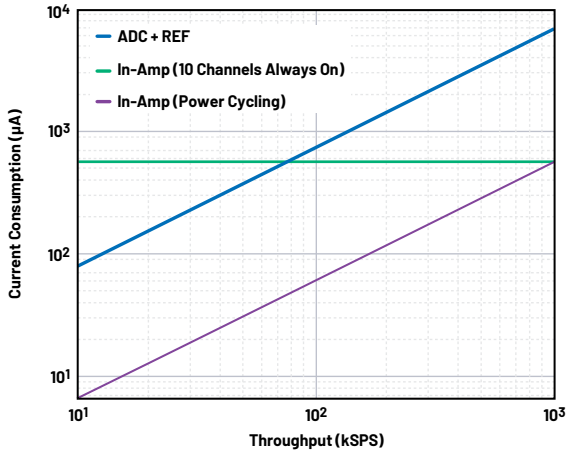

Figure 8. Signal chain power consumption vs. throughput, with and without power cycling at the front end.

This same analysis can be done for battery life, as opposed to power consumption, by dividing the battery capacity by the average current drawn.

Table 4. Batteries' Capacity

Battery	Capacity (mAh)
CR927	30
2× LR44	158
2× AAA	1000
CR2354	560

In this case, the relationship is inversely proportional—that is, the lower the throughput, the longer the battery will last.

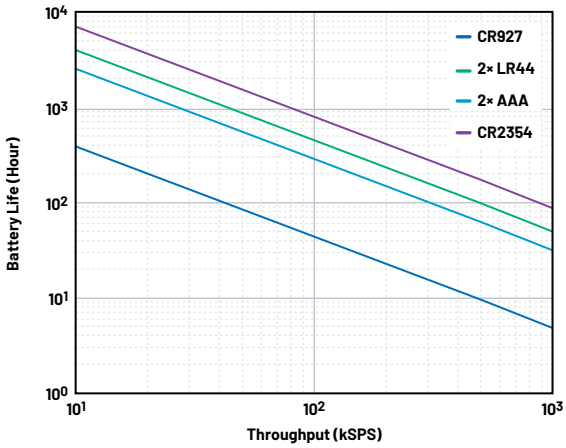

Figure 9. Battery life extends with power cycling/scaling.

Any amplifier, even if it does not have a shutdown mode like the MAX41400, can be power cycled like shown earlier. That is, powering it on and off completely instead of entering shutdown mode. However, care must be taken. On one hand, the wake-up time will be longer to get the amplifier ready, so the minimum t_{ON} will be longer. On the other hand, charging and discharging the decoupling capacitors over and over again will have implications on the current drawn to charge them up every power cycle, increasing the overall power consumption compared to using shutdown modes. Also, if the sensor is still driving the amplifier inputs while the rails are not powered up, this may lead to damage if they are unprotected.

SAR ADC-Based Signal Chain: Digital Supply Power Scaling

The previous section focused on reducing the analog supply power consumption, given it is the maximum contributor to the total power consumption. Reducing the throughput also has an impact on the digital power consumption as it allows the serial clock to run at a lower frequency:

$$I_{10} = C_{SDO} \times V_{10} \times f_{SCLK} \quad (5)$$

Equation 5 indicates that there are two extra potential steps we can take to minimize digital power consumption:

- Use a lower digital supply voltage (V_{10})
- Minimize the trace capacitance of the serial data output line

Another point to note is the value of the pull-up/pull-down resistors used in the digital communication lines. These resistors are used to ensure a proper logical level at the digital input/output, and their value may have an impact on the overall system power consumption. Using too low a resistor value, also known as strong pull-up, will cause a high current to flow through it. Hence, unnecessarily low values should be avoided. On the other end, if the resistance is too high, the voltage drop caused by the leakage current could result in the interpretation of an incorrect logic level. In addition, the voltage drop impacts the propagation. So designers must use the highest resistor value without compromising the voltage level (this will depend on the digital supply voltage and leakage current) or the signal integrity.

Sigma-Delta ADC-Based Signal Chain

In the case of sigma-delta ADC-based signal chains, the power scaling concept described in previous sections is not applicable straight away. This is because the conversions are not externally triggered, but rather they work from a free running clock.[4] So they cannot remain idle for a certain period of time as a function of an external conversion start signal.

However, many sigma-delta ADCs feature standby modes that can be used if the ADC does not need to convert continuously. As in previous sections, timing considerations[5] need to be taken into account as recovering the device from standby mode requires a wake-up time during which no samples can be taken.

Highly integrated sigma-delta ADCs like the AD4130 offer duty cycling modes in addition to standby modes. That way, the ADC powers up and down automatically without the need to interact with the host every cycle. The AD4130 offers two modes, 1/4 and 1/16, which means it is active during 1/4 or 1/16 of the time. That leads to significant power reduction compared to continuous conversion mode, as shown in Figure 10.

Table 5. AD4130 Current Consumption for Each Power Mode

AD4130 Power Mode	Typical Current Consumption
Continuous Conversion	32 µA
Duty Cycling	5 µA
Shutdown Mode	0.5 µA

Depending on the required throughput rate, techniques for optimizing power consumption can be either using one of the duty cycling modes, or just putting the part into standby mode for a given period. Indeed, the AD4130 has many operating modes that may impact power consumption of the ADC. The active functional model available in ACE[6] shows the power consumption and the expected battery life for the selected ADC configuration.

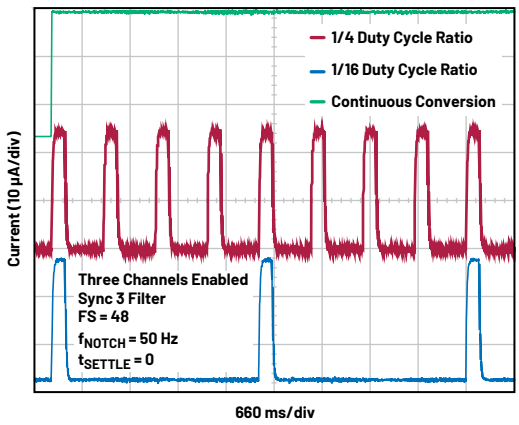

Figure 10. AD4130 current consumption under different modes of operation: continuous conversion, 1/4 duty cycle, and 1/16 duty cycle.

Sigma-Delta ADC-Based Signal Chain: AFE Dynamic Power Scaling with Duty Cycle

Just as with the SAR ADC-based signal chain, a sigma-delta-based signal chain can take advantage of the duty cycle to power down certain blocks during the time the ADC is placed into low power state (Figure 10). That would allow AFE power savings similar to the ones shown in Figure 9.

Sensor Excitation

Complete solution devices like AD4130 provide not only the core converter but also the internal programmable gain amplifier plus sensor biasing and excitation (selectable current source and precision voltage reference). This integration has implications in terms of ease of use, size, and optimization on the use of biasing, timing, or power cycling among the different building blocks. So, AD4130 on its own reduces the overall system power consumption by housing all these blocks on chip. Furthermore, it simplifies the design cycle thanks to its flexibility to be used in many different platforms like RTD, thermistor, or bridge sensors, to name a few. It also reduces the BOM count and the need for several power supply rails.

Other Power Optimization Techniques

Throughout this article, several ways for minimizing the signal chain power consumption have been presented. However, one portion of the signal chain has not been considered yet: the host controller. If the controller is powered up all the time because it needs to read and postprocess data from the ADC, it is going to sink a good portion of the power. Placing the controller into sleep mode while not in use will help achieve extra power savings.

ADCs with On-Chip FIFO

If the application does not need real-time data, but must read data points at much lower rate, ADCs with on-chip FIFO might play a role. The AD4130 incorporates such a block and this FIFO can store up to 256 conversions, so if the output data rate (ODR) is, for example, 2.4 kSPS, instead of reading every 416 µs, the microcontroller can be put to sleep mode and wake up every 100 ms to read the whole data memory in one go (see the Data Transfer section in Figure 11). In other words, having an ADC with memory that stores up to the latest 256 samples enables power cycling of the microcontroller too, thereby drastically reducing the overall system power consumption.

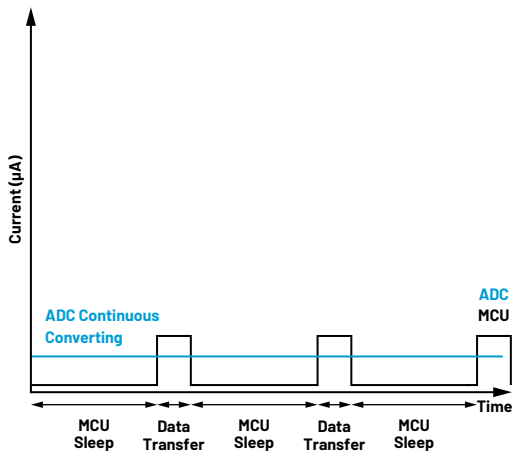

Figure 11. Microcontroller power reduction by using the ADC's on-chip FIFO.

Streaming ADC Data to Memory Through Direct Memory Access (DMA)

For ADCs that do not include on-chip FIFO, an alternative would be to use the direct memory access (DMA) available in most microcontrollers. DMA enables passing of data directly from a peripheral (in this case, the SPI) to memory (SRAM) without CPU intervention or interrupts for every single ADC sample received. The chosen microcontroller will have a direct impact on the achievable power savings. In many cases, the microcontroller will be able to stay in sleep mode most of the time and trigger an event only when an ADC sample is received. This event will then just briefly alert the DMA to start performing the SPI transactions and to return to sleep thereafter, thus minimizing the microcontroller power consumption compared to having the CPU fully awake for the whole SPI transaction. Note that using the DMA is only applicable if the format of the ADC data matches the destination memory. That is, for most microcontrollers, the DMA can be easily used only when the ADC data is 16 or 32 bits long.

Interrupt-Driven Programming

Many low power applications do not require the recording and processing of every single data point, but rather monitoring that the magnitude sensed is within certain thresholds. Traditionally, to do this, the host controller needed to be always awake in order to read each ADC sample and decide if the value was acceptable or not, then consequently, it would trigger an interrupt routine if need be.

Both the AD4696 (SAR ADC) and AD4130 (sigma-delta ADC) incorporate these threshold detection functions. Thresholds can be programmed such that a GPIO pin asserts only if the ADC output code is out of the user-defined bounds. This way, the host controller can stay in sleep mode most of the time and only wake up when the GPIO asserts, minimizing its power consumption given it will only be active when it is necessary to perform an action.

Conclusion

When designing a battery-powered measurement system, for applications such as portable field instruments, condition monitoring, or vital sign measurements (VSM), low power signal chains presented in analog.com/precisionlowpower are ideal for achieving power optimized solutions. Analog Devices' precision low power signal chains ease the journey for designers building low power measurement solutions, which offer the optimal combination of precision amplifiers, voltage references, ADCs, and isolation products. In these signal chains, power consumption is optimized while keeping noise performance, size, and ease of use as key vectors. These signal chains come in different flavors: single-channel, discrete multichannel (multiplexed), and also fully integrated multichannel solutions and ready-to-go power optimized designs, offering an excellent starting point for low power design.

Beyond presenting ADI's precision low power signal chains, this article demonstrated several system-level techniques that make the designed signal chains even more power efficient. Such techniques include power scaling, power cycling, duty cycling, or using on-chip features like FIFOs or interrupt-driven features like threshold detection.

References

[1] Padraic O'Reilly. "What Are the Most Important Timing Factors for Low Power Precision Signal Chain Applications? Part 1." *Analog Dialogue*, Vol. 56, No. 3, August 2022.

[2] Padraic O'Reilly. "What Are the Most Important Timing Factors for Low Power Precision Signal Chain Applications? Part 2." *Analog Dialogue*, Vol. 56, No. 3, August 2022.

[3] *The Data Conversion Handbook*. Analog Devices, Inc., 2005.

[4] Michael Clifford. "Fundamental Principles Behind the Sigma-Delta ADC Topology: Part 1." Analog Devices, Inc., January 2016.

[5] Bruce Pepitas. "Introduction to Dynamic Power Scaling." Analog Devices, Inc., January 2016.

[6] Analysis | Control | Evaluation (ACE) Software. Analog Devices, Inc.

Brandon Hurst. "How to Accelerate Peripheral Monitoring in Low Power Wearables with DMA." *Analog Dialogue*, Vol. 56, No. 1, January 2022.

Maithil Pachchigar and Alan Walsh. "Next-Generation SAR ADC Addresses Pain Points of Precision Data Acquisition Signal Chain Design." *Analog Dialogue*, Vol. 50, No. 4, December 2016.

Sanjay Rajasekhar and Arvind Shankar. "How to Leverage Input High-Z Technology to Reduce Solution Power and Size." Analog Devices, July 2022.

About the Author

Lluis Beltran Gil received his B.S. degree in electronics engineering in 2009 and in industrial engineering in 2012, both from the Universitat Politècnica de València, UPV (Technical University of Valencia). After graduation, Lluis joined Analog Devices in 2013 as an applications engineer in the Precision Converter Group in Limerick. Currently, Lluis is working on the SAR ADC Applications Team within the Instrumentation BU, and he is based in Valencia, Spain, where he also received his M.Sc. degree in electronics engineering from Universitat de València, UV (University of Valencia).