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Achieve Accurate RF Testing with a Raspberry Pi-Based DDS Signal Generator

Erbe D. Reyta, Hardware Applications Engineer,
Valentin Beleca, System Integration Engineer, and
Mihai Bancisor, Systems Integration Engineering Manager

Abstract

One of the most important aspects to consider in hardware testing that involves radio frequency (RF) is choosing a configurable, calibrated, and reliable signal source. This article provides a complete implementation of a Raspberry Pi-based, highly integrated solution for a synthesized RF signal generator that outputs a single tone from DC up to 5.5 GHz with output power ranging from 0 dBm to –40 dBm. The proposed system is based on a direct digital synthesis (DDS) architecture and its output power vs. frequency characteristic is calibrated, ensuring the output power stays within ±0.5 dB on the desired power level over the entire operating frequency range.

Introduction

An RF signal generator, particularly at microwave frequencies, has historically been generated based on phase-locked loop (PLL) synthesizers.[1] The PLL allows the generation of stable high frequency from a low frequency reference. A basic PLL model is presented in Figure 1. This model consists of a feedback system composed of a voltage-controlled oscillator that varies the output frequency, an error detector that compares the input reference frequency and the output frequency, and the frequency divider. The loop is said to be in a locked condition when the output frequency and phase of the frequency divider are equal to the frequency and phase of the input reference.[2-5]

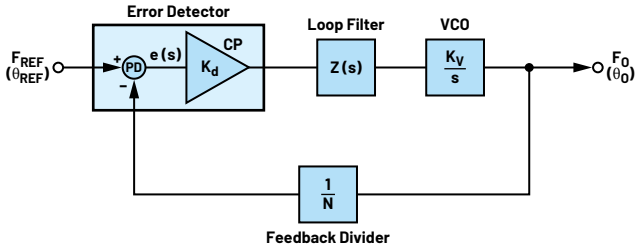

Figure 1. A basic PLL model.

Depending on the application, DDS architecture may present a better alternative to PLL as a frequency synthesizer. A typical DDS-based signal generator is shown in Figure 2. A tuning word is applied to a phase accumulator, which determines the slope of the output ramp. The upper bits of the accumulator are passed through an amplitude-to-sinusoid converter, and finally to a DAC. A DDS architecture gives distinct advantages over PLL. For instance, the DDS digital phase accumulator enables output frequency tuning resolutions much finer than a PLL-based synthesizer.

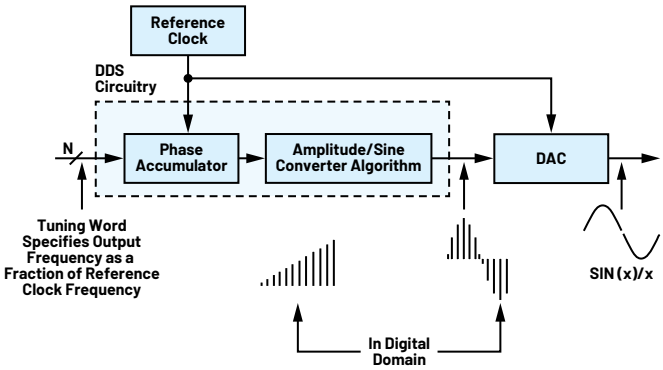

Figure 2. A typical DDS-based signal generator.

The PLL switching time is a function of its feedback loop settling time and VCO response time, which is slower by nature compared to a DDS, which is only limited by its digital processing delay. In terms of board size, a DDS offers a smaller area that translates to ease of system design and therefore eliminates various hardware RF design challenges.[6]

The following section will discuss the overall system design of a complete DC to 5.5 GHz sine wave signal generator based on DDS architecture, the CN0511. This will be followed by a discussion on the vector signal generator architecture and its specifications. The next section will focus on the system clocking as it describes the clock reference requirements and the circuit connections between the clock management unit and the vector signal generator. Power supply architecture and the system layout are also included in the discussion, describing how the overall system achieves high power efficiency and acceptable thermal dissipation. Then, the Software Architecture and Calibration section will discuss system software controls and calibration. In this section, the flexible control provided by the software will be explained as well as how the output power was calibrated. The last section describes the overall system performance including system phase noise, calibrated output power, and thermal performance of the system.

System-Level Architecture and Design Considerations

A: System-Level Design

The system shown in Figure 3 is a complete DC to 5.5 GHz sine wave signal generator based on a DDS architecture. A quad-switch DAC core and integrated output amplifier provide exceptionally low distortion over the entire operating frequency range, with a matched 50 Ω output termination.

The on-board clocking solution includes a reference oscillator and PLL, eliminating the need for an external clock source. All power is derived from a Raspberry Pi platform board, with ultrahigh power supply rejection ratio (PSRR) regulators and passive filtering to minimize the impact of the power converters on RF performance.

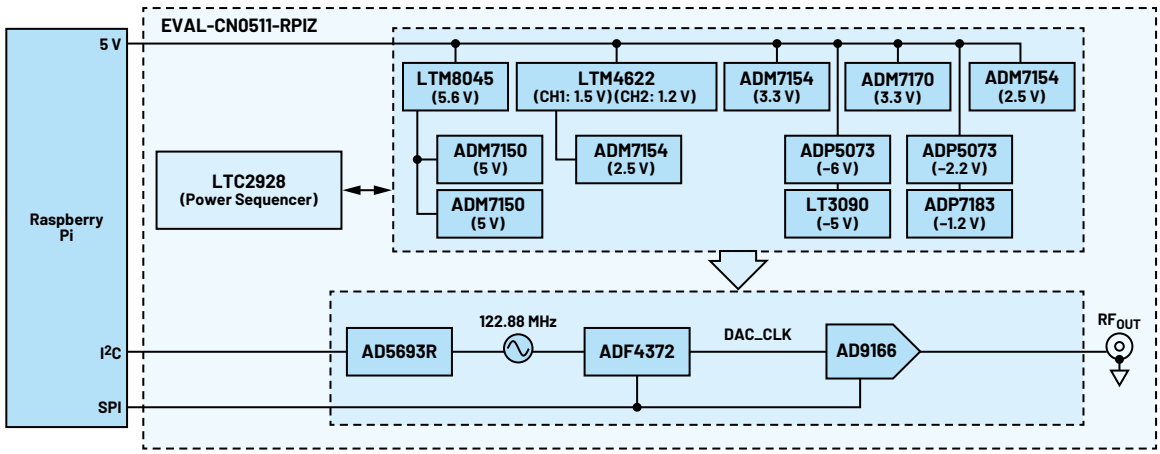

Figure 3. The CN0511: an RPI-based synthesized RF signal generator.

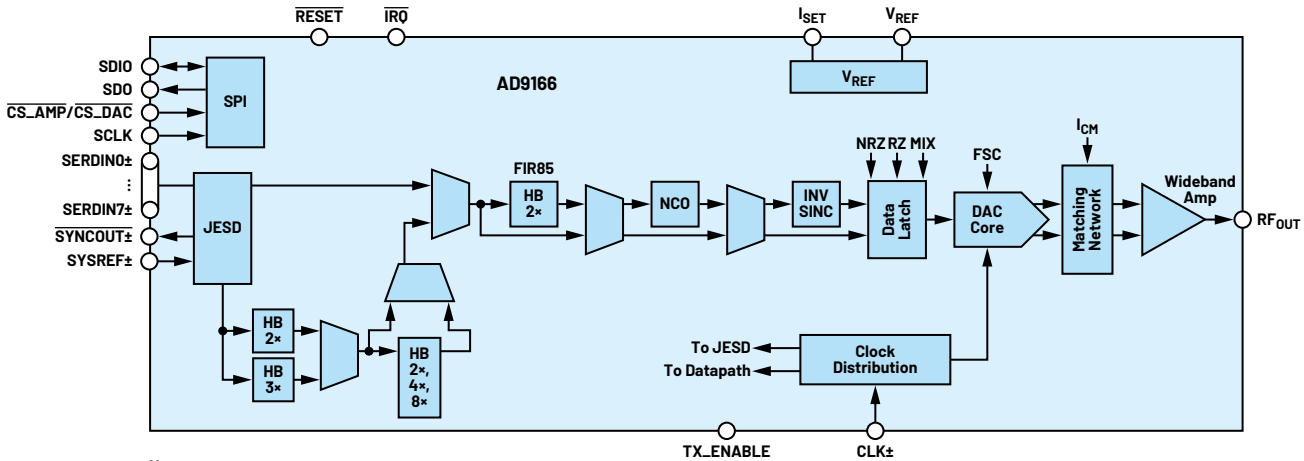

Figure 4. The vector signal generator used (AD9166)—a functional block diagram.

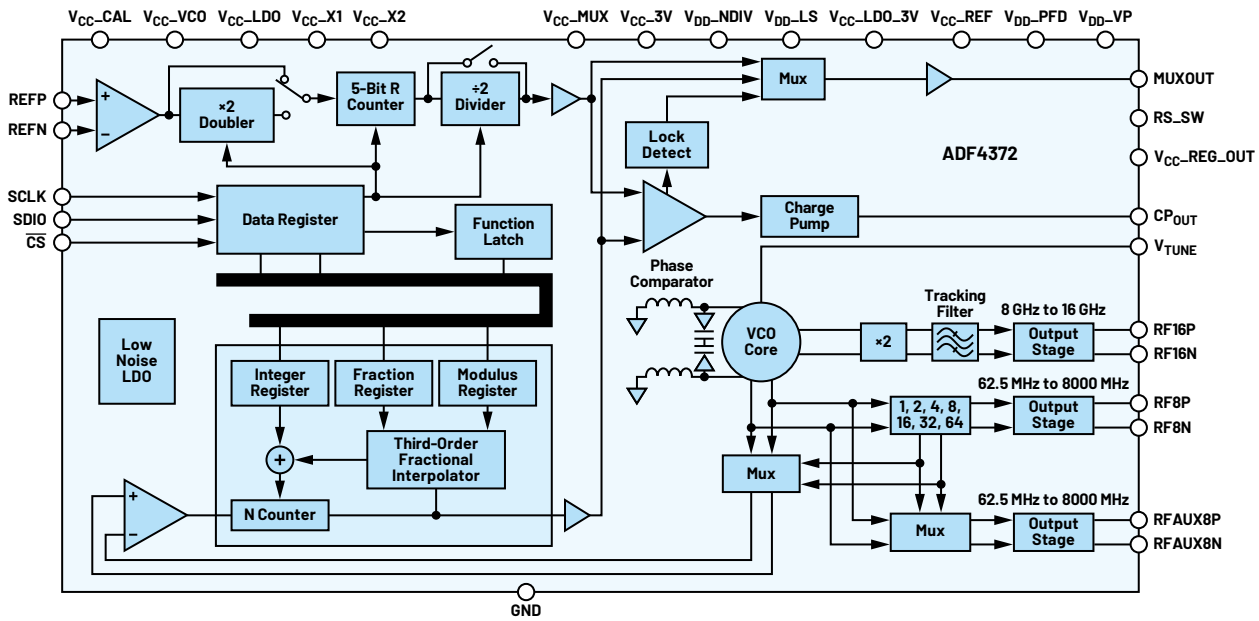

Figure 5. An ADF4372 RF8x output stage.

The architecture shown in Figure 3 can be used for various applications such as in radar, automated testing, an arbitrary waveform generator, and a single-tone signal generator. In this article, the latter is implemented. The following subsections will discuss the major integrated devices contained in the CN0511.

B: Vector Signal Generator

The DC to 9 GHz vector signal generator used, as shown in Figure 4, incorporates a 6 GSPS (1×, nonreturn to zero mode) DAC, 8-lane, 12.5 Gbps JESD204B data interface, and a DDS with multiple numerically controlled oscillators (NCOs). It is also a highly configurable digital data path that includes interpolation filters, inverse SINC compensation, and digital mixers to allow flexible spectrum planning.

The system shown in Figure 4 utilizes the DAC 48-bit programmable modulus NCO to enable digital frequency shifts of signals with very high precision (43 µHz frequency resolution). The NCO for this DAC only requires the 100 MHz speed of the SPI write interface for rapid updating of the frequency tuning word (FTW). The SPI also allows the configuration and monitoring of various functional blocks found in that DAC. The JESD lanes are not used in this design and the device is used in NCO only mode.

The vector signal generator from Figure 4 has an integrated output RF amplifier that is single-ended and 50 Ω matched, thus eliminating challenging RF output circuit interfaces. Table 1 shows the AD9166's highlights and performances under various conditions.

Table 1. AD9166 Highlight Specifications

Parameter	Value	Condition
Band Flatness	DC to 9 GHz	
SFDR	–83 dBc	For 51 MHz tone
	–66 dBc	For 451 MHz tone
	–38 dBc	For 4051 MHz tone
Power Consumption	~4 W	For 5000 MHz tone
Phase Noise	–134.8 dBc/Hz	At 3600 MHz tone; 10 kHz offset
Package	324-ball BGA (15 mm × 15 mm)	

C: System Clocking

The system in Figure 2 uses the ADF4372 PLL (see Figure 5), a wideband synthesizer with integrated VCO, that allows the implementation of fractional-N or integer-N frequency synthesizers when used with an external loop filter and an external reference frequency. In addition, the VCO frequency is connected to a divide by 1, 2, 4, 8, 16, 32, or 64 circuit that allows the user to generate RF output frequencies as low as 62.5 MHz at RF8x.

The quality of the clock source such as its phase noise and spur characteristics, as well as its interface to the high speed DAC clock input, directly impacts AC performance. Hence, phase noise and other spectral content are modulated directly onto the output signal. To achieve optimum integer boundary spur and phase noise performance, the ADF4372 uses a single-ended reference input signal, which is then multiplied to produce the clock for the high speed DAC as shown in Figure 6.

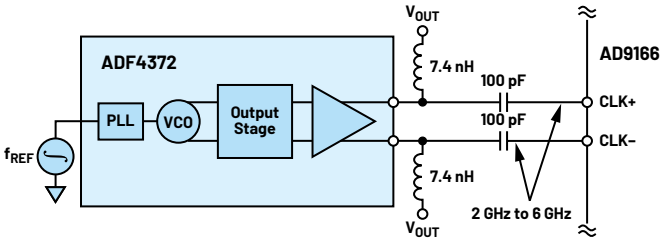

Figure 6. Circuit connection between the ADF4372 and the AD9166.

D: Power Supply Architecture

The system power tree for the CN0511, shown in Figure 7, uses the LTM8045, LTM4622, and ADP5073 switching regulators to achieve 90% efficiency based on the system load requirements. The low dropout linear regulators (LDOs), such as the ADM7150, ADM7154, and ADP1761, were chosen to supply the DAC, amplifier, PLL, and VCO for their ultralow noise and high PSRR to achieve the best phase noise performance possible.

The LTC2928 power sequencer IC was used to ensure that the high speed DAC powers up in the correct order to avoid damage to its internal circuitry. The power sequencer IC monitors and manages up to four voltage rails, individually controlling the power on time and its other supervisory functions, which include undervoltage and overvoltage monitoring and reporting.

E: Layout Consideration

For this application, where the highest performance and higher output frequencies are required, the choice of printed circuit board (PCB) materials significantly impacts results. Figure 8 shows the recommended CN0511 PCB stack-up, which uses Rogers 4350 dielectric material on the layers that contain RF traces to minimize the signal attenuation in signals greater than 3 GHz and this also ensures the best signal integrity at the RF output.

Figure 8. Recommended PCB cross section and stack-up.

Thermal performance is directly linked to PCB design and operating environment. To improve the thermal performance of the design, thermal vias are used on the PCB thermal pad.

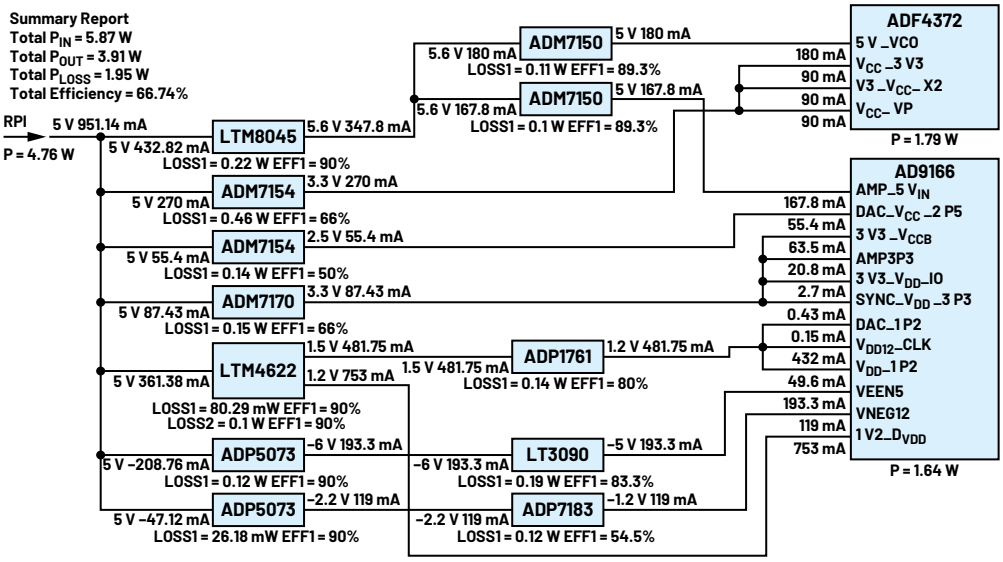

Figure 7. System power tree.

Software Architecture and Calibration

A: Software Control

In any application involving a signal generator, the control of the instrumentation equipment is desired to be easy and flexible. The CN0511 can be considered plug and play because it only needs one SD card with a Kuiper Linux image plugged into the Raspberry Pi. The Kuiper Linux image contains all the necessary software needed to control the signal generator. There are two methods for changing the output power and frequency: the PyADI-IIO module can be used to write the code or the IIO-Oscilloscope graphical user interface (GUI) can be used to input the desired output.

The PyADI-IIO is a Python abstraction module for ADI hardware with industrial input/output (IIO) drivers. This module provides simplified and easy to use Python methods and attributes for controlling the hardware. The board can be controlled with very simple Python lines of code that can be run locally or remotely. Any sweep in frequency for testing other equipment can be created with a simple for loop and some delays.

The IIO-Oscilloscope is a cross-platform GUI application, where the output power amplitude and frequency are required as input from the user.

Both modules, PyADI-IIO and IIO-Oscilloscope, provide the output of the junction temperature sensors: one inside the PLL IC and the other one inside the vector signal generator IC. Figure 9 depicts these two software modules as well as the other components needed to communicate with the CN0511 board (libAD9166, LibIIO, and Linux Kernel). libAD9166, shown in Figure 9, is another library that is required for accurate control of the output power and is preinstalled on the Kuiper image. This library contains the C++ code required to output the calibrated power and is specific for this board. The theory behind how the calibration is achieved continues in section B: Output Power Calibration.

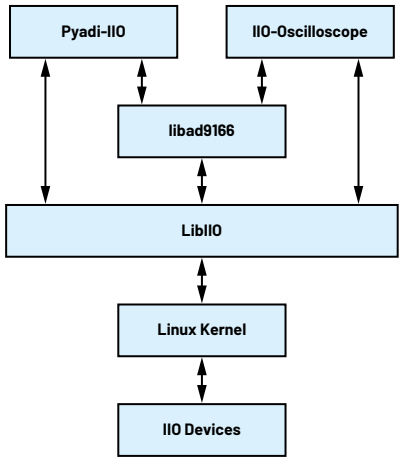

Figure 9. A block diagram with the software components needed to communicate with the device through the PyADI-IIO and IIO-Oscilloscope.

B: Output Power Calibration

In signal generator applications, band flatness is a critical parameter. In this system, the output power vs. frequency characteristic is mainly given by the vector signal generator's output. As the frequency increases, the output impedance decreases from its DC value. This change in output impedance, along with any impedance mismatch at the load, directly affects the output power. Moreover, a predictable sinc roll-off also affects the output power response in frequency. The measured uncalibrated output power vs. frequency characteristic is discussed and displayed in Figure 10. To overcome these undesired factors, a software calibration of the output power vs. frequency was implemented.

The knobs that allow for the output power to be corrected are two registers from the AD9166: the 10-bit register that sets the full-scale current, Ioutfs_reg (addresses 0x42 and 0x41), and the 16-bit register that sets the full-scale current, Iout_reg (addresses 0x14E and 0x14F). These two registers control the output current of the AD9166's DAC, which is also the input for the AD9166's amplifier (Figure 3).

Ioutfs_reg offers a dynamic range of the output power of about 10 dBm, a perfect value for adjusting the undesired characteristic shown in Figure 10.

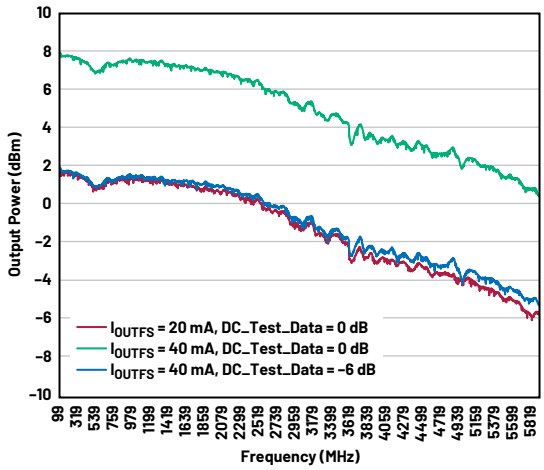

Figure 10. Output power vs. frequency: uncalibrated output power.

From measurements, each PCB sample displayed the same shape of the characteristic shown in Figure 10, except for an offset difference. Taking that into consideration, two calibration routines were developed. The first calibration routine is done only once and obtains the parameters needed to correct the whole shape, making it flat, and the second routine corrects the offset error between each board and is run as a production test for each board. Both calibration routines are done by output measurements, calculations, and register adjustments based on calculations.

The main idea behind the first calibration routine is displayed in Figure 11. First, the whole characteristic from Figure 10 is split into multiple frequency intervals that can be approximated with line segments from $f_{min}[x]$ to $f_{max}[x]$ where x is the index of the interval, $x \in [0, 31]$, and x is an integer and positive value. For the actual design, 31 intervals were chosen but only three intervals are displayed in Figure 11a for better exemplification. For each interval, two constants need to be obtained: one for offset correction, Offset_correction (Figure 11b), and one for gain

correction, Gain_correction (Figure 11c). The parameter $f_{min}[x]$ also needs to be stored to track the intervals.

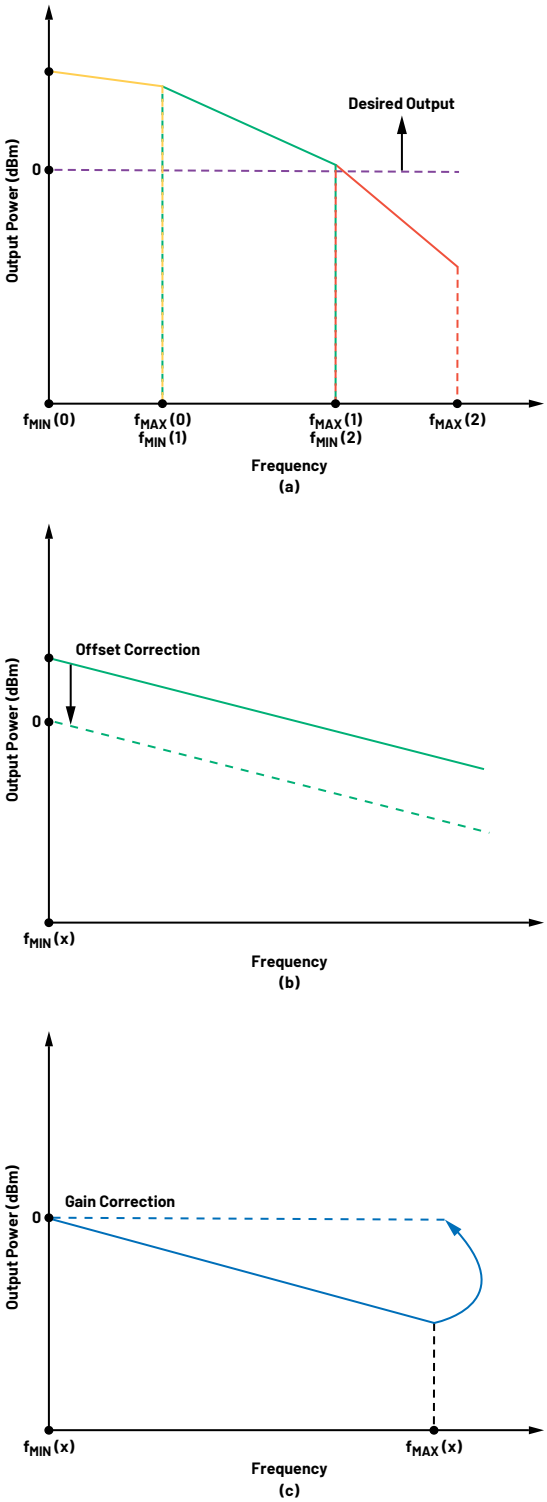

Figure 11. Visual exemplification for the calibration routines: (a) splitting the characteristic into multiple segments; (b) offset correction for each segment; (c) slope correction for each segment.

Figure 12a displays a pseudocode flowchart that captures how the first calibration routine works. To accomplish this algorithm, a very accurate spectrum analyzer is needed to measure the output power (Keysight E5052B/R&S FSUP was used). The parameters resulting from the first routine (Figure 12a) are used in the second calibration routine, which is shown in Figure 12b.

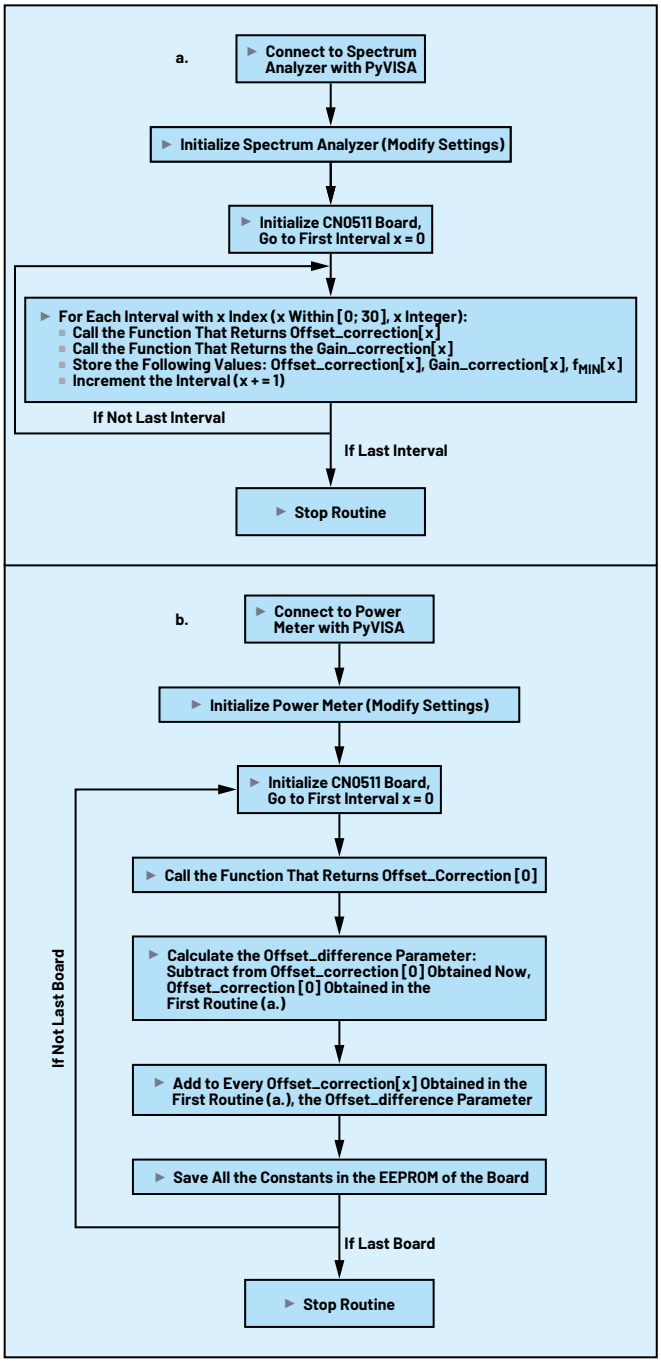

Figure 12. A pseudocode flow graph for: (a) the first calibration routine that runs only once; (b) the second calibration routine that runs on every CN0511 board.

The second calibration routine (Figure 12b) runs for each PCB sample in a production test and adds the same constant to Offset_correction parameter for each interval. At the end of the second routine, the modified parameters Offset_correction[x] as well as Gain_correction[x] and $f_{min}[x]$ are stored in the EEPROM of the board for each interval. These parameters are further used in the software when the board is functioning.

To set the calibrated output power, Equation 1 is used in the software to calculate the value on Ioutfs_reg register needed to adjust the output power at the frequency fx. The fx is the frequency within the interval x: fx ∈ [f_{min}[x], f_{max}[x]), fx being a real positive number, and f_{min}[x] is the minimum frequency of the interval with the x index.

$$I_{OUTFS}\_reg[x, fx] = Offset\_correction[x] + \\ + Gain\_correction[x] \times (fx - f_{MIN}[x]) \quad (1)$$

As seen in Equation 1, three parameters must be stored on the board to allow the output correction for each interval, x: Offset_correction[x], Gain_correction[x], and f_{min}[x].

System Performance

A: Calibrated Output Power

Figure 13 shows the wideband compensated band flatness of the CN0511 at several different output power levels. For any output power set between 0 dBm and –40 dBm, the accuracy is ±0.5 dBm in the whole band, from DC to 5.5 GHz.

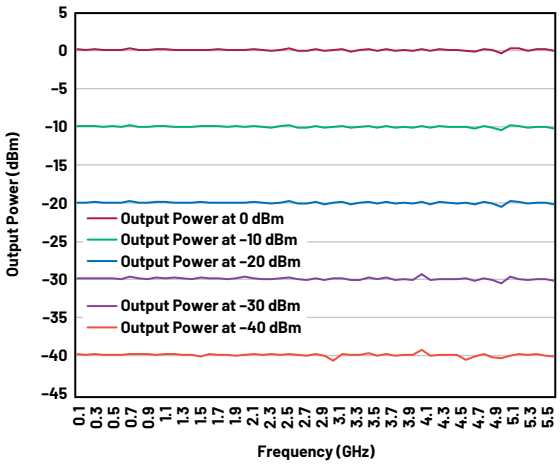

Figure 13. Calibrated output power vs. frequency.

B: Phase Noise

The quality of the clock source, as well as its interface to the AD9166 clock input, directly impacts phase noise performance. Phase noise and spurs at a given frequency offset on the clock source are directly transferred to the output signal. The graphs displayed in Figure 14 are of the single side band (SSB) phase noise vs. frequency offset as measured. All data were collected with the output power set at full scale. The onboard 122.88 MHz CMOS voltage-controlled crystal oscillator was used as a system clock reference.

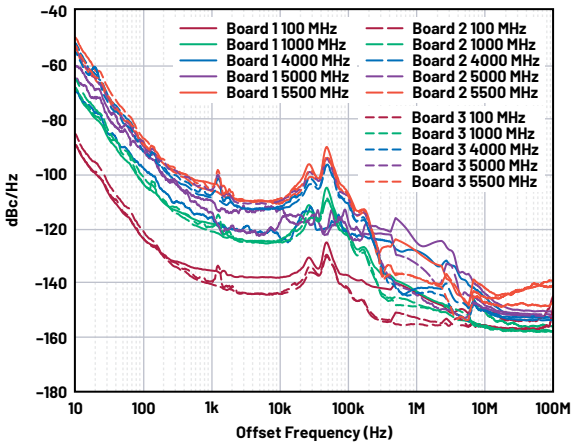

Figure 14. System phase noise performance.

C: Thermal Performance

The high speed DAC can dissipate nearly 4 W depending on the application and configuration. It uses an exposed die package to reduce thermal resistance and allow the cooling of the die directly. A mechanical heat sink with a fan is used to dissipate the thermal heat from the package. With heat sinks attached, the LTM4622 shows the highest thermal reading that is around 60.6°C at an ambient temperature of 25°C.

Conclusion

A high frequency, low distortion, and low noise signal source was proposed in this article. The system presented is a solution for a low cost RF signal synthesizer using high speed DAC-based DDS architecture. Using a vector signal generator, based on a DDS technique, the proposed system offers several advantages over a simple PLL such as simplicity, low distortion, high resolution tuning, nearly instantaneous frequency hopping, phase, and amplitude modulation.

The advantages of the DDS architecture used bring the possibility of adjusting and calibrating the output power as well as fine-tuning of the output frequency. Adding a calibration routine in the system provides the user with an output reference tone, from DC to 5.5 GHz, that has ±0.5 dBm accuracy with a dynamic range from 0 dBm to –40 dBm—a near perfect solution for a laboratory instrument.

Acknowledgment

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About the Author

Erbe D. Reyta has been a hardware application engineer in ADI's Circuits from the Lab® program since 2011 where he has mainly focused on precision system hardware development. He earned his bachelor's degree in electronics and communications engineering at the University of the Philippines-Diliman and attained his master's in engineering degree in computer engineering at Pamantasan ng Lungsod ng Maynila (University of the City of Manila) in the Philippines.

About the Author

Valentin Beleca is a system integration engineer at Analog Devices where he works on PCB design. He started working at ADI in November 2021 in Cluj-Napoca, Romania. He is currently an M.Sc. student in the Integrated Circuits and Systems Master's Program at Technical University of Cluj-Napoca and he has a B.Eng. in electronics and telecommunications from Technical University of Cluj-Napoca.

About the Author

Mihai Bancisor is a systems integration engineering manager in the Customer Office Solutions Group and has been with Analog Devices for 11 years. His focus is software-defined radio and system on modules. He holds a B.Sc. and an M.Eng. in applied electronics from the Technical University of Cluj-Napoca.