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Smart Battery Backup for Uninterrupted Energy Part 1: Electrical and Mechanical Design

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Abstract

This article outlines the system requirements for the Open Compute Project Open Rack Version 3 (OCP ORV3) battery backup unit (BBU). It emphasizes the importance of having an efficient and intelligent BBU that can provide energy during power outages. Additionally, it will showcase the analog and digital design solutions, electrical and mechanical solutions, and their architectures that are developed to meet the written specifications.

Introduction

Data centers power the internet, connecting communities worldwide. Social media companies like Facebook, Instagram, and X (formerly known as Twitter) rely on data centers for their information dissemination and storage, while search engines like Yahoo! and Google utilize data centers to power their primary search engine and storage functions. Nearly all major companies and government agencies around the world require reliable data center functionality to operate and maintain their primary business functions by way of intelligent computing, storage, and search. As the number of users grows each year, data center capacity continues to grow at an extraordinary rate to keep up with demands as well as technology improvements. As these growth demands increase, so too must the data center system architecture to keep pace.

The OCP, an organization that shares data center designs, has a system architectural definition that is based on the Open Compute Project Open Rack Version 2 (OCP ORV2) in which the backplane voltage is nominally 12 V and a system power of 3 kW. Increased usage, on the other hand, causes an increase in power needs, pushing the 12 V system power requirement excessively high and consequently harming overall system performance. To address this, the backplane voltage is increased to 48 V while the system power remains unchanged, minimizing the amount of current and copper traces required and reducing heat dissipated in the backplane. This change enhances overall system efficiency and reduces the need for a complex cooling system. This is the basis for the new Open Rack Version 3 standard, OCP ORV3.





The dependability of a data center is a fundamental operational necessity. Adding BBU to the system provides system redundancy. In the event of a power outage or brownout, the system needs time to notice the situation, preserve vital data, and move the operation to another data center server, most likely at a different data center facility and location. This must be accomplished in a seamless manner. Backup power systems are used in each rack to regulate the system's holdup power. This need is defined in the most recent standard, ORV3 BBU, as a 15 kW power output equal to 4 minutes of system operation per BBU unit, based on Li-Ion battery power storage and conditioning.

This specification provides Analog Devices with a guide to complete and engineer a reference design solution that incorporates its bidirectional power converter for single circuitry dedicated to charge and discharge operation, a battery management system (BMS) device, an on-board design system host microcontroller with firmware and GUI support, and hardware amplification through collaboration with the OCP organization.

Design Requirements and Hardware Implementation

As the OCP organization provides the specification (Revision 1.3), it will outline the requirements needed to conceptualize and design to meet the BBU module standard. The BBU module reference design is based on the ORV3 48 V proposal and consists of a battery pack with BMS, charger/discharger circuit, and other functionality blocks, as illustrated in Figure 2.



Figure 2. The OCP ORV3 BBU block diagram.

Aside from the circuitry requirement, the BBU module will need to have several major operation modes during its lifespan, and these are the following:

- Sleep mode: This is when the BBU module is in transportation or stock, or is not attached to an active busbar, which minimizes the cell discharge current for longer storage time. BBU monitoring or reporting is not available in sleep mode. The BBU will wake up and exit sleep mode when the busbar voltage is detected to be above46 V for > 100 ms and < 200 ms and PSKILL signal is low.</p>
- Standby mode: This is when the BBU module is fully charged and healthy, and constantly monitoring busbar voltage to be prepared for a discharge event. The BBU module operates in this mode for the vast majority of its lifespan. BBU modules' status and parameters are visible on the upstream rack monitor through the communication bus.
- Discharge mode: This is when the busbar voltage drops below 48.5 V for > 2 ms, BBU module discharge mode is activated. The BBU module is expected to take over the busbar voltage within 2 ms with a backup time of 4 mins.
- Charge mode: This is when the BBU module enables its internal charger circuit to charge up its battery pack when all conditions are met. The charge current can be anywhere from 0 A to 5.5 A based on the previous depth of discharge of the battery capacity. It also allows the upstream system to override the charge

current through the communication bus. There should be a charger timeout control scheme based on the calculated charge current.

- State of health check (SOH) mode: This is when the BBU module routinely tests battery pack capacity through forced discharge of the battery pack. The BBU module shall perform the SOH test every 90 days to determine the battery's EOL status.
- System control mode: The BBU shall allow the upstream system to control charger/discharger operation through the communication bus.

In addition to BBU module operation requirements, OCP specifies the standard for battery pack capacity, battery cell type, and battery pack configuration. These are the following:

- Battery pack capacity: The BBU module can provide 3 kW backup power not more than 4 mins over a period of 4 years.
- Battery cell type: The BBU module should have a Li-Ion 18650 type with 3.5 V to 4.2 V cell voltage, a minimum of 1.5 AH battery capacity, and a 30 A continuous rated discharge current.
- Battery pack configuration: The BBU module would have a battery pack configuration of 11S6P (six cells parallel strings of 11 cells in series each string).

Also, the BBU module is required to have a BMS for battery charge/discharge algorithms, protections, control signals, and interfaces for communication. The BMS is also responsible for having a cell balancing circuit where the cell voltage on the battery pack is maintained within $\pm 1\%$ (0.1 V).

The reference design block diagram (see Figure 3) shows selected parts and integrates various elements designated for certain tasks and constructs circuitry capable of delivering uninterruptible power, determining module health, fault, and module communications. The LT8228, a bidirectional synchronous controller, is housed within the BBU module. This device offers power conversion in the case of a line power interruption and battery charger during nonfault operation. The LT8551, a 4-phase synchronous boost DC-to-DC phase expander, works in tandem with the LT8228 to increase discharge power capacity delivery to 3 kW per BBU module. Aside from power conversion ICs, the BBU module incorporates the MAX32690, an ultra low power Arm® microcontroller, responsible for overall system operation. The LTC2971, a 2-channel power system manager, is used for precision sensing and fault detection of the power path, as well as a crucial voltage droop function. The MAX31760, a precision fan speed controller, was used to perform system cooling during charge and discharge operations. An EEPROM acts as data storage, allowing the user to recover any usable data on the BBU module during its serviceable time. In addition to the power converter and housekeeping microcontroller, a BMS IC was included in the design. The ADBMS6948, a 16-channel multicell battery monitor, is used for battery voltage level monitoring, while its inherent coulomb counter was employed to determine the state of charge (SOC) and the SOH levels for cell balancing and battery life expectancy calculation. The battery health status monitoring procedure is done by the MAX32625, an ultra low power Arm microcontroller. Both microcontrollers are carefully selected to lower total power consumption and thus extend battery life during BBU sleep mode operation.

Aside from the provided parts, this reference module also produces and constructs the BBU module (see Figure 4a) and BBU shelf (see Figure 5) to house and demonstrate the reference design in line with the OCP ORV3 BBU module and shelf mechanical specifications. The BBU shelf includes six slots for the BBU module, therefore a single BBU shelf may offer backup power of up to 18 kW as needed.



Figure 3. An Analog Devices OCP ORV3 BBU block diagram.



Figure 4. (a) A 3D rendered mechanical overview of an ADI BBU module and (b) airflow simulations.

Mechanical rendering and airflow simulation are two of the architectural benefits of the BBU module reference design. First, visualization that allows for accurate and appealing representations is included. Mechanical-structural analysis identifies design problems and potential changes early on, which helps the whole design process. Last but not least, it can decrease the need for actual prototypes, which can be time consuming and expensive. Furthermore, airflow simulation can give performance analysis, assist in identifying potential concerns, and increase design efficiency. It also handles thermal management by assisting in the identification of hotspots, optimizing heat loss, and enhancing overall system reliability. Furthermore, planning battery pack spaces for safety and compliance aids in risk reduction. See Figure 4b for more information.



Figure 5. A 3D rendering of an ADI BBU shelf with six inserted BBU modules.

Data and Results

The test findings presented below comprise steady-state performance measurements, functional performance waveforms, temperature measurements, and operation transition. The following configurations were tested using the BBU module reference design:

Table 1. ORV3 BBU Module Parameters

Discharge Operations (Boost Mode)	Charge Operation (Buck Mode)
Input voltage: 30 V to 44 V	Input voltage: 49 V to 53 V
Output voltage: 47.5 V to 48 V	Output voltage: 48 V
Output load: O A to 63.2 A	Output load: 0 A to 5 A
Switching frequency: 150 kHz	Switching frequency: 400 kHz

Performance Data

Efficiency and Power Loss

The BBU module reference design demonstrates the capability to outperform the efficiency and power loss specified constraints in the ORV3 BBU specification. The discharge and charge limitations were set at 97% and 95%, respectively. For the period of discharge operation, the measured average efficiency at the half-load (31.6 A) was 98.5% while the average efficiency at the full load (63.2 A) was 98%. With the influence of a substantially larger inductor, lower MOSFETs drain-to-source on-resistance, and a carefully selected switching frequency would provide high efficiency and reduced ripple current. Furthermore, the BBU module achieves a high average efficiency of 97% during charge operation with a 5 A load. Running at (400 kHz) switching frequency while using the same inductor value, efficiency was increased, and power loss was minimized. High efficiency and lower power losses will extend the battery life cycle and lessen the fan speed required for thermal cooling. See Figure 6.

On the other hand, conduction losses for control and sync MOSFETs contribute to the overall power losses during BBU discharge and charge operations.



Figure 6. Efficiency and power loss during discharge and charge modes of operation, respectively.

Charge Operation Efficiency and Power Loss



Output Voltage Droop

Another requirement from the ORV3 BBU specification was the inclusion of a voltage droop during discharge mode operation. Voltage droop is the deliberate loss of the BBU backplane voltage while driving system load. The BBU backplane voltage will alter in real time in response to the measured system load current using the LTC2971 in-circuit DAC. As a result, the backplane voltage droop from no load to full load stays below the ±1% limit required by the ORV3 BBU. See Figure 7.

Discharge Operation Output Voltage Droop



Figure 7. An output voltage droop during discharge mode of operation.

Switching Waveforms

Examining switching waveforms provides valuable information for performance evaluation, fault analysis, efficiency optimization, EMI reduction, and safety considerations. It enables engineers to identify and resolve issues, optimize system performance, and ensure the reliable and efficient operation of the BBU module in the data center.

The switching operation of the BBU module is critical during discharge mode operation, converting 30 V to 44 V battery pack voltage to 48 V backplane voltage. This is accomplished by using a synchronous power MOSFET that is precisely regulated by the LT8228 pulse-width modulation (PWM) signal and accompanied by the LT8551, which repeats the LT8228's action. The switching frequency and current sharing of each phase, which results in stepped-up voltage, are important to its operation. Switching waveforms of the main converter and its multiphase expander at full load are shown in Figure 8. In charge mode operation, the bidirectional converter operates in a single phase, stepping down the 49 V to 53 V backplane voltage to 44 V to charge the battery pack. It works by rapidly switching the synchronous power MOSFET and ramping the inductor current. The switching waveform of the bidirectional converter at a 5 A load is shown in Figure 9.



Figure 8. Main controller and expander switching waveforms during discharge mode of operation running at 44 V input and 63.2 A output load.



Figure 9. A main controller waveform during charge mode running at 53 V input and 5 A output load.

Thermal Performance

Thermal performance and efficiency must be carefully balanced. While it is critical to have a BBU module that can withstand high temperatures and continue to work without overheating, it is also important to have a BBU module that can operate at optimum efficiency, converting as much of the input power as possible into output power. In Figure 10, the board's worst temperature measured was only 40°C to 60°C during the discharge mode of operation, which ran at full load for around 4 minutes. In charge mode, the temperature on synchronous MOSFETs was less than 50°C. A properly built air-cooling system reduces component emitted temperature and prevents thermal runaway. Proper design of cell-to-cell gaps in the battery stack and an adequate design for air flow provide sufficient thermal cooling. See Figure 11.

Transition of Operation

The transition operation of a BBU module is critical in ensuring an uninterrupted power supply during power interruptions or variations. This procedure comprises the flawless transfer of battery pack energy to the backplane of a data center, ensuring that vital systems and devices stay functioning for 4 minutes. The BBU module constantly monitors the backplane busbar voltage. When the busbar voltage falls to the BBU module activation level of 48.5 V for 2 ms, the BBU module backplane voltage must ramp up to give full power to the busbar within 2 ms. The busbar voltage must never drop below 46 V throughout the transition. After detecting that the busbar voltage is more than 48.5 V for more than 200 ms, the BBU module quits discharge mode operation. See Figure 12.



Figure 10. Board thermal performance running at full load during discharge and charge modes of operation, respectively.



Figure 11. A battery stack gap design.



Figure 12. Transitioning of operation from stable to having a power interruption.

Summary

Data centers are moving toward 48 V systems in order to save energy. The 48 V server rack is more efficient in terms of power and heat dissipation, size, and cost than the 12 V server rack due to lower current, copper losses, and power busbar sizing. A front-end unregulated, high efficiency stage followed by a voltage regulator tuned to the appropriate load is best suited to data center server microprocessors and memories. Such levels of thought, as well as the latest innovation from 0CP, pave the way for more efficient power distribution and smart battery backup unit design to support continuous and flawless operations.

Choosing and implementing the proper device for the BBU module and shelf simplifies the overall design, extends the battery lifetime cycle, reduces the long engineering development lead time, and minimizes engineering and production costs. Furthermore, offering mechanical simulations shortens the prototyping step, offers data that may be used to improve thermal cooling and management, and boosts design assurance. Finally, supplying an appropriate and well-designed firmware algorithm and sequence ensures smooth and effortless BBU operation.

Part 2 of this series will go over the various BBU modules' major microcontroller functions and operations as it relates to the specialized design for BBU housekeeping. Furthermore, it will provide a more in-depth overview of how useful information is monitored and used to build and execute a correct workflow routine.



About the Author

Christian Cruz is a staff applications development engineer at Analog Devices, Inc., Philippines. He holds a bachelor's degree in electronics engineering from the University of the East in Manila, Philippines. He has more than 12 years of engineering experience in the field of analog and digital design, firmware design, and power electronics, which includes power management IC development as well as AC-to-DC and DC-to-DC power conversion. He joined ADI in 2020 and is currently supporting power management requirements for cloud-based computing and system communications applications.



About the Author

Gary Sapia received his Bachelor of Science degree in engineering from Texas A&M University, with advanced technology courses in power electronics and RF system design. He has over 28 years of experience focused on the design and development of analog systems, including power conversion and high frequency solutions for the communications and GPS markets. Prior to joining Analog Devices, Gary spent 18 years as a field applications engineer at Linear Technology (now part of ADI), focused on Cisco and other prominent Bay Area networking companies.



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Marvin Neil Solis Cabueñas graduated with a bachelor's degree in electronics engineering from De La Salle University in Manila, Philippines. Before joining ADI in 2021, Marvin worked as a systems engineer for Azeus Systems Philippines, Inc., then worked as a network engineer for Technistock, Philippines, Inc. from 2014 to 2017, and as a research and development engineer for Nokia Technology Center Philippines from 2017 to 2020. He has more than ten years of work experience in different fields such as embedded systems programming, digital signal processing, simulation modeling, and others. He currently works as a senior software systems engineer working on various projects for the Power Business Unit of ADI. He is currently working toward his master's degree in electrical engineering at the University of the Philippines.



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