Vol 57, No 4—October 2023

ANALOG DEVICES
AHEAD OF WHAT'S POSSIBLE™

AnalogDialogue

SPICE vs. IBIS: Choosing the More Appropriate Model for Your Circuit Simulation

May Anne Porley, Applications Engineer,
Jermaine Lim-Abrogueña, Systems Integration Engineer, and
Mar Christian Lacida, Product Applications Engineer

Abstract

As circuit simulation continuously gains popularity in the prototype industry, simulation models can be one of the critical requirements for broad and end market customers. SPICE and IBIS models are two of the most requested simulation models and can provide cost savings in the prototyping stage of circuit board development. This article differentiates SPICE from IBIS modeling systems and the significant impact of testing prior to circuit board fabrication. The article will discuss which model to use depending on the circuit design. It will examine sample use cases and commonly used simulation tools such as LTspice® and HyperLynx®.

Introduction

Behind this digital age where fast-paced advances in technology are evident, electronics manufacturers continuously develop essential components and tools that the industry needs to support this digitalization trend. In the simulation world, this means the availability of models that designers could use in their system design verification to ensure the functionality of their designs once board development commences. Two of the common simulation models mostly used in testing a design before fabrication are the SPICE and IBIS models. Although these are both behavioral models by nature, there are recommendations as to when they are to be used in simulations.

Benefits of Using Simulation Models

In general, simulation models aid system designers in simulating circuit design prior to prototyping. In using IBIS and SPICE simulation models, the goal is not just to simulate, but also to uncover any issues related to signal integrity up to circuit design performance. These issues are more often caused by the characteristics of board design including the traces or could be as simple as component functionality.

An IBIS model does not only represent the clamping behavior and driving strength of the components, but it also represents the impedance of the digital input/output (I/O) buffers, including the driver and/or receiver's output and input impedances. These are not directly stated in the model, but they are already implicit in the I-V data that represents the components' behaviors. Buffer impedances are significant to determine during simulations, as these are key to resolving signal integrity issues such as crosstalk and reflections. Crosstalk is an unwanted signal interference that happens when the signal traveling on one trace couples with the signal traveling on the other trace. On the other hand, reflections are one of the most common problems encountered during signal integrity simulations prior to board fabrication, and these are known to occur when there is a mismatch between the input or output buffer's impedance and the trace's characteristic impedance. Ideally, signals that enter the device and travel along the trace should reach the other end of the trace without any interference. But in reality, this scenario doesn't usually happen. Because of the impedance mismatch, signal integrity is affected. During reflection occurrence, what normally happens is that a portion of the signal that propagates along the transmission line will reach the other end, and a portion of this signal goes back. One of the strategies to address this issue is to add a termination to the buffers. Designers leverage the IBIS model's impedance feature to compute for the series or shunt resistors necessary to be used for termination, to match the impedances between the pin and transmission line, and to address signal reflections.

The SPICE model plays a significant role in utilizing time and money efficiently by predicting circuit behaviors so possible issues can be seen, considered, and resolved prior to prototype build to expect enhanced circuit performance. Cost and speed are two of the key benefits of SPICE model simulation. That is to avoid circuit errors early in the process, which could lead to costly and time-consuming prototype reworking and component reordering and resoldering. Simulation

models nowadays are more advanced and can provide accurate component performance approximations. Designers may easily swap components to evaluate circuit designs with varying bills of material (BOMs). At the same time, designers don't have to spend more time prototyping circuits components and later resolder once a prototype error has occurred.

Background

What Is a SPICE Model?

SPICE is an acronym for Simulation Program with Integrated Circuit Emphasis, a general-purpose circuit simulator that takes a text netlist describing the circuit elements (transistors, resistors, and capacitors) and their connections and translates them into mathematical equations using nodal analysis and solves them. In relation, a SPICE model is a text-based behavioral model that is used by SPICE simulators to mathematically predict the behavior of a device under varying conditions.

What Is an IBIS Model?

IBIS is an acronym for Input/Output Buffer Information Specification. It is a behavioral model that describes the analog behavior of the digital input and output buffers of a device. It consists of tabular data that describes the current-voltage (I-V) relationship of the components within the digital buffers, as well as the voltage across time (V-t) switching characteristics of the output or I/O buffers. It is used for the signal integrity analysis of system boards prior to fabrication and is presented in plain ASCII-text formatted data. It does not disclose any proprietary information since IBIS models are like a black-box model, which does not contain internal information that can be reverse engineered.

Overview of the Models

What Do They Look Like?

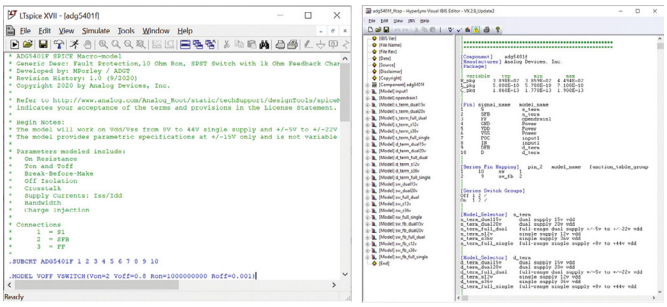

Figure 1. A SPICE file (.cir) on the left using LTspice and IBIS file (.ibs) on the right using Siemen's HyperLynx.

Both IBIS and SPICE models are text-based behavioral models as shown in Figure 1 where contents can be viewed using a simple tool such as notepad. However, for more convenience in going through the model, it is recommended to use Cadence Model Integrity or Siemen's HyperLynx to view an IBIS file. On the other hand, a SPICE model can be opened and installed to a wide range of SPICE simulation tools such as LTspice, NI Multisim™, OrCAD® PSpice®, or other SPICE simulators.

Both SPICE and IBIS models are non-executable files and are text-based description files. Both models mostly consist of three main parts:

- Header file: provides a brief description or general information about the model, the device, revision history, notes specific to the model, and the company or brand of the device being modelled.
- Model name/title: basically mentions the device name, pinout and/or pin-to-buffer mapping. A dot subcircuit <space> model name (.subckt ADGxx) <space> pinouts line is used in SPICE. While for IBIS, it is in terms of [Component] ADGxx.
- Model structure: a text-based representation of the model. SPICE models consist of different blocks exhibiting each parameter of a device including pin functions that may be composed of primitive and native components such as capacitors, resistors, diodes, voltage, and current sources. On the other hand, IBIS models consist of I/V and V/T data table modeling each digital I/O buffer.

Where to Find Them?

SPICE and IBIS models are mostly located on individual semiconductor company web pages. Semiconductor manufacturers today develop their simulation models to represent their products and, at the same time, maintain the model's inclusion, content, accuracy, and model support. Analog Devices' website offers a wide selection of SPICE and IBIS models of ADI products as shown in Figure 2.

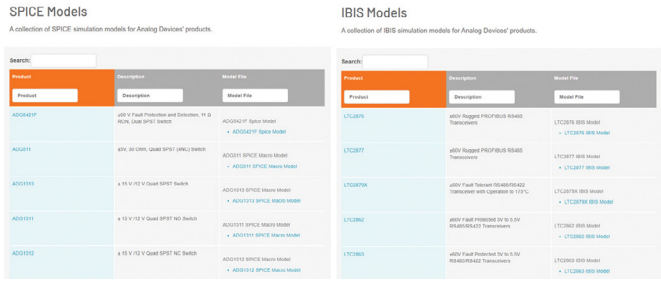

Figure 2. A wide selection of SPICE (left) and IBIS (right) models taken from ADI's website.

Other SPICE models can be found inherently in the library of the manufacturer's SPICE simulator. Figure 3 shows the switches library of LTspice that covers most of ADI's switch products. For an easier simulation approach, it would be beneficial to choose a SPICE simulator that has an available wide range of SPICE model libraries.

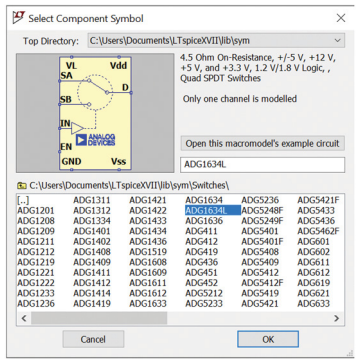

Figure 3. A sample of an intensive library of SPICE models in LTspice.

Supplementary Files

Both SPICE and IBIS models need an accompanying file called a symbol in order to be used in a simulator. IBIS models usually come in the form of text-based representation data, but to simulate them using electronic design automation tools, they are placed into a symbol where external components are connected. Similar to IBIS models, SPICE models also need a symbol file that is usually in a dot symbol (.asy) format, which must be installed simultaneously to the SPICE simulator library. Once both model and symbol have been added/set up to the library, the

designer may now use the model in their circuit simulation. Figures 4 and 5 show an example of symbol files used in IBIS and SPICE models.

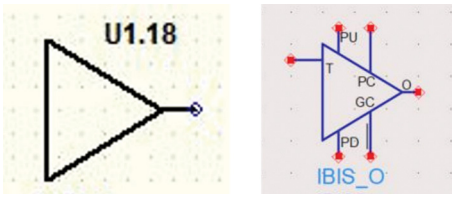

Figure 4. An IBIS symbol for output buffer using HyperLynx (left) and Advanced Design System (right).

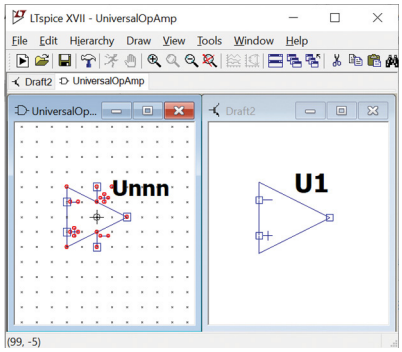

Figure 5. A SPICE symbol file (right) template of a simple 3-pin operational amplifier and its equivalent symbol (left) used in a circuit simulation in LTspice.

For both IBIS and SPICE, symbol files are not provided by the manufacturers, but most simulators have available template symbols that may be used depending on the number of pinouts or device type. In addition, for SPICE, symbol files can also be generated automatically, and this functionality depends on the SPICE simulator.

Model Comparison

SPICE Models

In general, SPICE models replicate the behavior of a component including its pinout, pin configurations, functionality, and other operations. These models do not have a standard architecture, but the goal is to create an architecture that accurately replicates an expected behavior performance of a component including its pin functions. The model may consist of passive components such as resistors, capacitors, diodes, and transistors, which when designed accordingly create the target component behavior. One note to remember is since SPICE models accurately replicate the behavior of a component, they may contain complex circuitry that may result in to slow simulation cycle. SPICE models can range from a simple one-line text describing a passive component like a resistor, to a more complex circuit and subcircuits that can be hundreds of lines long.

SPICE models, as mentioned above, can be opened using a text-based tool but for most recent SPICE simulators, an equivalent schematic representation can be viewed for much easier circuit analysis as shown in Figure 6 where a three-amp state variable filter can also be converted into an equivalent text netlist describing the circuit elements and its connections.

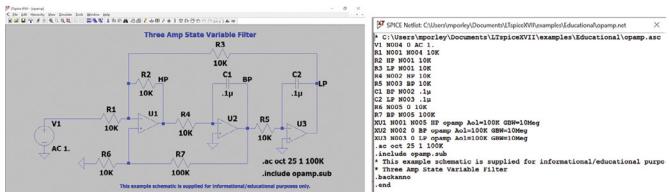

Figure 6. A three-amp state variable filter sample SPICE model.

In terms of model performance, a rule of thumb for a SPICE model is to provide close behavioral performance in comparison to the device data sheet's specifications and functions. For example, a switch SPICE model should have on-resistance and timing parameters, while an amplifier is most likely to have gain bandwidth and input offset parameters. In relation, the model functions and specifications must be close to or within the typical to minimum or maximum values provided in the data sheet.

IBIS Models

Generally, an IBIS model follows a standard architecture in representing a digital I/O buffer. This is done through IBIS keywords representation that is used to describe each digital buffer's components as shown in Figure 7. These IBIS keywords appear in the form of V-I lookup data tables as well as V-t lookup data tables.

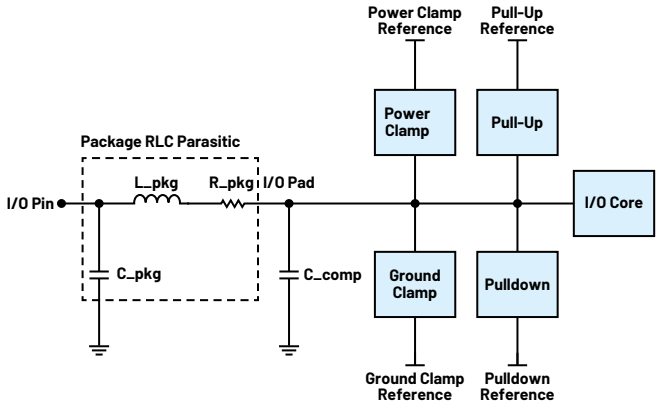

Figure 7. An IBIS block diagram of a typical I/O buffer.

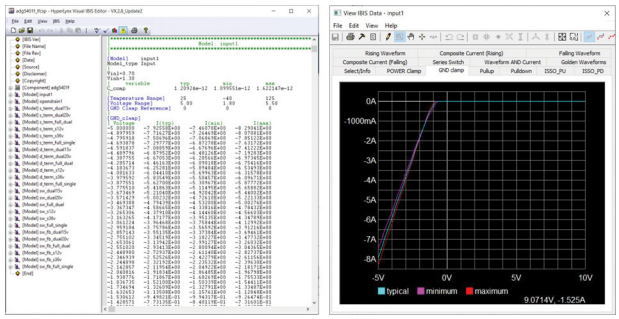

Figure 8. The ADG5401F's V-I data for an IBIS keyword (left); plotted V-I curve (right) using Siemen's HyperLynx.

Figure 8 on the left shows an example of how V-I lookup tables look in an IBIS model, and on the right shows the waveform when this V-I lookup table is plotted using Siemen's HyperLynx. It is a series of current measurements taken under a set of voltage ranges, usually from $-V_{DD}$ to twice the V_{DD}, to represent the behavior of a particular IBIS component in three conditions—typical, slow, and fast corners. This is done by varying the process corners, operating voltage, and operating temperature of a device. These tables are used to represent the clamping protection components of the receiver in the form of [Power_clamp] and [GND_clamp] keywords, as well as the driving strength of the I/O buffers in the form of [Pullup] and [Pulldown] keywords. These 4 V-I keywords are represented separately in the model since both the receive mode and the drive mode are necessary for signal integrity simulations.

V-t tables, on the other hand, represent the driver's switching characteristics in the form [Rising_Waveform] and [Falling_Waveform] when transitioning from one state to another, taken when the load is in reference to V_{DD} and ground. It also contains the slew rate of the I/O buffer, under the IBIS keyword [Ramp], taken at 20% to 80% of the transition edge. These waveforms and the ramp data describe how fast the driver components turn on or off with respect to time.

Although these keywords are represented separately in the model, when used during simulations, the electronic design automation simulation tools combine these V-I and V-t data to construct a buffer model based on their operating region, and it will be used to perform signal integrity simulations and timing analysis of printed circuit boards.

In addition, IBIS models also contain the RLC pin and/or package parasitic values of the device, and the buffer capacitance (C_Comp) for each I/O buffer. C_comp is the capacitance seen from the pad back to the buffer and does not include the package capacitance.

To know more about the V-I and V-t data tables or keywords found in an IBIS model, you may refer to the previously published article entitled "IBIS Modeling—Part 1: Why IBIS Modeling Is Critical to the Success of Your Design."

Simulation Tools

There's a wide range of industry-standard SPICE and IBIS simulators that provides design simulation for most high speed design systems and analog and mixed-signal circuits both for professionals and education. SPICE simulators usually generate nodal equations based on the connections/nodes of the circuit and then try to solve the current and voltage values at the respective nodes. IBIS simulators, on the other hand, refer to the V-I and V-t lookup data tables presented in the model to predict the output behavior of a signal. Commonly used simulators in the industry are:

IBIS Simulators

- Siemen's HyperLynx is an electronic design automation tool that is used for analyzing signal integrity, power integrity, electrical design rule checking, and electromagnetic modeling in high speed electronic designs. This tool can be used in viewing, editing, and simulating with IBIS models.
- Keysight's Advanced Design System is an electronic design automation tool that is used for various design processes such as frequency and time domain circuit simulation, schematic design and layout, design rule check, and electromagnetic field simulations. This tool is commonly used for IBIS model simulations.

SPICE Simulators

- LTspice® is high performance SPICE simulator software that includes a graphical schematic capture interface. Schematics can be probed to produce simulation results with a built-in waveform viewer. This SPICE simulator's graphical user interface (GUI) was based on a statistical analysis of the keyboard entry and mouse motion required to enter a schematic, which can be more interactive in comparison to other SPICE simulations. LTspice includes an extensive library of SPICE models covering most of ADI's products and signal chain products, as well as a library of passive components.
- NI Multisim has an interactive schematic environment to instantly visualize and analyze electronic circuit behavior. This simulator has a virtual oscilloscope, digital multimeter, and other bench equipment that makes the circuit simulation experience close to a typical engineer's bench evaluation environment.
- OrCAD PSpice Designer combines schematic entry, native analog, mixed-signal, and analysis engines to deliver a complete circuit simulation and verification solution. Whether you're prototyping simple circuits, designing complex systems, or validating component yield and reliability, OrCAD PSpice technology provides the best, high performance circuit simulation to analyze and refine your circuits, components, and parameters before committing to layout and fabrication.

IBIS Model and SPICE Model Use-Case

IBIS Model

IBIS models usually come in the form of text-based representation data, but to simulate them using EDA tools, they are placed into a symbol where external components are connected. Simulators will then use the data incorporated in the model to analyze and predict buffer behaviors in a given situation.

Siemen's HyperLynx and Keysight's Advanced Design System already have the IBIS symbols that designers can use in their simulations. Figure 9 will show how these symbols are shown in these tools.

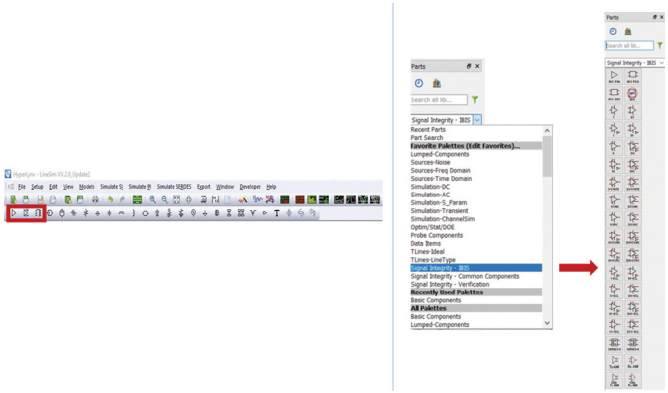

Figure 9. HyperLynx toolbar showing symbols for a single-ended buffer, differential buffer, and IC component that can be used for IBIS model simulations (left); Advanced Design System toolbar showing symbols for different types of buffers that can be used for IBIS model simulations (right).

- In HyperLynx, when simulating single-ended input or output buffers, one may use the first highlighted buffer on the left figure, then load the IBIS model in it and choose the specific buffer to be simulated. The tool will automatically

show an output buffer if an output buffer model is chosen. Otherwise, if an input buffer is to be simulated, the tool will automatically convert the symbol into an input buffer symbol.

- In Advanced Design System, the palette for Signal Integrity–IBIS will show various types of buffer models. If an open drain output is needed, one must choose the symbol labeled OSNK, or if a terminator is to be simulated, the symbol labeled T must be used in simulations. Note that if the wrong symbol is chosen, this may lead to an error. For example, when an input buffer is needed but an output buffer symbol is placed in the schematic, one won't be able to see the available input buffer pins modeled in an IBIS because the simulator will only allow output buffer pins to be loaded in the symbol.

One of the applications of IBIS model simulations is resolving unwanted signal behaviors that are usually caused by an impedance mismatch between the buffer and the PCB trace that functions as a transmission line. As an example, consider the schematic simulation using HyperLynx in Figure 10.

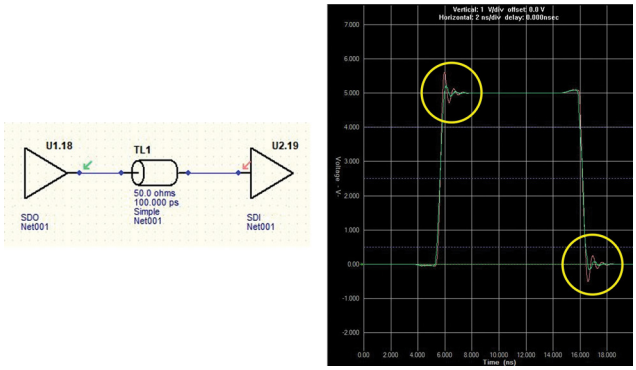

Figure 10. An unterminated schematic (left) and its corresponding results (right).

Figure 10 shows an unterminated output buffer simulation using a 50 Ω trace that yields unwanted overshoot and undershoot signals. This can be addressed by adding a series termination resistor to match the impedance between the buffer and the trace. But before doing this, the output buffer's impedance must first be determined.

V-t tables found in an IBIS model, [Rising_Waveform] with respect to ground and the [Falling_Waveform] with respect to V_{DD}, can be used to compute the buffer's output impedance since this parameter is already innate in the data represented in the model. Using the voltage divider theorem, one can derive the buffer impedance value, and use this to compute the appropriate terminating resistor that needs to be added to the model to match the impedance between the buffer and the trace. This will help solve the impedance mismatch and eliminate the unwanted overshoot and undershoot in the signals.

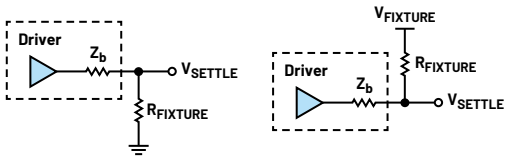

Figure 11. A schematic reference for the voltage divider.

Figure 11 shows the schematic for the voltage divider where Z_b is the buffer impedance, R_fixture and V_fixture which are found in the model, while V_{SETTLE} is the voltage where the V-t waveforms settled.

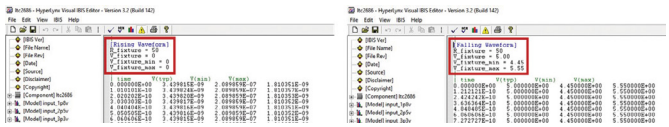

Figure 12. An IBIS model showing the fixtures used in extracting V-T lookup tables: rising waveform (left) and falling waveform (right).

Once the terminating resistor value has been determined, this should be added to the schematic.

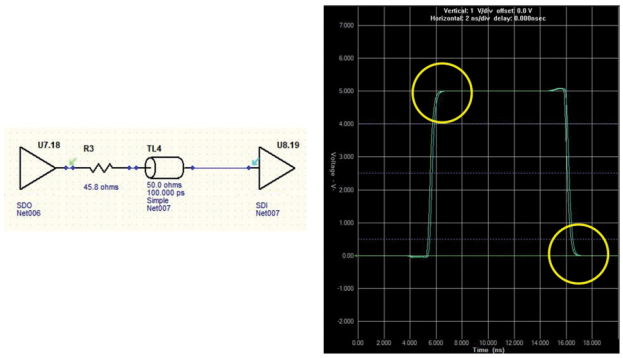

Figure 13. A terminated schematic (left) and its corresponding results (right).

Figure 13 shows the terminated schematic and its corresponding results where the initial overshoot and undershoot have already been addressed.

The method discussed above is just one of the strategies that can be taken to compute the buffer impedance and resolve mismatched impedance concerns. There are also other methods such as using the IBIS model's pulldown V-I table and performing load line analysis to identify the operating point. From there, output impedance can be derived as well as the value for the series terminating resistor.

SPICE Models

Figure 14 shows a sample SPICE simulation using the ADG1634L model in transient analysis. The designer can evaluate the performance of the ADG1634L (in this example) and simulate it to check the timing and other functions of the device in which plot results will be shown in the time domain. The transient analysis predicts the behavior of the components throughout a specified timeframe. SPICE models can also be simulated in different analysis types such as DC analysis and AC analysis. DC analysis calculates the voltage and current of a circuit based on a range of DC input values. AC analysis determines the phase and magnitude of the nodes in a circuit, which may be useful when trying to check circuit behavior in the frequency domain.

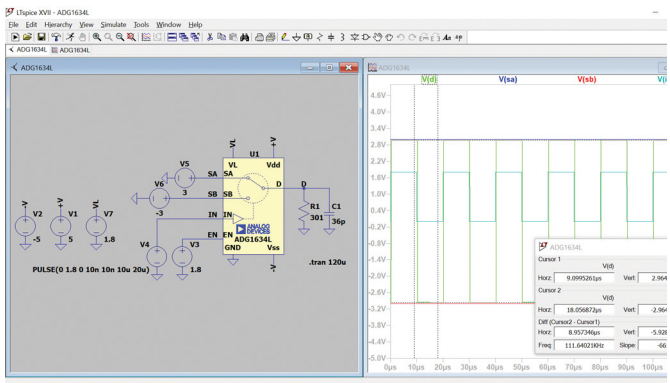

Figure 14. A sample SPICE simulation using the ADG1634L model.

Expanding this further, more complex circuit designs can be simulated in SPICE that determine the performance of the design. See the example in Figure 15.

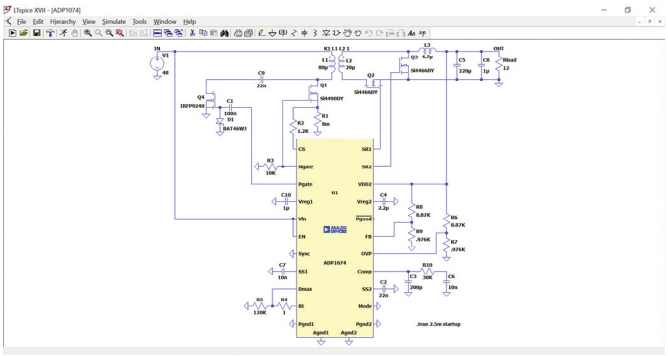

Figure 15. An example of a forward active clamp circuit SPICE simulation in LTspice.

Which Model Is Better for Your Simulation?

Here are some points to consider if the IBIS model could be most suitable for a circuit simulation:

- If a designer is looking for the behavioral characteristic of a digital I/O buffer such as buffer impedance, drive strength, rise time, or fall time
- When the component you are trying to evaluate is a digital component such as FPGAs
- For designs that are concerned with the signal integrity or possible transmission line errors of the digital I/O pins of a component when connected to a PCB trace

On the other hand, for circuit simulations that require a more complete component performance including its analog, digital, and supply pin functionality and its behavioral response when connected to multiple components in a circuit, it might be best to use SPICE models. Other key points to use SPICE models over IBIS models are:

- When trying to evaluate a component's functionality and its behavioral performance when used in a circuit
- When trying to evaluate the behavioral response of the component at different analyses and domains (time or frequency)
- For complex designs that require intensive nodal analysis and solve current and voltage nodes in a circuit

Conclusion

SPICE and IBIS models are gaining popularity in the industry because these models help design engineers verify the target circuit performance before and during prototyping, which provides cost and time-saving advantages. Both models are behavioral in nature. SPICE models, in general, replicate the behavior of a component including its pinout, pin configurations, functionality, and other operations. IBIS models mimic the device's digital I/O behavior using parameters in tabulated voltage-current and voltage-time information. To use the models, both SPICE and IBIS models need an accompanying file called a symbol to be used in a simulator. A SPICE model simulation predicts the performance of a component including its expected pin functionality and configuration, while an IBIS model simulation is often used for predicting the occurrence of signal integrity problems at the digital I/O pins such as impedance mismatch, crosstalk, reflection, undershoot or overshoot during PCB simulations. The choice of which model to use depends on the designer's purpose in using the model. For designs that are concerned with the signal integrity, drive strength, or possible transmission line errors of the digital I/O pins of a component when connected to a PCB trace, an IBIS model would be highly recommended. On the other hand, for circuit simulations that look for a component performance including its analog, digital, and supply pin functionality when used in a circuit, it is recommended to use SPICE models.

References

Alonso, Gabino. "Get Up and Running with LTspice." *Analog Dialogue*, Vol. 53, No. 4, December 2019.

Engelhardt, Mike. "SPICE Differentiation." *LT Journal of Analog Innovation*, January 2015.

Leventhal, Roy. "How to Use the IBIS Model." March 2014.

Leventhal, Roy and Lynne Green. *Semiconductor Modeling: For Simulating Signal, Power, and Electromagnetic Integrity*. Springer, 2006.

Lim, Jermaine and Keith Francisco-Tapan. "IBIS Modeling—Part 1: Why IBIS Modeling Is Critical to the Success of Your Design." *Analog Dialogue*, Vol. 55, No. 3, September 2021.

"Advanced Design System." Wikipedia, The Free Encyclopedia, May 2022.

"HyperLynx High-Speed Design Analysis & Verification." Siemens.

"IBIS Modeling Cookbook for IBIS Version 4.0." The IBIS Open Forum, September 2005.

"LTspice®: Schematic Editor." Analog Devices, Inc.

"LTspice®: Overview." Analog Devices, Inc.

"Why IBIS?" Advanced Micro Devices, Inc.

About the Author

May Anne Porley is an applications engineer at Analog Devices, Philippines, within the Automated Test Equipment (ATE) Group. She joined ADI in 2012 and provides applications support for switches, multiplexers, level translators, and unbuffered crosspoint switches portfolios. Moreover, May Anne led the development of SPICE models for the switches and multiplexers portfolio. She graduated from De La Salle University—Dasmariñas, Philippines, with a bachelor's degree in electronics engineering.

About the Author

Jermaine Lim-Abrogueña a systems integration engineer under Customer-Office Solutions—Asia Pacific, Japan and China's (COS-APJC) System Modeling and Simulations Group at Analog Devices. She joined ADI in October 2014, where her contributions focused on developing IBIS Models for various ADI products. She received her bachelor's degree in electronics engineering from Pamantasan ng Lungsod ng Maynila.

About the Author

Mar Christian Lacida is an applications engineer at Analog Devices within the Automated Test Equipment (ATE) Group in Cavite, Philippines. He joined ADI in 2018 and provides applications support and LTspice model development for the switches and multiplexers portfolio. He graduated from the Polytechnic University of the Philippines-Sta. Mesa, Manila, with a bachelor's degree in electronics engineering.