Vol 58, No 2—June 2024

ANALOG DEVICES | ADI Analog Dialogue™

Phase Matching in Between Isolated Condition Monitoring Channels: A DAQ μModule Application

Malcolm Leeland Kwok, Product Applications Engineer

Abstract

Condition monitoring systems that are capable of simultaneously capturing data across multiple sensors typically use a channel-to-channel isolated solution to eliminate ground loops. While board-level discrete signal chains are faced with high channel-to-channel phase mismatch errors due to component tolerances, Analog Devices' precision signal chain μModule® solutions achieve minimal phase mismatch with the use of ADI's integrated passives (*i*Passives™) technology.

Introduction

Condition monitoring (CM) systems play a crucial role in various industries, from manufacturing and aerospace to healthcare and infrastructure. These systems help detect and analyze various conditions, ensuring the safety, reliability, and performance of assets and machinery. One of the main parameters being monitored is vibration, where the signal's amplitude, frequency, and phase contain an abundant amount of information on an asset's condition.

This article examines the importance of accurate phase measurement in a CM system and the challenges it faces in data acquisition (DAQ) involving multiple simultaneous sampling channels. A variety of traditional solutions are discussed, while introducing an innovative approach to set a new level of phase matching performance.

Architecture

CM systems consist of multiple sensors or transducers. Many systems use the centralized system architecture, each connected to a separate channel or input on a DAQ solution through analog cables.[1]

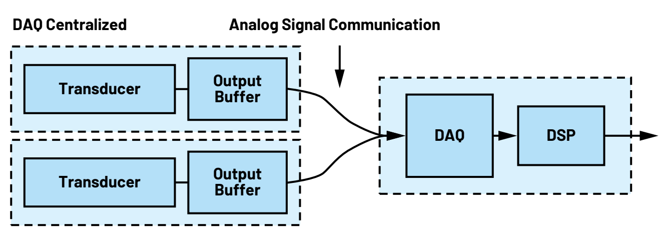

Figure 1. A centralized DAQ architecture.[1]

The sensors can be of various types, measuring parameters such as vibration, sound, and current. They can gather data across multiple points and axes on a single asset, or even simultaneously across separate assets.[2] The data from these channels are then processed to provide valuable insights into the system's behavior, such as predicting machine failures before they happen or anticipate maintenance needs before they become urgent.

Use Cases

Using a Multichannel Simultaneous Sampling ADC

The first use case is when a CM system uses phase analysis from two or more orthogonal sensors to monitor machine operation and anomalies, such as imbalance, misalignment, and loose footing. Instead of using a tachometer, the phase of one of the sensors can be used as the reference in determining the fault location.[3]

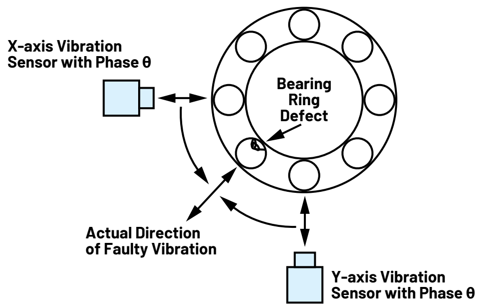

Figure 2. Application: Using phase analysis to determine type and location of fault.

In multi-axis sensing, postprocessing of time and frequency information relies on preserving a relatively constant time delay between signal capture. This translates into requirements of synchronized simultaneous sampling and channel-to-channel phase matching to preserve magnitude and phase (time) domain information for high performance. Otherwise, this would lead to less precise measurement of the phase angle between the sensors. Vendors of CM systems have phase matching specifications that go as low as 1° at 20 kHz, even including the delay and jitter from isolation circuitry.

For achieving this, using multichannel simultaneous sampling sigma-delta (Σ-Δ) ADCs, such as ADI's AD7768-4 or AD4134 can be convenient. See Table 1. Sigma-delta ADCs are preferred in CM applications over successive approximation register (SAR) ADCs due to their higher DC-to-100 kHz resolution and advanced filtering suitable for time and frequency domain analysis of vibration signals. For more information on this, refer to the article "Condition Monitoring System Design Choices and Their Impact on Signal Chain Implementation."[1]

Table 1. Phase Matching Performance and Phase Calibration Resolution across Various ADCs

	AD7768/AD7768-4	AD4134
Channel-to-channel phase matching at 20 kHz (max)	Not measured	0.024°
Phase calibration resolution at 20 kHz	0.88°	0.3°

However, phase mismatch errors can come from the signal chain when using discrete-time sigma-delta (DTSD) ADCs like the AD7768-4. Due to the inherent lack of alias rejection of DTSD ADCs at multiples of its sampling frequency, the system can be vulnerable to out-of-band interferences, which may corrupt the CM signals of interest. To improve rejection at these frequencies, its ADC driver stage is designed with an analog antialiasing filter (Figure 3), typically of third order or higher, while preserving minimal in-band magnitude error. For example, a second-order Butterworth filter designed for –80 dB rejection at 16 MHz (sampling frequency) and f3dB of 160 kHz (input bandwidth) could have a phase mismatch of ±0.15° at 20 kHz even with RC mismatch tolerances as low as 1%.[4]

This is not a problem for continuous-time sigma-delta (CTSD) ADCs, like the AD4134, since they do not have vulnerabilities outside its pass band, eliminating the need for an analog antialiasing filter. A key difference, however, is that DTSDs are more power scalable than CTSDs. Additionally, there may be other sources of latency, such as the input amplifier and isolation circuitry.

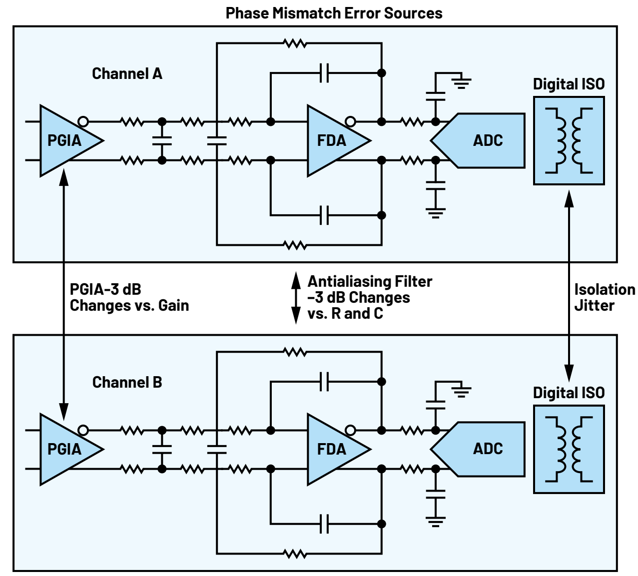

Figure 3. Phase mismatch error sources.

As a solution, both of these multichannel ICs have phase calibration registers to adjust each channel's phase (Table 1), given the knowledge of each channel's latency (more accurate than $1/F_{sampling}$, or around 0.5° at 20 kHz) across frequency and temperature. Overall, using a multichannel simultaneous sampling ADC is a generally sufficient solution, yet it has its limitations.

Ground Loops and the Need for Isolation

Consider simultaneously monitoring across different parts of a single machine, or even across different machines altogether. In this system, we need to have careful consideration of ground loops.

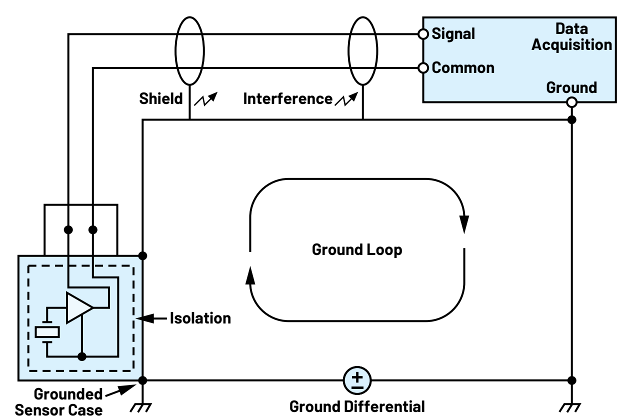

Figure 4. Improper grounding in an accelerometer installation.[5]

Grounding and shielding are used in instrumentation to protect measurement signals from unwanted noise and stray electromagnetic fields. The cable used to connect the sensor and the DAQ solution is usually a shielded twisted pair, where the shield is grounded from the sensor side, or from the DAQ side.

If, for example, (1) the sensor has a path to ground, (2) the DAQ has a separate one as well, and (3) the cable shield is grounded from both sides, it then forms a ground loop (Figure 4). A ground loop allows current to flow along the shield. Induced currents on the shield from power lines and nearby machinery can then couple the interference on the signal line. For proper grounding, there should ideally be only a single low impedance path to ground from any point in the system. Designing the grounding system requires consideration of the application, environment, and the sensor's type of isolation.

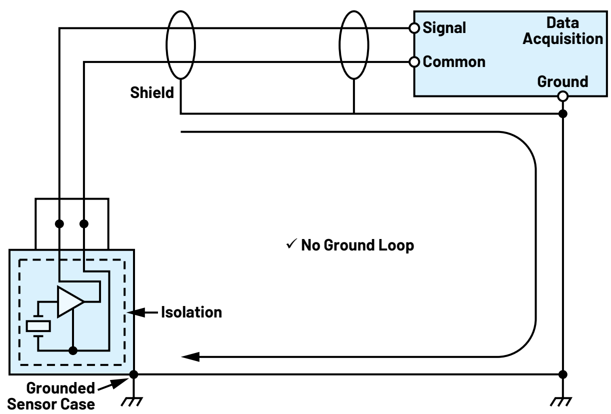

Figure 5. Proper grounding: Grounded at the instrumentation, isolated at the accelerometer.[5]

Accelerometers can be (a) case grounded, (b) case isolated, or (c) ground isolated.[6]

(a) A case grounded accelerometer has a path to ground when attached to a conductive surface. For a single-channel system, it requires only the DAQ to be isolated. For a multichannel system however, grounding multiple sensors will create a ground loop.

(b) To avoid this problem, it is then best to have isolated sensors and a grounded multichannel DAQ solution (Figure 5). Many accelerometers have basic case isolation, where the sensing element isolated from the sensor housing, typically through a coated pad.

(c) Others achieve ground isolation from the mounting surface using various techniques.

i. Adhesive mounting provides a varying level of isolation, depending on the thickness of the adhesive.

ii. Integral housing isolation and isolation mounts typically come at a higher/additional cost, but they may be necessary in hazardous environments, such as wind turbines exposed to lightning strikes.

To summarize, isolating the sensor while grounding the DAQ is a solution to the ground loop problem, but it may come at a higher cost.

Lower Cost, Isolating at the DAQ

To avoid the costs of isolating the sensors, a possible solution is to use multiple single-channel ADCs, like the AD7768-1, with isolation circuitry (Figure 7). To ground at the sensor side, the sensor case can be used as the grounding point. This makes the DAQ solution independently configurable, scalable, and applicable to a wider variety of use cases.

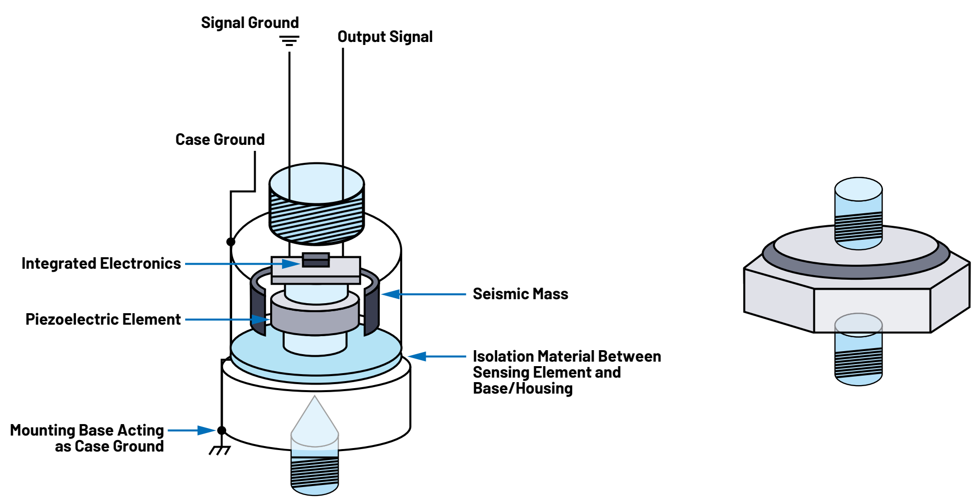

Figure 6. Case isolated accelerometer and an isolation base.[6]

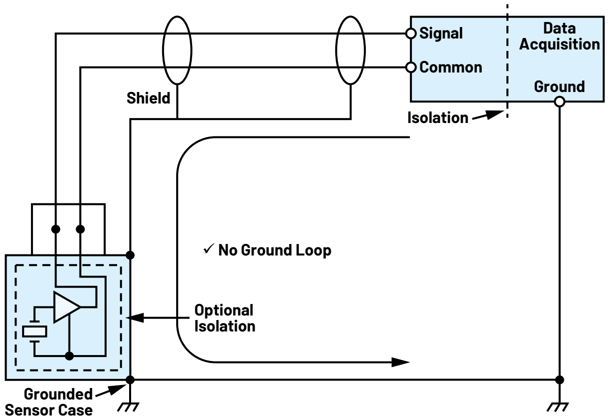

Figure 7. Proper grounding: Isolated at the instrumentation, grounded at the accelerometer.[5]

You may have realized it: This points back to the higher phase mismatch between channels, caused primarily by the analog AAF.

Without simultaneous sampling and phase calibration registers, the last resort to reduce phase mismatch errors is to calibrate them through timing. An FPGA can control the timing to start capturing data per channel, requiring high frequency clocks and phase/delay locked-loops. This adds much complexity to the DAQ solution.

The World of µModule Solutions

µModule solutions provide phase matching solutions at the package level.

Integrating the complete signal chain into a system-in-package (SIP) enables the µModule solution to provide a data sheet outlining the performance of the entire signal chain. While eliminating significant PCB assembly issues such as cold solders and bill-of-materials (BOM) availability, it has enhanced performance enabled by ADI's integrated passives (*i*Passives) technology, allowing customers to solve complex system-level challenges, such as phase matching.

ADI's ADAQ7768-1 single-channel µModule DAQ system suitable for CM applications includes a 36 V programmable gain instrumentation amplifier (PGIA), a fourth order active antialiasing filter (AAF), and a 24-bit DTSD ADC with the same features as the AD7768-1.

Utilizing an *i*Passives network for its fourth-order analog AAF, the ADAQ7768-1 is able to achieve a tight device-to-device phase matching performance, comparable to simultaneous sampling ADCs and their phase calibration resolution, as seen in Table 2 and Figure 9. Figure 10 illustrates how an *i*Passives network achieves its close matching from fabrication, expressing the difference in resistance through the color gradients. *iPassives* resistor tolerance can go below 0.1%, while temperature coefficient of resistance (TCR) can be matched less than 1 ppm/°C, translating to a tightly controlled RC filter bandwidth that is stable across temperature. With the use of *i*Passives network, µModule solutions solve the phase mismatch problem through the BOM and assembly approach, setting a new level of performance that is limited in traditional discrete signal chains.

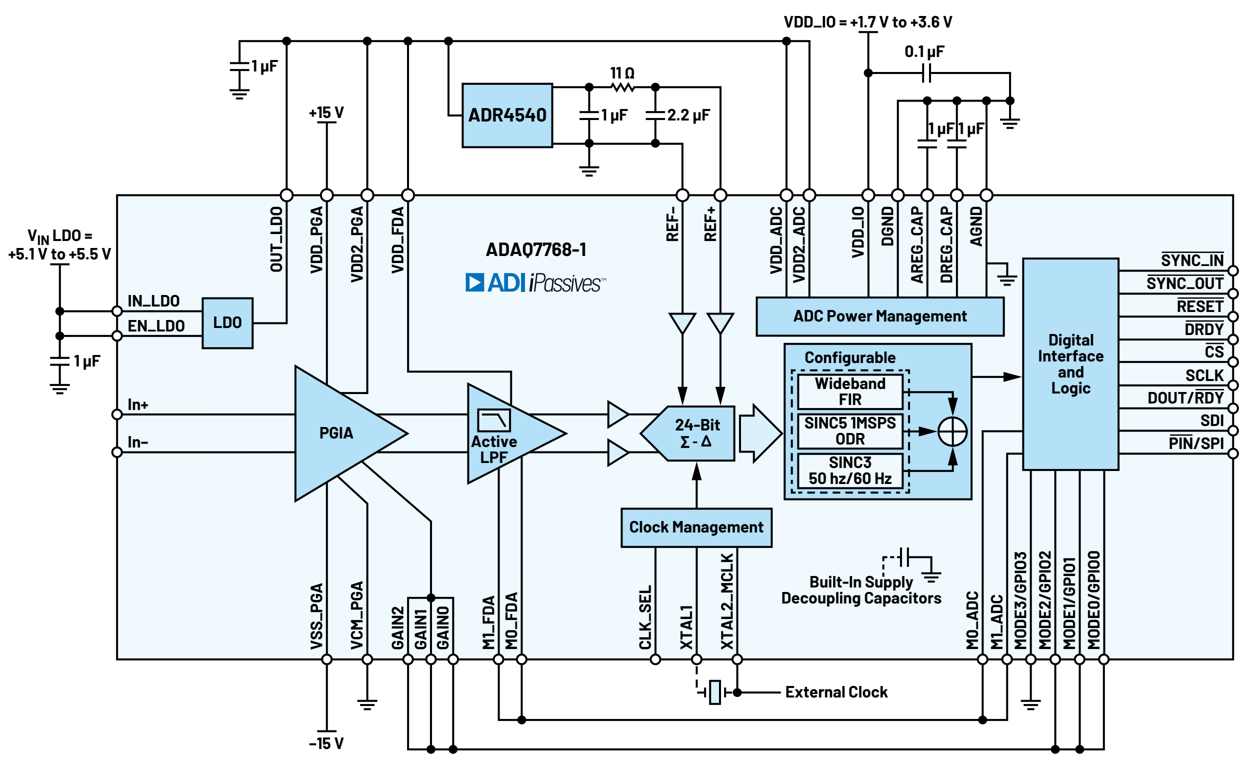

Figure 8. The ADAQ7768-1 functional block diagram.

Table 2. Phase Matching Performance and Phase Calibration Resolution Across Various ADCs Including Precision Signal Chain µModule Solutions

	AD7768/ AD7768-4	AD4134	ADAQ7768-1	ADAQ7767-1
Channel-to-channel phase matching at 20 kHz (max)*		0.024°	0.22°	0.20°
Phase calibration resolution at 20 kHz	0.88°	0.3°		

*ADAQ776x-1 Phase Mismatch Max = 6 sigma (Typ = ±1 sigma)

*Phase Matching = Phase Mismatch * 2

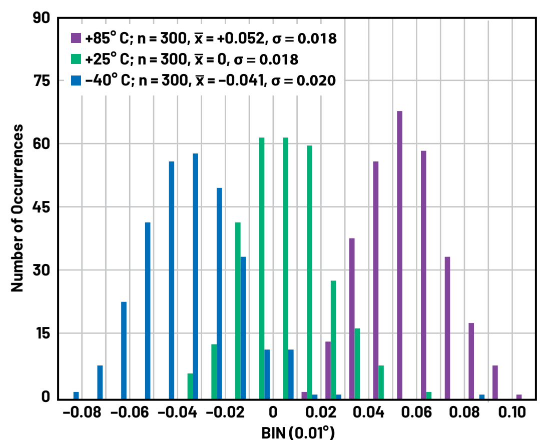

Figure 9. The ADAQ7768-1 device-to-device phase angle mismatch at 20 kHz across temperature, normalized to mean value at 25°C.

Generics and Distinction

There are other generics from the ADAQ7768-1 that use the same integrated ADC, namely the ADAQ7767-1 and the ADAQ7769-1 (Figure 11).

ADAQ7768-1

The ADAQ7768-1 includes a fully differential PGIA. With its high impedance and low input bias current, it connects directly to various sensors. Unlike a conventional voltage feedback amplifier, the integrated PGIA maintains nearly the same bandwidth across all its gain settings—leading to tight device-to-device phase matching regardless of the gain setting.

ADAQ7767-1

The ADAQ7767-1 does not provide an integrated input amplifier— lowering cost and enabling the customer to provide custom input signal conditioning. This device has three input ranges, with a maximum of ±24 V for single-ended inputs, allowing a DC-coupled IEPE sensor architecture and a simpler power solution.

ADAQ7769-1

The ADAQ7769-1 builds upon the ADAQ7767-1 by adding a single-ended programmable gain low noise amplifier. It is still capable of the ±24 V single-ended input range, allowing a DC-coupled IEPE sensor architecture with a more complete solution.

Implementing Synchronization

To obtain the full phase matching performance of these products, it is required that the device follows proper methods of synchronization. While there is a generic method of synchronizing various products, some devices have their own unique methods that are usually added as a benefit to the overall system.

Generally, in many SD ADCs, a SYNC or $\overline{\text{SYNC\_IN}}$ pin is provided to allow a controller to synchronize separate, and usually similar, ADCs with each other. In time-sensitive ADCs, this typically comes with the requirement to have the SYNC

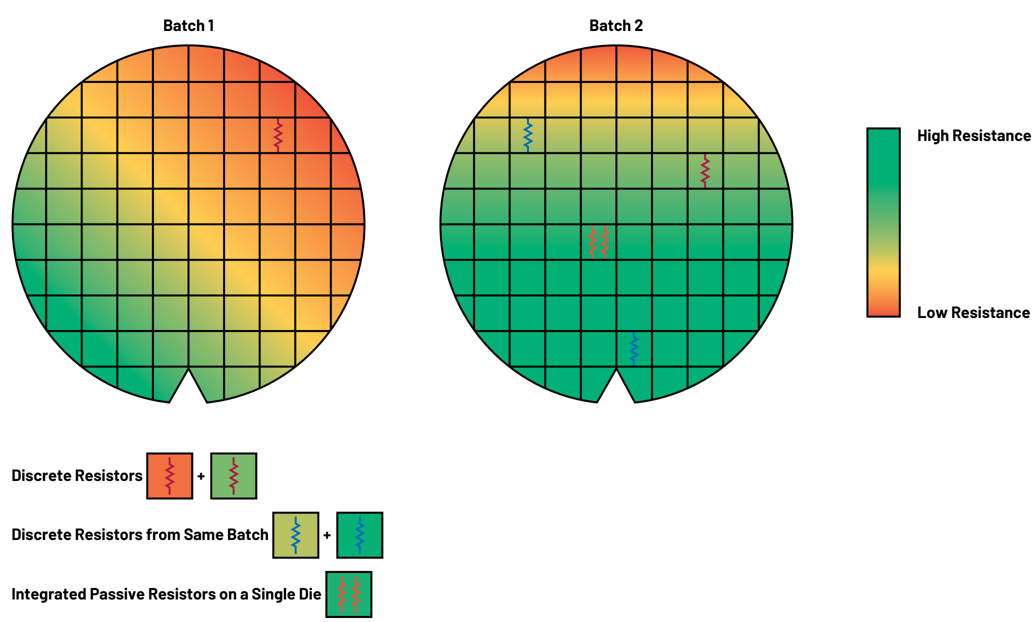

Figure 10. ADI's iPassives resistors have tighter tolerance and matching compared to discrete resistors.[7]

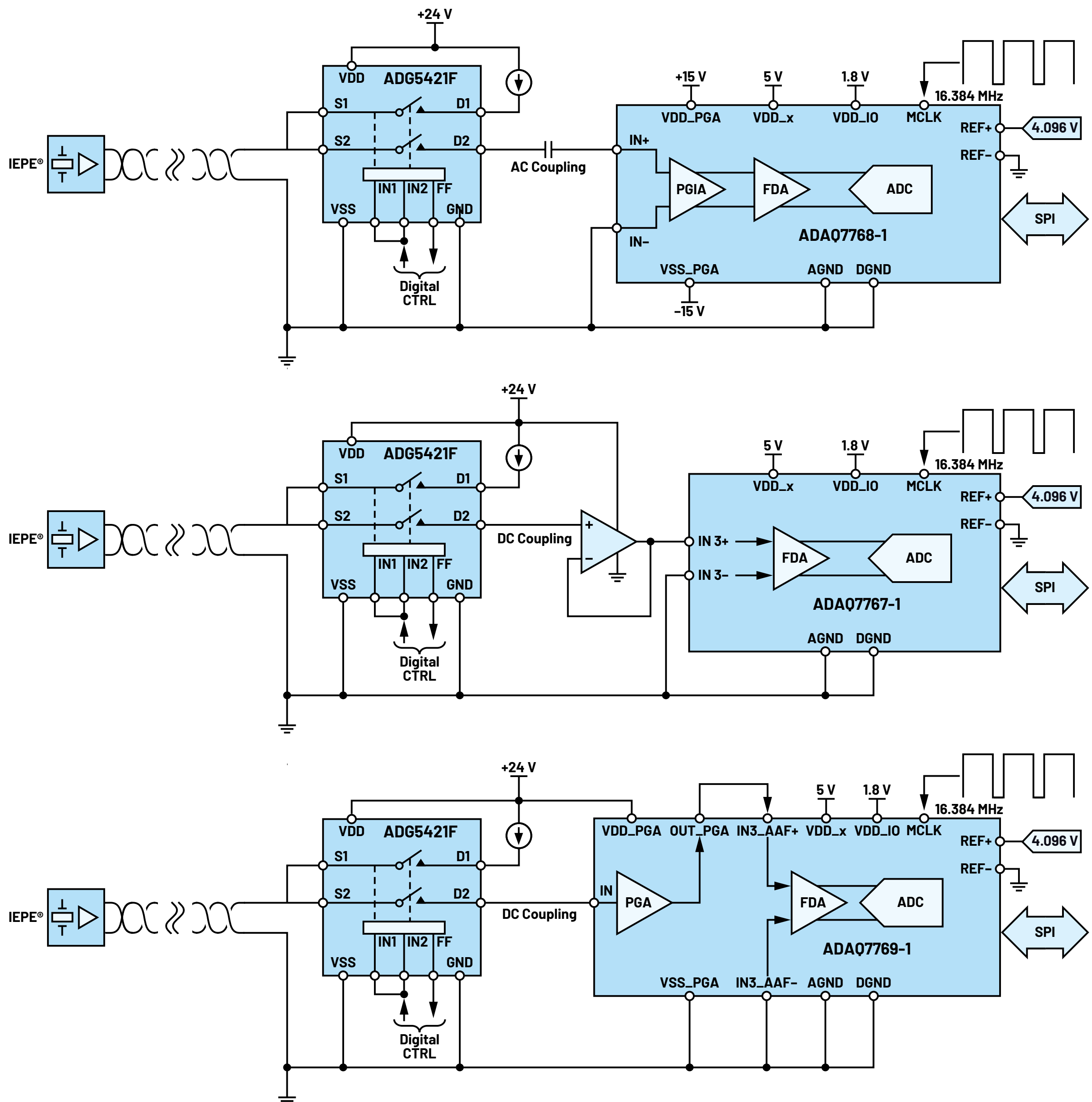

Figure 11. Various ADAQ776x-1 generics used with IEPE sensors.

pulse in sync with the shared controller clock (MCLK). Otherwise, the synchronization trigger of one device may be one MCLK period delayed from the others due to jitter and propagation delays. Figure 12 shows how each ADAQ776x-1 can be synchronized using a $\overline{\text{SYNC\_IN}}$ pulse from a controller, ideally tracking with the system MCLK.

Due to the synchronization and phase matching requirements in CM applications, the ADAQ776x-1 and AD7768-1 generics include a $\overline{\text{SYNC\_OUT}}$ pin that outputs a $\overline{\text{SYNC\_OUT}}$ pulse when triggered by a GPIO = $\overline{\text{START}}$ input pulse, or through an SPI write. In both cases, the $\overline{\text{SYNC\_OUT}}$ pulse can then be fed into the $\overline{\text{SYNC\_IN}}$ pin, triggering the start of a valid data conversion.

To reduce the number of isolated digital lines in channel-to-channel isolated systems, it is recommended to use Method 2 where synchronization can be achieved by initiating a $\overline{\text{SYNC\_OUT}}$ pulse through an SPI write to all devices from the same SPI input line (SDI), as shown in Figure 13. This assumes a common MCLK across channels, that is ideally synchronized with the SPI clock (SCLK) to avoid delayed triggering. This implementation eliminates the need for an isolated $\overline{\text{SYNC\_IN}}$ or $\overline{\text{START}}$ line from the controller. Further reducing digital isolation lines, the ADAQ776x-1 and AD7768-1 generics can combine the data ready signal (DRDY or RDY) with the output data (DOUT) in the same line.

A channel-to-channel isolated high performance DAQ solution using the ADAQ7768-1 is shown in Figure 14. It uses the ADP1031 as its isolated power solution, powering up all the supply rails, plus a ADuM141D for additional isolated digital lines.

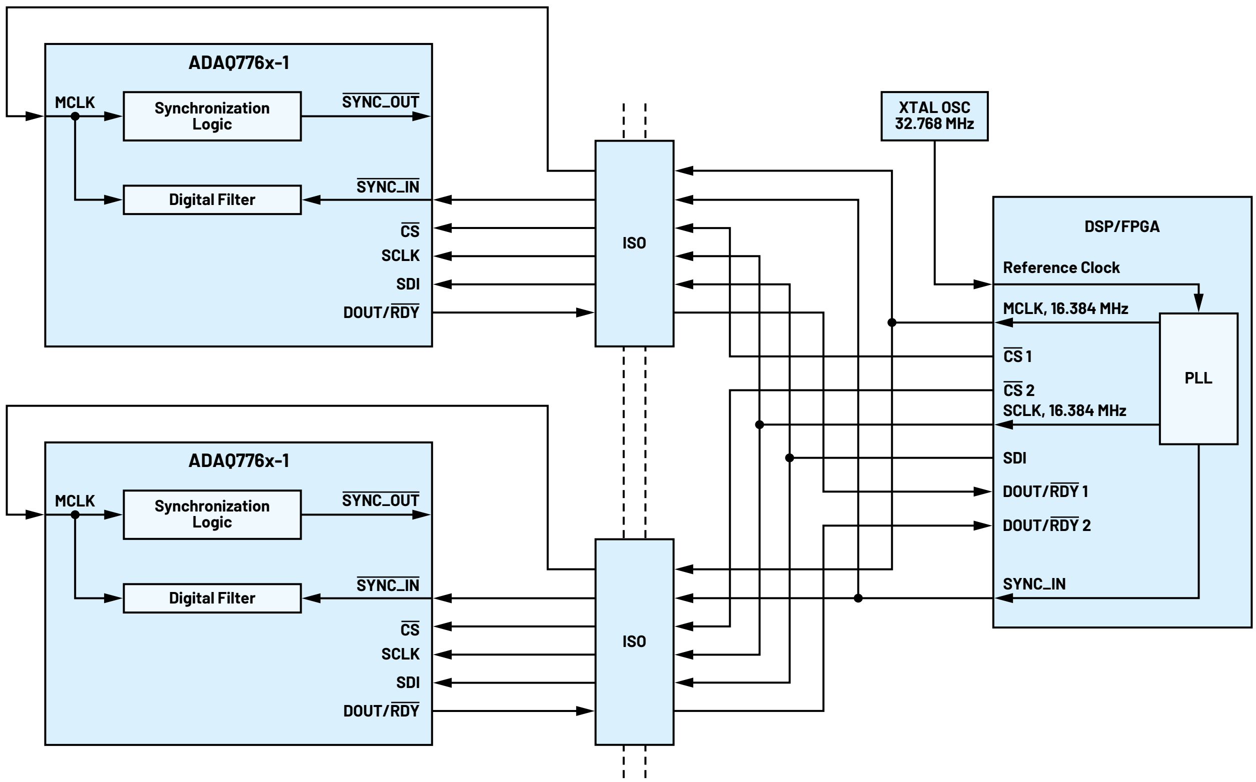

Figure 12. Synchronization of ADAQ776x-1 devices in channel-to-channel isolated systems using a SYNC_IN that tracks with MCLK.

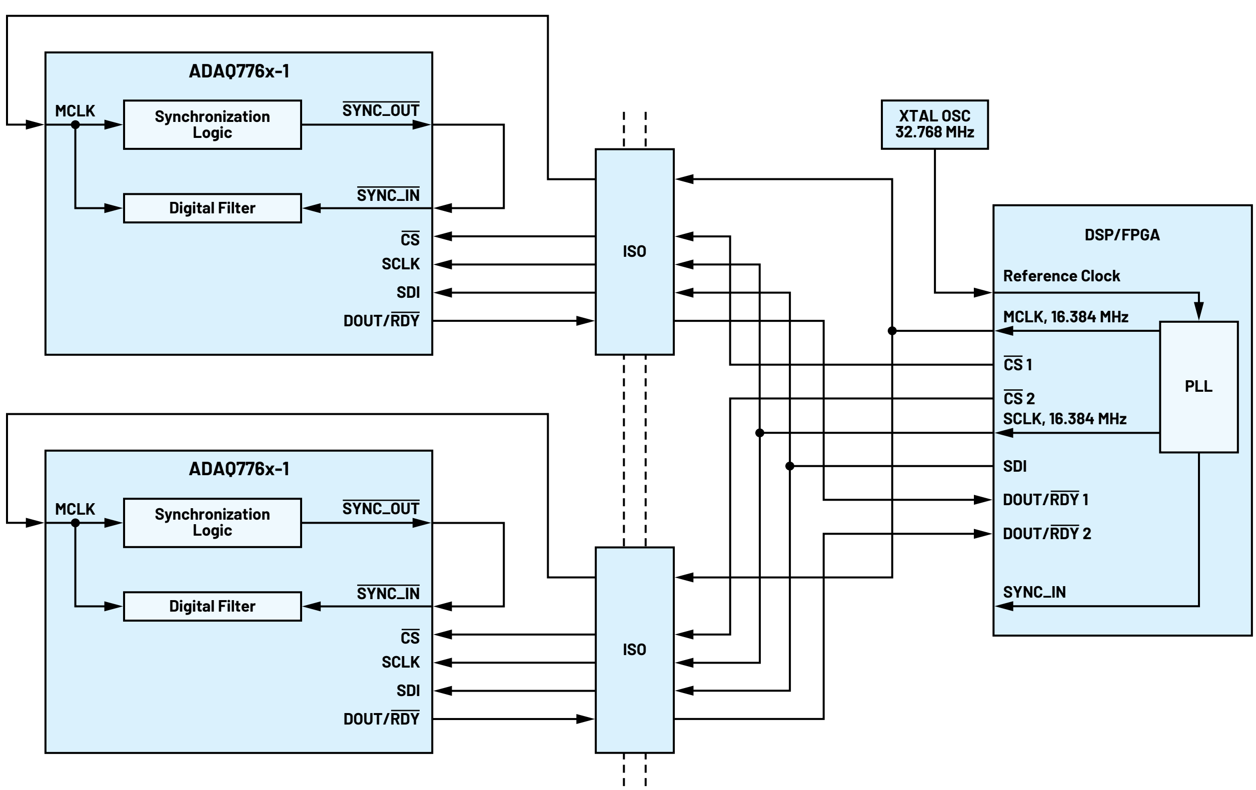

Figure 13. Synchronization of ADAQ776x-1 devices in channel-to-channel isolated systems using an SPI write.

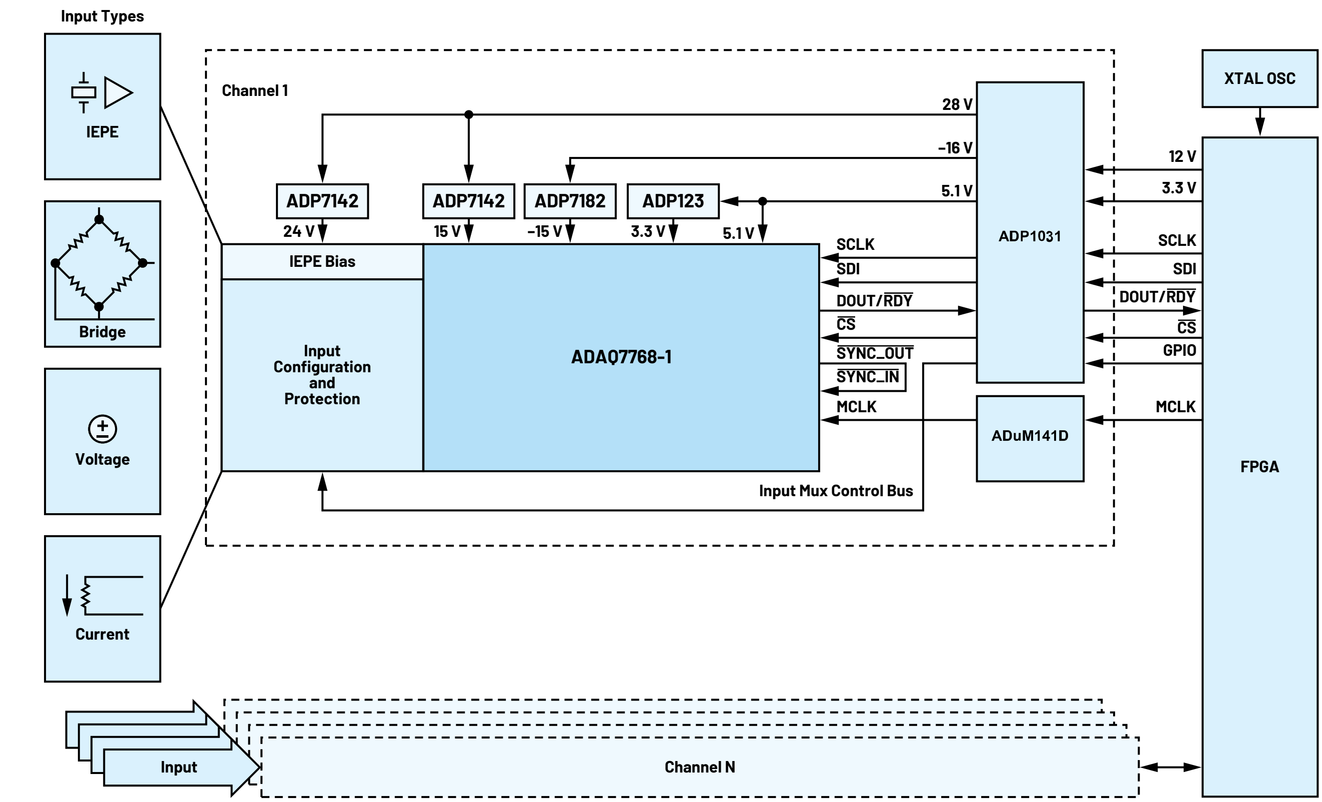

Figure 14. Channel-to-channel isolated high performance DAQ solution using the ADAQ7768-1.

Conclusion

A CM system comprised of isolated single channels of the ADAQ776x-1 is a cost-effective solution that delivers a phase matching performance comparable to simultaneous sampling SD ADCs. µModule solutions tackle the phase matching problem introduced by the RC anti-alias filters with the precise resistors provided by ADI's *i*Passives technology.

Acknowledgments

I would like to thank John Healy and Naiqian Ren for their technical contributions to this article.

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About the Author

Malcolm Kwok is a product applications engineer for Signal Chain µModule® Solutions. Since joining Analog Devices, he has been involved in the conceptualization and product development of signal chain µModule solutions, with applications focused on precision data acquisition and condition-based monitoring. He received his bachelor's and master's degrees in electronics engineering from De La Salle University Manila.