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Fully Differential Amplifier Provides High Voltage and Low Noise Signal to Precision Data Acquisition Signal Chain

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Abstract

Fully differential amplifiers (FDAs) are devices that have differential inputs and outputs with an output common mode controlled independently by a direct current (DC) input voltage. They are used in the front end of analog-to-digital conversion in data acquisition systems to condition the signal to an appropriate level for the next stage, typically an analog-to-digital converter (ADC). FDAs generally come in a single chip, have smaller supply voltages, and thus have limited output dynamic range. This article demonstrates an approach to designing a composite high voltage low noise FDA with an adjustable common-mode output. It also provides a complete analysis of FDA noise and its effects on the overall signal-to-noise ratio (SNR) of the signal chain of a high performance data acquisition system.

Introduction

High voltage FDAs are needed for applications that require wide output dynamic range and similar alternating current (AC) performance to high performance FDAs. For example, a high voltage FDA may be needed for testing and evaluating a precision data acquisition signal chain with a wide input range. Most FDAs today are generally limited in smaller output voltage ranges, due to smaller supply voltages. They are suited to drive the input of high performance ADCs, which typically require single supplies. They have superior AC performance that approaches the best SNR and total harmonic distortion (THD). However, they do not have a good swing to the rail, offset, bias current, and drift as many higher voltage precision op amps have. This is perfectly fine as they meet the requirements in driving ADCs, and Analog Devices offers a selection of ADC drivers used for a variety of applications.

FDAs can accommodate either a single-ended or differential input, have gain(s) and have differential output with a common mode that is typically adjustable via an output common-mode input pin (V_{OCM}) (see Figure 1). FDAs have the advantage of having a larger output dynamic range because of the ability to provide maximum output that is twice the output rails, has lower noise immunity, and has reduced even-order harmonic distortions. For example, a ±5 V FDA can produce a maximum output peak-to-peak of close to ±10 V or 20 V p-p.

A circuit that has ±18 V could then provide an output greater than 60 V p-p. The ADA4625-1/ADA4625-2 are low noise JFET amplifiers with very good noise and distortion performance and have a wide supply range of up to ±18 V. Designing an FDA with discrete op amps can be tricky when it requires the ability to satisfy all the DC and AC performance requirements of applications.

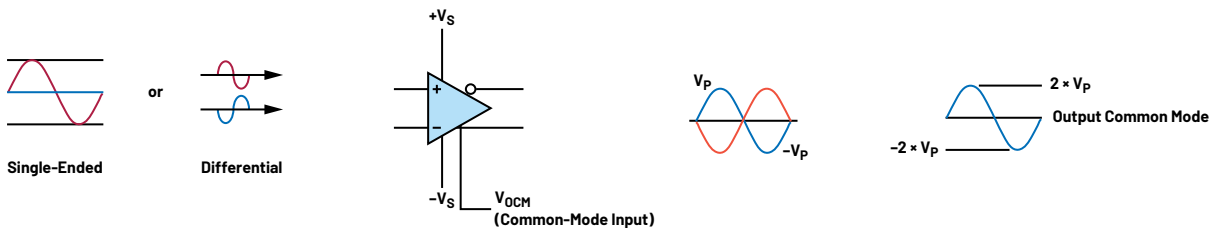

Figure 1. An FDA.

An obvious way to create a differential amplifier is to use a noninverting and inverting amplifier to produce a differential signal at the output (Figure 2). The drawback to this approach is that the two amplifiers, U1 and U2, don't operate in a very symmetrical manner, which means that performance is not optimized.

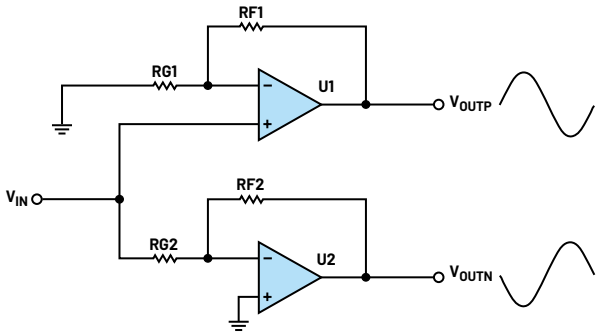

Figure 2. Single-ended to differential circuit

A better approach would be to configure the two op amps in a differential manner, similar to a basic differential amplifier, with the feedback and gain resistor shared between U1 and U2, with the gain $A_v = (R_G + 2R_F)/R_G$ (see Figure 3).

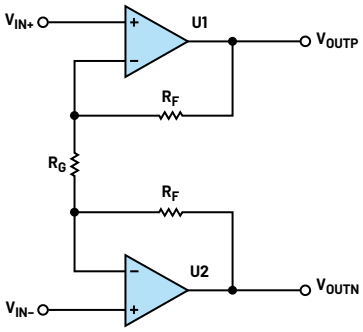

Figure 3. A differential amplifier circuit

This configuration provides a balanced output with a simplified gain network, where the gain simply can be changed through the gain setting resistor, R_G. However, when the input is single-ended, the differential output is not going to be symmetrical in amplitude (see Figure 4). With asymmetrical outputs, the output range would be severely limited, since one of the outputs reaches the rail before the other. This can be addressed by modifying the resistor gain network to make the output symmetrical (Figure 5). Notice that the gain resistor was broken into two (R_{G1} and R_{G2}) and the feedback of U2 is taken off the center of R_{G1} and R_{G2}, making the outputs symmetrical. The gain is given by: $A_v = (R_{G1} + R_{G2} + R_{F1} + R_{F2})/R_{G1}$.

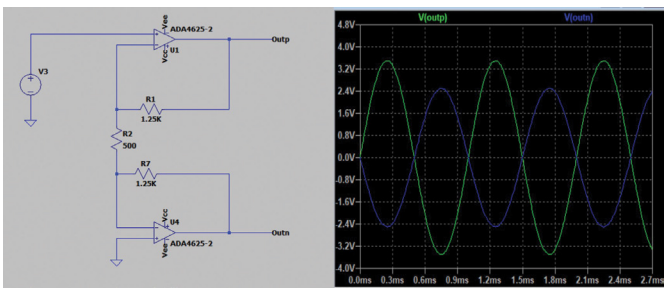

Figure 4. Asymmetrical outputs.

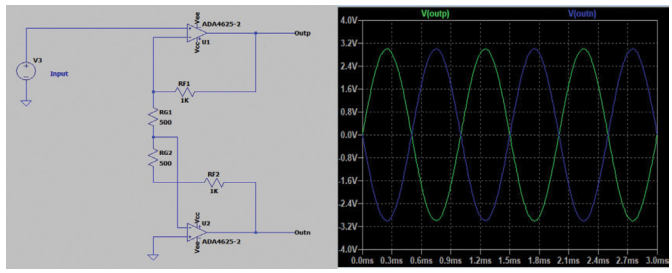

Figure 5. Symmetrical outputs.

Adding Adjustable Output Common Mode

There are two ways to add the adjustable common mode: one is by adding a V_{OCM} amplifier to each input using two ADA4625 devices (figures 6 and 7), and the other method is using only one ADA4625-1 as a V_{OCM} amplifier (figures 8 and 9). There are pros and cons to these approaches as discussed later in the article.

By adding amplifiers U3 and U4, any DC input voltage (V6) applied gets added to the positive and negative inputs. Because the same voltage is added to each input, they appear as DC common mode at the output. U3 and U4, however, create additional power consumption in the circuit, beyond the additional noise that gets further amplified by the U1 and U2 differential stage. It is, however, very straightforward and doesn't impact the overall signal gain. The signal gain is given by $A_v = (R_{G1} + R_{G2} + R_{F1} + R_{F2})/R_{G1}$ for the circuit in Figure 6, and $A_v = (R_G + R_{F1} + R_{F2})/R_G$ for the circuit in Figure 7.

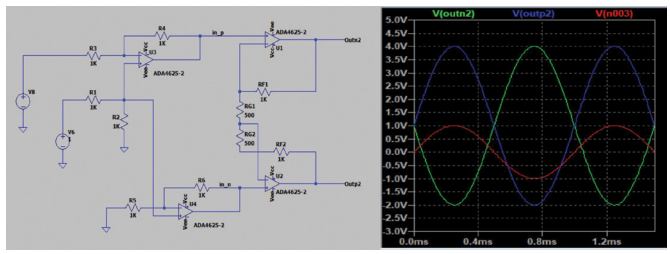

Figure 6. Single-ended-to-differential with two-amplifier adjustable common-mode circuit. The plots on the right show the LTspice® simulation of the input (red) and outputs (blue and green).

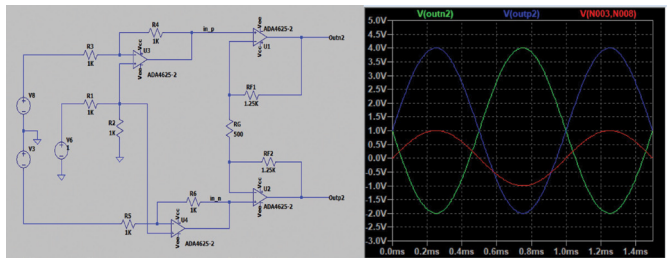

Figure 7. Differential-to-differential with dual-amplifier adjustable common-mode circuit. The plots on the right show the LTspice simulation of the input (red) and outputs (blue and green).

Another method of adding adjustable V_{OCM} is by adding a single amplifier whose output is added to each of the inputs. The advantages include using fewer components, only one amplifier, and fewer resistors, as well as lower noise contribution from the added components. In fact, U3 doesn't contribute any additional noise because its output referred noise appears as common mode to the inputs of U1 and U2, except for the noise coming from the resistor dividers R4 to R7.

Resistors R3 to R7 form the resistor adder network that adds the V_{OCM} to the input signals. R3 to R5 add common mode to the positive input signal, while R6 to R8 (R6 and R7 in the single-ended input) add to the negative input. Notice that the same resistor network attenuates the input signals. This reduces the overall signal gain of the circuit. The overall signal gain is given by $A_v = [(R_{G1} + R_{G2} + R_{F1} + R_{F2})/R_{G1}][(R4//R5)/(R4//R5 + R3)]$ for the circuit in Figure 8, and $A_v = [(R_G + R_{F1} + R_{F2})/R_G][(R4//R5)/(R4//R5 + R3)]$ for the circuit in Figure 9. The noise analysis section shows what the dominant noise contributor is and, depending on the desired overall gain and other factors important to the designer, whether it's more beneficial to use the second method of adding the V_{OCM} over the first method.

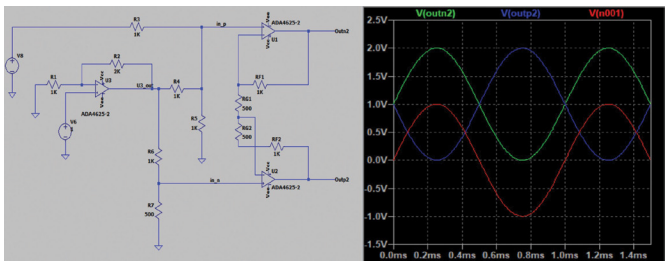

Figure 8. Single-ended-to-differential with single-amplifier adjustable common-mode circuit. The plots on the right show the LTspice simulation of the input (red) and outputs (blue and green).

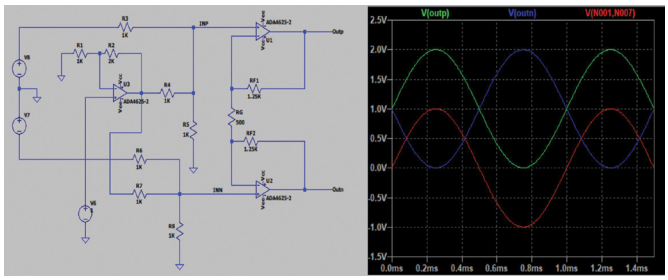

Figure 9. Differential-to-differential with single-amplifier adjustable common-mode circuit. The plots on the right show the LTspice simulation of the input (red) and outputs (blue and green).

Noise Analysis

Noise is a critical consideration in providing stimulus to a high performance precision data acquisition signal chain, as this will eventually set the limitations of the system in terms of dynamic range and SNR. A 16-bit ADC has a theoretical SNR of –98 dB (6.02 N + 1.76 dB, N = number of bits), which means an equivalent noise of ~36 µV rms for 4.096 Vp output (or 8.192 V p-p). This noise, called quantization noise, is due to the quantization error of the ADC. The SNR of –98 dB would be the ideal limit of a 16-bit system, and any degradation will be due to additional noise to the inputs or circuits around the ADC. The following are the analyses of the noise contributions of each of the components in the circuits for both the single- and dual-amplifier V_{OCM} fully differential circuits. Figure 10 shows the noise model of the FDA circuit with a two-amplifier V_{OCM}.

Differential Stage—U1 and U2 Noise Contributions

The ADA4625-1/ADA4625-2 have an ultralow current noise density of 4.5 fA/√Hz at 1 kHz, while the referred to input (RTI) voltage noise is around 3 nV /√Hz at 1 kHz, which we can consider in this analysis as the wideband noise. The total noise contribution of the current and voltage noise of U1 and U2 at the output differentially in rms can be shown to be:

$$e_{N,V\_U1U2} = \left(\sqrt{e^2_{N,RTIU1} + e^2_{N,RTIU2}}\right)\left(\frac{R_G + R_{F1} + R_{F2}}{R_G}\right) \quad (1)$$

$$e_{N,I\_U1U2} = \left(\sqrt{i^2_{N,RTIU1} + i^2_{N,RTIU2}}\right) R_G \left(\frac{R_G + R_{F1} + R_{F2}}{R_G}\right) \quad (2)$$

Where $e_{N_V,U1U2}$ is the output voltage noise due to the RTI voltage noise of U1 and U2, while $e_{NI,U1U2}$ is the output voltage noise due to the input current noise. The RTI voltage noise was combined by getting the root of the sum of the squares (RSS) at the input and then amplified by the gain and feedback network R_F and R_G. Similarly, the current noise is RSS'ed, converted to voltage noise by R_G, and amplified to the output. Since the input current noise is very small, its contribution is insignificant, making the resistors and the voltage noise of the amplifiers the dominant noise contributors at the output.

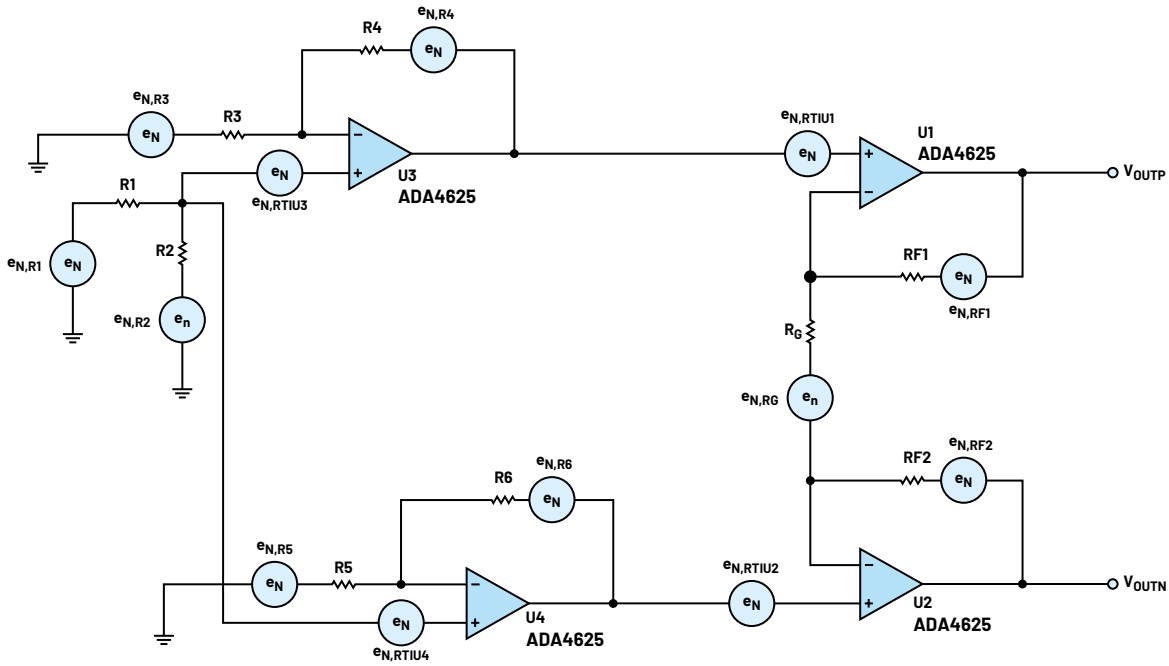

Figure 10. A two-amplifier V_{OCM} noise model.

The output noise due to the gain and feedback resistor network of U1 and U2 (R_{F1}, R_{F2}, and R_G) are found to be:

$$e_{N,RES\_U1U2} = \sqrt{\left[e_{N,RG}\left(\frac{R_G + R_{F1} + R_{F2}}{R_G}\right)\right]^2 + e^2_{N,RF1} + e^2_{N,RF2}} \quad (3)$$

Where the thermal noise of 1 kΩ at room temperature is 4.06 nV/√Hz.

Combining at the output the voltage noise of U1 and U2 and its feedback resistor network noise, ignoring the current noise, using equations 1 and 3 gives us:

$$e_{N,U1U2} = \sqrt{e^2_{N,V\_U1U2} + e^2_{N,RES\_U1U2}} \quad (4)$$

It can be seen from earlier that the voltage noise of the amplifiers can easily become dominant with higher gain. Using smaller values for R_G—500 Ω, for example—can greatly minimize the noise from the resistors.

V_{OCM} Circuit—U3 and U4 Noise

Let's next analyze the noise from the V_{OCM} circuit in Figure 10. The total noise from the V_{OCM} circuit (U3 and U4), including the resistor noise, and ignoring the input current noise from each of the amplifiers, are derived to be the following:

$$e_{NO,U3} = \sqrt{\left[e_{N,RTIU3}\left(1+\frac{R4}{R3}\right)\right]^2 + \left[e_{N,R3}\frac{R4}{R3}\right]^2 + e^2_{N,R4} + \left[e_{N,R1//R2}\left(1+\frac{R4}{R3}\right)\right]^2} \quad (5)$$

$$e_{NO,U4} = \sqrt{\left[e_{N,RTIU4}\left(1+\frac{R6}{R5}\right)\right]^2 + \left[e_{N,R5}\frac{R6}{R5}\right]^2 + e^2_{N,R6} + \left[e_{N,R1//R2}\left(1+\frac{R6}{R5}\right)\right]^2} \quad (6)$$

$$Total\ V_{OCM}\ Output\ Noise = \sqrt{e^2_{NO,U3} + e^2_{NO,U4}}$$

Where R1//R2 is the parallel combination of R1 and R2. It is also evident from earlier that the total noise from U3 and U4 is dominated by both the amplifier voltage and the resistor noise. It is a good idea to keep the values of the resistors low to minimize their contribution to the overall noise, making the amplifier noise the only dominant noise contributor. The noise from the output of the V_{OCM} circuit will appear to the inputs of the differential stage, and then consequently be amplified to the output by the differential stage.

V_{OCM} Circuit—Single-Amplifier U3 Noise

As mentioned earlier, the noise at the output of U3 appears as common mode to the inputs of U1 and U2 (shown as inp and inn, see Figure 11), and therefore does not add noise to the differential stage. The additional noise comes from resistors R3 to R8, which, by close inspection, are three resistors in parallel at each input to the differential stage—R3 to R5 at the positive input and R6 to R8 at the negative input (Figure 11c), which also makes the resistor contributions minimal.

Of the two circuits (the dual-amplifier and the single-amplifier V_{OCM} circuit), the latter has much lower noise contributions. Its drawback, however, is reduced overall signal gain. It also offers lower power and fewer amplifiers. Equations 7 and 8 show the noise at the output of the V_{OCM} circuit in Figure 11, and its corresponding noise contribution at the output of the differential stage change to U1 and U2, respectively.

$$e_{N,V_{OCM\_U3},} = \sqrt{e^2_{N,R3R4R5} + e^2_{N,R6R7R8}} \quad (7)$$

$$e_{N,V_{OCM\_U3}} = \left(\sqrt{e^2_{N,R3R4R5} + e^2_{N,R6R7R8}}\right)\left(\frac{R_G + R_{F1} + R_{F2}}{R_G}\right) \quad (8)$$

Tying It All Together—Overall SNR of the ADC Signal Chain

The total SNR of the ADC signal is determined by the total noise contribution of the analog front end (AFE) and the ADC, which may include noise from other sources. The total SNR of the ADC signal chain is given by:

$$SNR = 20\ log\left(\frac{Total\ System\ Noise,\ rms}{\frac{V_{REF}}{\sqrt{2}}}\right) \quad (9)$$

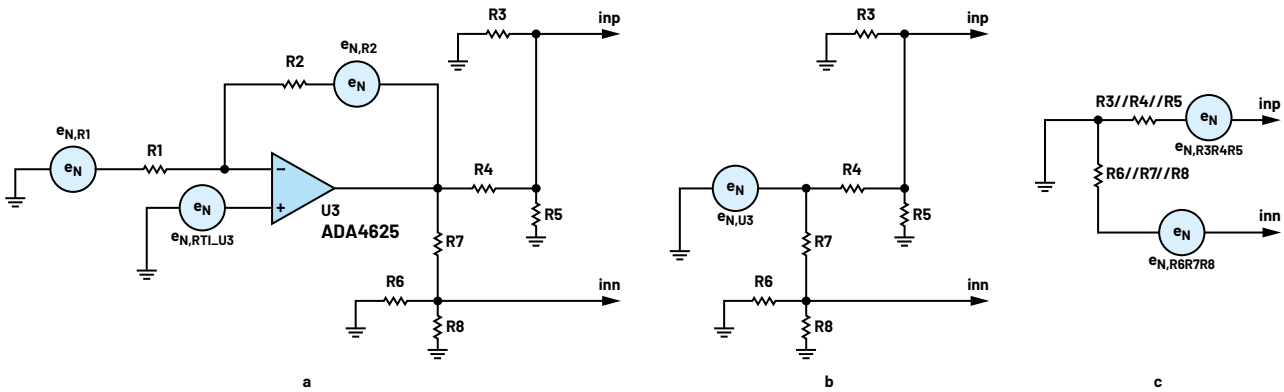

Figure 11. A single-amplifier V_{OCM} noise model.

Where V_{REF} is assumed to be the positive full scale of a bipolar output ADC.

In general, the total SNR of the signal chain can be summed up in Figure 12.

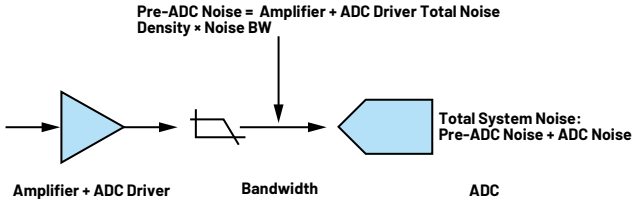

Figure 12. A data acquisition front-end signal chain.

The noise of the ADC combined with the noise at the input from the AFE will produce a total degraded SNR from the ADC's theoretical or ideal value. To combine the noise of the AFE to that of the ADC, the SNR of the ADC needs to be converted into its rms integrated noise equivalent, given as follows:

$$ADC\ Noise\ (\text{rms}) = \left(\frac{V_{REF}}{\sqrt{2}}\right) \times 10\ \left(\frac{ADC\ SNR}{20}\right) \quad (10)$$

As an example, the ADAQ7767-1 has a typical SNR of −106 dB and has an equivalent rms noise of 14.5 µV.

The ADAQ7767-1 is a 24-bit data acquisition solution with an integrated ADC driver and antialiasing filter. It comes with a gain of 1, 0.364, 0.143 V/V. It has a noise bandwidth (BW) of 110 kHz at 250 kSPS, and its steep cutoff is dominated by its digital brickwall filter. Given that the ADA4625-1/ADA4625-2 have a typical 3.3 nV/√Hz wideband voltage noise, the output noise contribution of the differential stage (U1 and U2) from Figure 13, with a noise gain of 6, are as follows:

$e_{N,V\_U1U2} = [\sqrt{2(3.3\ nV)^2}](500\ \Omega + 1.5\ k\Omega + 1\ k\Omega)/500\ \Omega = 28\ nV/\sqrt{Hz}$, due to U1 and U2 RTI noise, using Equation 1.

$e_{N,RES\_U1U2} = \sqrt{[2.87\ nV(6)]^2 + (4\ nV)^2 + (4.97\ nV)^2} = 18.4\ nV/\sqrt{Hz}$, due to resistor gain network, using Equation 3.

$e_{N,U1U2} = \sqrt{(28\ nV)^2 + (18.4\ nV)^2} = 33.5\ nV/\sqrt{Hz}$, total output noise contribution of the differential stage.

From Equation 8, where the equivalent value of the three resistors (1 kΩ) in parallel is 333.3 Ω to the input of differential stage, with 2.3 nV/√Hz noise:

$e_{NO,V_{OCM\_U3}} = 6\sqrt{2(2.3\ nV)^2} = 19.5\ nV/\sqrt{Hz}$, output noise contribution circuit due to resistors R3 to R8.

Therefore, the total output noise, which appears at the input of the ADAQ7767-1, is as follows:

$$e_{NO} = \sqrt{e^2_{NO,V_{OCM\_U3}} + e^2_{N,U1U2}} = \quad (11)$$

$$\sqrt{(19.5\ nV)^2 + (33.5\ nV)^2} = 38.8\ nV/\sqrt{Hz}$$

The input gain stage configuration of the ADAQ7767-1 is set to 0.143 V/V and has an input range of ±28 V (56 V p-p). Combining the noise of the input circuit with the noise of the device, given that the typical SNR of −106 dB is equivalent to 14.5 µv rms noise, yields the following:

$$Total\ Input\ Noise\ (\text{rms}) = (38.8\ nV/\sqrt{Hz}) \quad (12)$$

$$(0.143)(\sqrt{110\ kHz}) = 1.8\ \mu V\ \text{rms}$$

$$Total\ System\ Noise = \sqrt{(14.5\ \mu V)^2 + (1.8\ \mu V)^2} \quad (13)$$

$$= 14.6\ \mu V\ \text{rms}$$

The contribution of the input circuit to the total system noise is only very small, in part due to the small input gain of the ADAQ7767-1. Note that no filter bandwidth adjustment factor is used when we multiply the bandwidth since the 110 kHz is a digital filter with brickwall characteristics. From the typical SNR of −106 dB, the resulting SNR of the signal chain will therefore be:

$$SNR = 20\ log\left(\frac{14.6\ \mu V\ \text{rms}}{4.096/\sqrt{2}}\right) = -105.9\ \text{dB} \quad (14)$$

Noise simulation of the input circuit in Figure 13 using LTspice (Figure 14) shows a total rms noise of 12.3 µV rms for 110 kHz bandwidth. This is to be multiplied by the gain of 0.143 V/V, which results in 1.8 µV rms noise at the input of the ADAQ7767-1, identical to the calculated value of the total input noise.

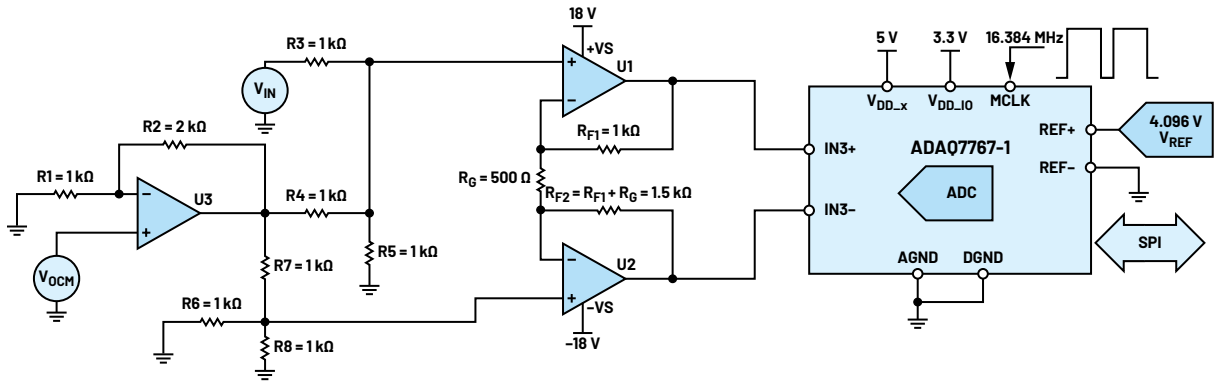

Figure 13. The ADAQ7767-1 precision signal chain with high voltage input.

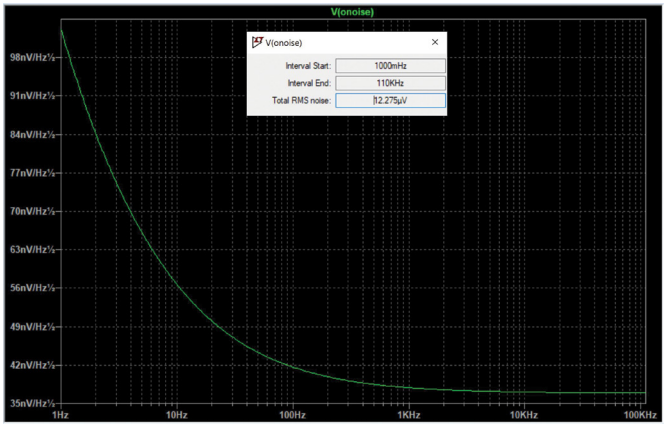

Figure 14. LTspice noise in Figure 13 ADAQ7767-1 input circuit.

Table 1 shows the resulting overall SNR of the signal chain using the other gains of the ADAQ7767-1.

Table 1. Overall Signal Chain SNR with Different ADAQ7767-1 Gains

Total AFE (FDA) Noise (V rms)	Bandwidth in Hz (Brickwall)	ADAQ7767-1 Gain	Total ADC Input Noise (V rms)	Total System Noise (V rms)	Overall SNR (dB)
3.88E-08	1.10E+05	0.143	1.84E-06	1.46E-05	-105.94
3.88E-08	1.10E+05	0.364	4.68E-06	1.52E-05	-105.58
3.88E-08	1.10E+05	1	1.29E-05	1.94E-05	-103.49

We have only used the single-amplifier V_{OCM} circuit in Figure 13. The circuit can be used to provide a large input voltage to a front-end signal chain system without a significant impact on the noise performance. The dual-amplifier V_{OCM} circuit can provide similar noise performance at the same overall signal gain. The noise equations shown in the Noise Analysis section, V_{OCM} Circuit—U3 and U4 Noise, can be used to calculate the total noise at the output of the dual-amplifier V_{OCM} circuit, and the same methods and concepts can be applied to calculate the total SNR of the signal chain.

Conclusion

Creating a composite FDA using the ADA4625-1/ADA4625-2 in the circuits presented in this article provides a low noise and high voltage output solution with an adjustable common mode that can be used to drive a high performance data acquisition signal chain with a wide input range. Either single-ended or differential input can be accommodated by configuring the feedback network of the differential stage appropriately. The single-amplifier V_{OCM} circuit is superior to the dual-amplifier V_{OCM} circuit because it offers lower power and fewer amplifiers. Our example shows that the overall SNR of the ADAQ7767-1 signal chain is not affected significantly by the FDA circuit at lower gains. It has input ranges of ±4.096 V, ±11.264 V, and ±28 V for gains of 1 V/V, 0.364 V/V, and 0.143 V/V, respectively, where the lowest gain has the widest input range and benefits the most from the solution.

About the Author

Darwin Tolentino is currently a product/test development manager in Analog Devices in General Trias Cavite for the precision µModule® signal chain, which provides integrated and complete solutions to precision data conversion. He joined ADI in 2000 as a product manufacturing engineer, and later became a product and test development engineer designing ATE solutions for various linear and precision products, such as amplifiers, references, and converters.