Vol 58, No 3—August 2024

ANALOG DEVICES | ADI Analog Dialogue™

Considerations for the Output Current and Voltage Ripple in a Multiphase Buck with Coupled Inductors

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Abstract

Multiphase coupled inductors are a promising technology with significant system benefits due to the current ripple cancellation inside each coupled phase. A surprising fact, however, is that the total output current ripple of the multiphase buck is the same for coupled or noncoupled inductors. This article focuses on considerations for the output current ripple and the specific details that impact output voltage ripple and overall converter performance.

Introduction

The multiphase buck converter is a widely used topology for voltage step-down applications with high output currents. Voltage regulators with this circuit can be found in servers, AI, data centers, cloud computing, communications, automotive, and more.

Current ripple in inductors is an important parameter that influences design choices, which impacts efficiency, output voltage ripple, transient performance, solution size, and other performance metrics. This article will focus on these current ripple considerations.

The conventional multiphase buck converter with discrete inductors (DL) is shown in Figure 1a. An alternative to replace DLs with coupled inductors (CLs) is depicted in Figure 1b.[1-9] It is important to ensure a phase shift between all converter phases (1 to N_{ph}) for optimal interleaving of waveforms. Such phase shift is generally expected to minimize the total output current ripple that goes into the output capacitance C_o and therefore the output voltage ripple. The appropriate phase shift is also needed to get the best performance in the CL.

The current ripple in each phase of the conventional buck converter can be calculated using Equation 1, where duty cycle $D = V_{OUT}/V_{IN}$, V_{OUT} is the output voltage, V_{IN} is the input voltage, L is the inductance value, and F_s is the switching frequency. Assuming the discrete inductor is replaced with a coupled inductor of the same value (L, now leakage inductance) and added mutual inductance L_m, the current ripple in CL can be shown in Equation 2.[6] The figure of merit (FOM) is expressed as Equation 3, where N_{ph} is the number of coupled phases, ρ is a coupling coefficient (Equation 4), and j is a running index that defines an applicable interval of the duty cycle (Equation 5).

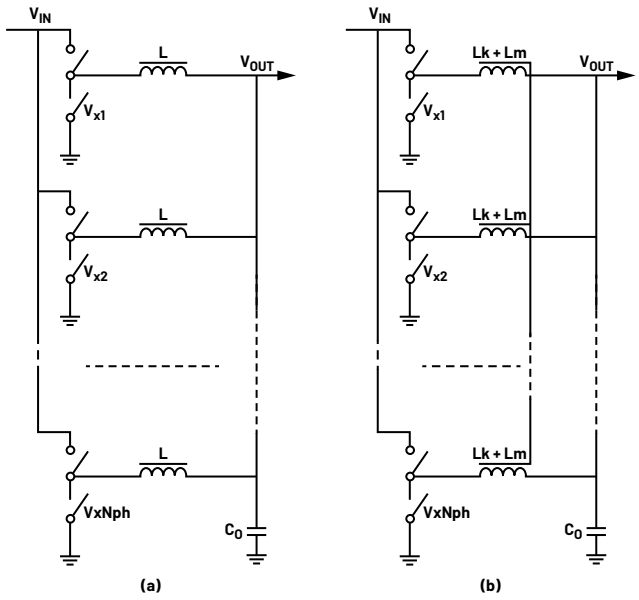

Figure 1. Multiphase buck converter with (a) discrete inductors DL and (b) coupled inductors CL.

$$dIL_{DL} = \frac{V_{IN} - V_{OUT}}{L} \times \frac{D}{F_S} \quad (1)$$

$$dIL_{CL} = \frac{V_{IN} - V_{OUT}}{L} \times \frac{D}{F_S} \times \frac{1}{FOM\,(D,\, N_{ph},\, \rho,\, j)} \quad (2)$$

$$FOM = \frac{1 + \frac{\rho}{\rho + 1} \times \frac{1}{N_{ph} - 1}}{1 - \left[(N_{ph} - 2 \times j - 2) + \frac{j \times (j+1)}{N_{ph} \times D} + \frac{(N_{ph} \times D \times (N_{ph} - 2 \times j - 1) + j \times (j+1)}{N_{ph} \times (1 - D)} \right] \times \frac{\frac{\rho}{\rho + 1}}{N_{ph} - 1}} \quad (3)$$

$$\rho = \frac{L_m}{L} \quad (4)$$

$$j = floor\,(D \times N_{ph}) \quad (5)$$

Generally, CL exhibits a larger FOM,[6] indicating a significant advantage in terms of current ripple cancellation (Equation 2) as compared to DL (Equation 1). In other words, the same transient performance of inductance L will result in a considerably smaller current ripple in the case of CL, allowing for a potential reduction in F_s for higher efficiency. Alternatively, the inductance value can be decreased for faster transient and smaller magnetics and output capacitance. Thus, the benefits of CL can be leveraged in various ways, such as reducing solution size or achieving notable improvements in efficiency.

Total Current Ripple at Output

Interleaved multiphase converters offer the advantage of reduced total current ripple when multiple inductor currents flow into the same net.[10,11] In the case of a multiphase buck converter, this reduction in total AC flowing into the output capacitors (C_o) is generally achieved (Equation 6). Reduced AC in the output capacitance is typically beneficial as it reduces the output voltage ripple and slightly improves efficiency. Additionally, improvements can also be observed in the ripple in input capacitors. However, the main focus of this article will be on the current ripple in inductors and its impact on the output.

$$dIL_O = \frac{V_{OUT}}{L \times F_S} \times \left(1 - \frac{j}{N_{ph} \times D}\right) \times (1 + j - N_{ph} \times D) \quad (6)$$

The current ripple in DL phase (Equation 1) will have the largest amplitude at D = 0.5. Normalizing (Equation 6) by that worst value allows to eliminate voltages, frequency, and inductance, and plot the normalized (relative) total current ripple curves as a function of the duty cycle (Equation 7). Of course, this assumes that all eliminated circuit conditions remain the same.

$$dIL_{O\_NORM} = \frac{D}{0.25} \times \left(1 - \frac{j}{N_{ph} \times D}\right) \times (1 + j - N_{ph} \times D) \quad (7)$$

The total normalized output current ripple in the multiphase buck converter is represented by Equation 7 and is visualized in Figure 2. It is worth noting that it equals a single-phase current ripple when N_{ph} = 1, as expected. When more phases (1 to N_{ph}) are paralleled with a phase shift of 360/N_{ph} degrees between each phase, it often results in a proportionally higher output current and therefore power. However, Figure 2 shows that the total current ripple that goes into output capacitance decreases dramatically at the same time. This highlights one of the advantages of interleaving multiple phases for better system performance, which applies to both DL and CL configurations. Although the current waveforms inside each phase of uncoupled DL and CL may appear different, the total summed current (total output current in a multiphase buck) exhibits the same waveform. In fact, equations 6 and 7 are applicable to both DL and CL buck converters (with the exception that CL needs $N_{ph} > 1$). Figure 3, Figure 4, and Figure 5 show simulated current ripple in six phases of buck with V_{IN} = 12 V, V_{OUT} = 1.0 V (D = 0.0833), L = 50 nH, F_s = 600 kHz. Bottom red curves illustrate the total six phase current ripple at the output. Figure 3a corresponds to the discrete inductor case L_m = 0 (DL = 50 nH), and Figure 3b has a small L_m = 20 nH introduced (CL = 6× 50 nH). Increasing the coupling further, Figure 4a has L_m = 50 nH and Figure 4b has L_m = 200 nH. The latter corresponds to the off-the-shelf six-phase coupled inductor CL1010V1-6-R050-R: CL = 6× 50 nH, L_m = 200 nH. Finally, it is important to note that Figure 5a and Figure 5b depict cases that are practically unrealistic due to challenging implementation of very large L_m = 1 µH and L_m = 10 µH, respectively.

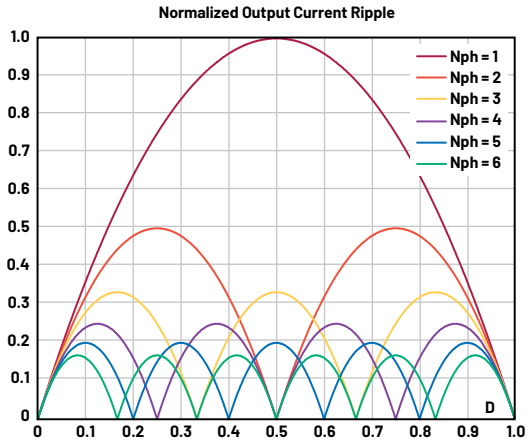

Figure 2. Normalized total output current ripple (7) in a multiphase buck converter as a function of the duty cycle D.

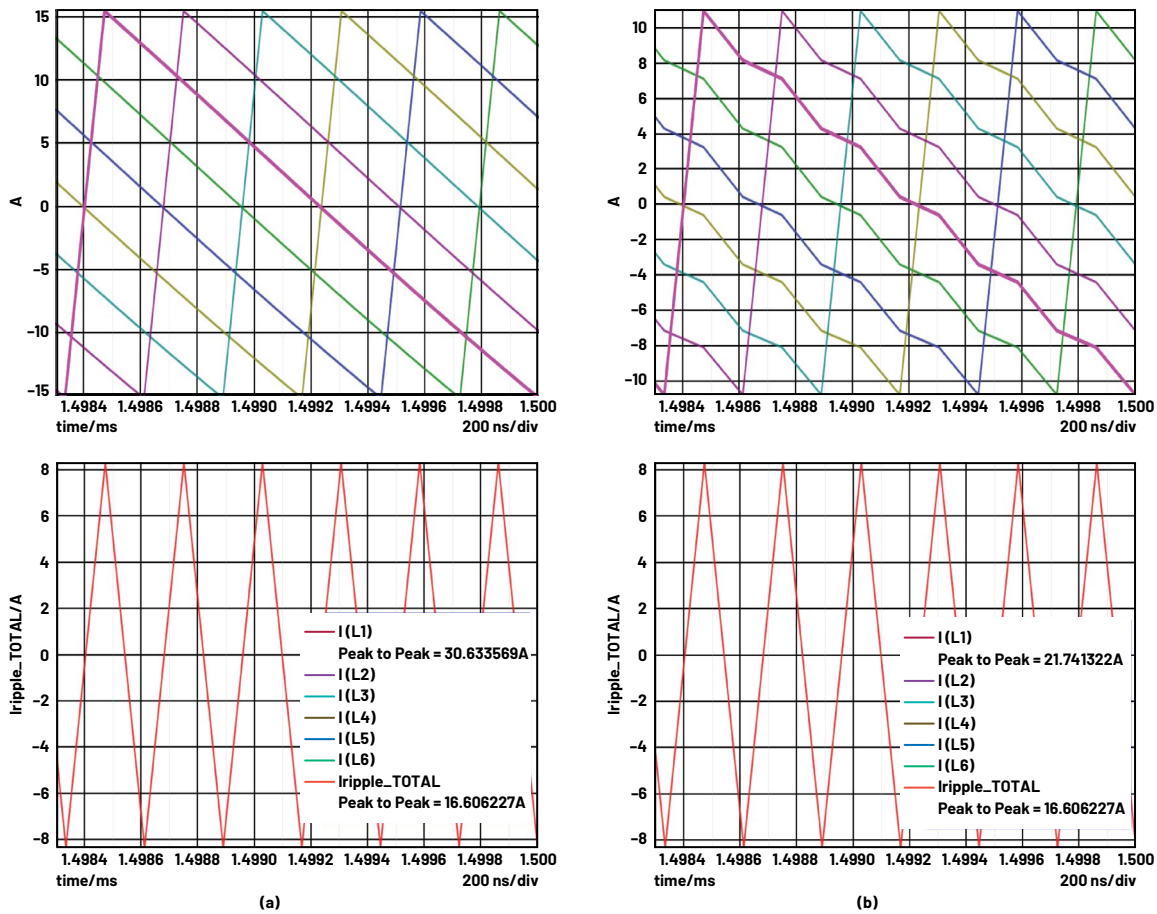

Figure 3. Individual inductor currents (top) and the total output current (bottom red curves) for a 6-phase 12 V to 1.0 V buck where F_s = 600 kHz: (a) discrete DL = 50 nH (L_m = 0), (b) CL = 6× 50 nH, and L_m = 20 nH. The first phase current I(L1) is highlighted for clarity. Output current ripple is the same 16.6 A for any L_m value.

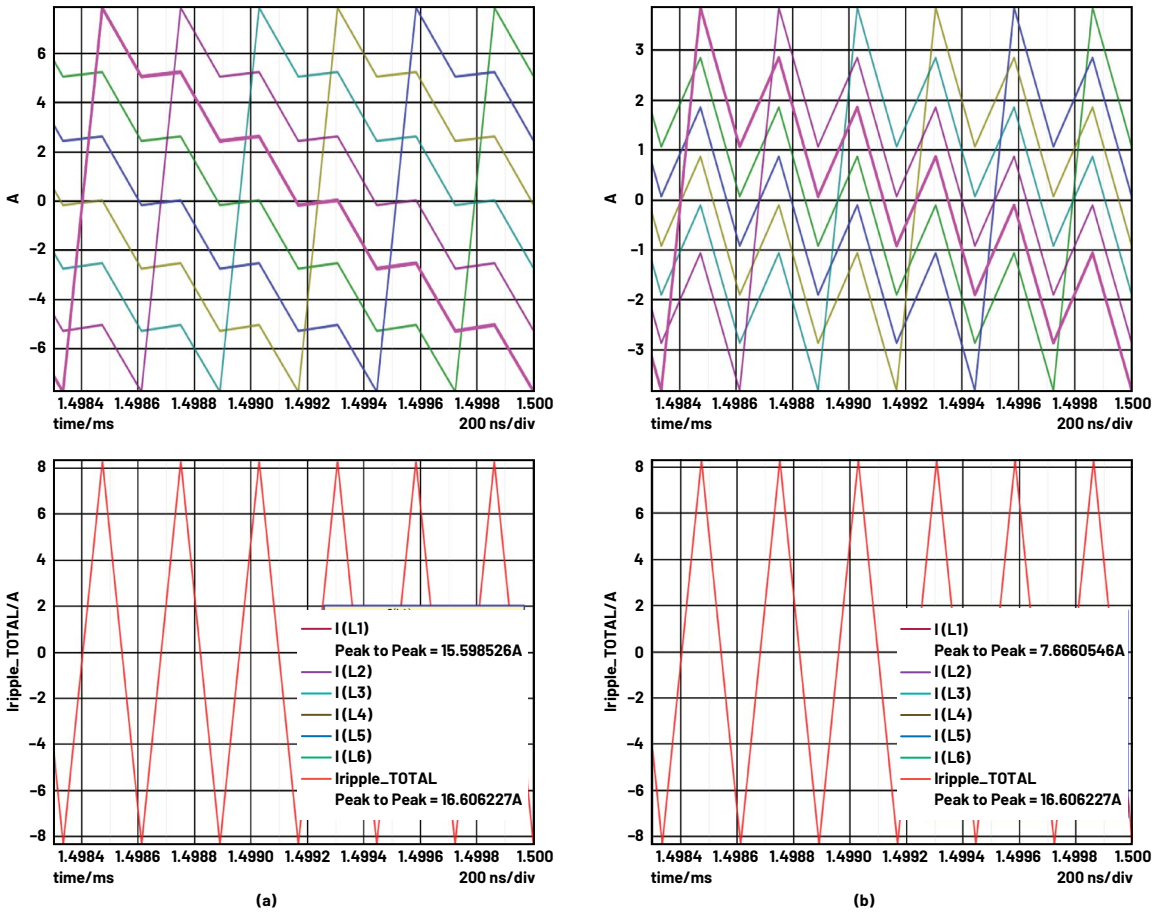

Figure 4. Individual inductor currents (top) and the total output current (bottom red curves) for a 6-phase 12 V to 1.0 V buck where F_s = 600 kHz: (a) CL = 6× 50 nH, L_m = 50 nH, (b) CL = 6× 50 nH, and L_m = 200 nH. The first phase current I(L1) is highlighted for clarity. Output current ripple is the same 16.6 A for any L_m value.

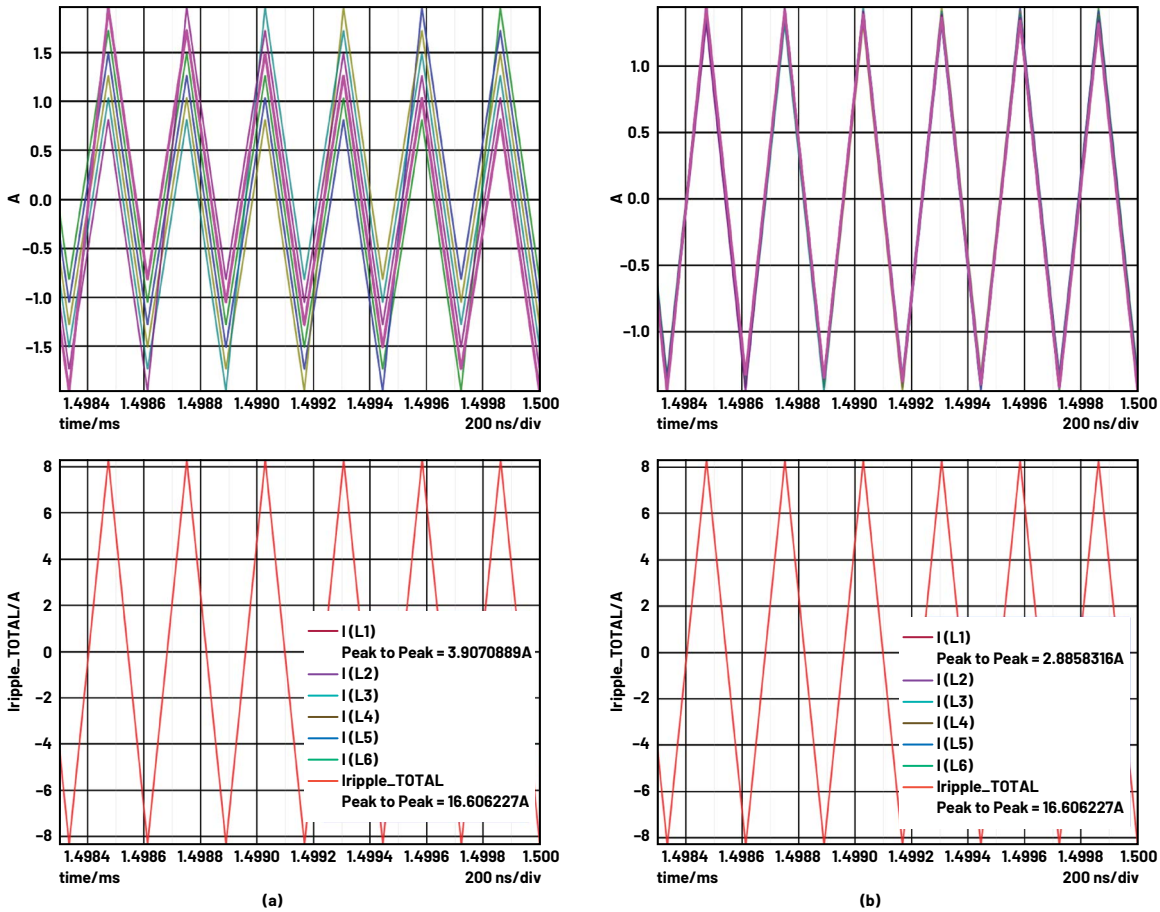

Figure 5. Individual inductor currents (top) and the total output current (bottom red curves) for a 6-phase 12 V to 1.0 V buck where F_s = 600 kHz: (a) CL = 6× 50 nH, L_m = 1 µH, (b) CL = 6× 50 nH, and L_m = 10 µH. The first phase current I(L1) is highlighted for clarity. Output current ripple is the same 16.6 A for any L_m value.

The advantage of current ripple cancellation in CL is visible. As mutual inductance is increased, the ripple current in each phase decreases dramatically until reaching a diminishing return, where a further increase of L_m lowers the current ripple at a smaller and smaller rate. Designing an overkill L_m, such as 1 µH or 10 µH in Figure 5, would also noticeably impact the CL size and most likely DCR, so these cases are plotted just to show the current ripple trend.

Comparing the amplitude of the phase currents between DL = 50 nH (Figure 3a) and CL = 6× 50 nH with L_m = 200 nH (Figure 4a) shows a significant reduction in current ripple, with a 4× decrease (from 30.63 A to 7.7 A). However, note that the bottom red curves representing the total output current ripple from all phases remain identical for any L_m value (including L_m = 0 in Figure 3a), even though the phase current waveforms are very different. The peak-to-peak amplitudes of the simulated ripple waveforms in figures 3 to 5 align with the calculated current ripple (1), (2), and (6) plotted in Figure 6. For the given conditions V_{IN} = 12 V, N_{ph} = 6, and, F_s = 600 kHz, the total output current ripple from all six phases remains constant for any L_m value and equals 16.6 A for V_{OUT} = 1.0 V. One way to understand this phenomenon is by recognizing that as the L_m value increases, the current ripple decreases, causing the phase currents to become more similar. Consequently, their peaks effectively add up to the output. It could be approximately considered that coupling reduces the phase ripple by a factor ~N_{ph} but then N_{ph} similar ripple peaks are added together at the output, resulting in the same total output current ripple. This is particularly evident in Figure 5, where waveforms with very large L_m are shown. It can be observed that the total current ripple cancellation for interleaved phases remains consistent for the same inductor values. However, there is a distinction in how this cancellation occurs. In the case of DL, it primarily takes place at the output net. On the other hand, the presence of coupled inductors allows a significant portion of the interleaving and ripple cancellation to propagate upstream into each individual phase current.

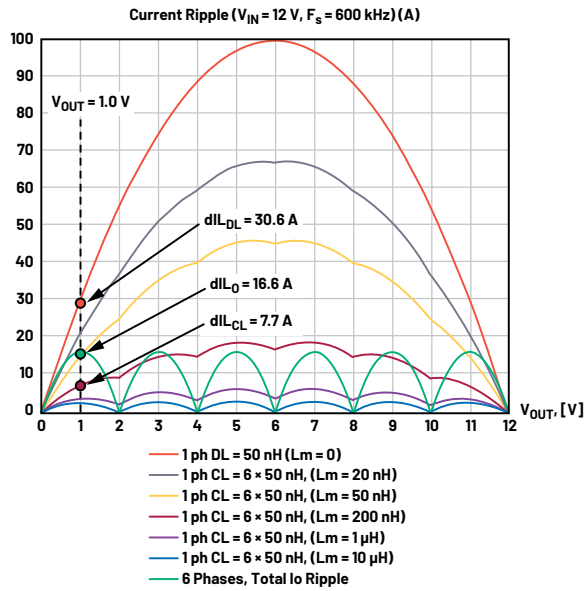

Figure 6. Calculated current ripple vs. V_{OUT} for 6-phase V_{IN} = 12 V buck (F_s = 600 kHz) with 50 nH inductors and different L_m. The total output current ripple is shown in green, same for all L_m values.

Notice that all curves in Figure 6 correspond to the same maximum current slew rate limit (and therefore transient), defined by the 50 nH inductance value in each phase.

Output Voltage Ripple

A simplified understanding of output voltage ripple assumes that the total output current ripple passes through the effective equivalent series resistance (ESR) of the output capacitance bank, resulting in a directly proportional voltage drop. This voltage drop manifests as a steady-state voltage waveform at the output of the converter. A more detailed analysis would entail considering the actual capacitance in each output capacitor, along with capacitor parasitics and layout parasitics. However, the general expectation is that a higher total current ripple at the output will lead to the higher output voltage ripple. This could pose a limiting factor for CL. The phase current ripple in figures 3 to 5 is shown for comparison under apples-to-apples conditions, illustrating the same total output current ripple for the same inductance values. However, in practical applications, a DL ripple of 30.6 A as shown in Figure 3a may exceed the typical target range for 30 A to 50 A load current per phase. In such scenarios, the F_s would be higher or the DL value would be increased. Utilizing the benefits of CL often entails maintaining a comparable (and acceptable) phase current ripple between DL and CL designs. The advantage of CL manifests either in significantly lower F_s for higher efficiency or in a smaller inductance value, facilitating the faster transient and reducing the size of the output capacitance.[8] This means that while the current ripple inside the phase would be comparable between DL and CL—the total output current ripple of the CL solution could be higher.

However, several factors should be taken into account. The typical multiphase solution usually has the power stages lined up in a row, followed by inductors and then output capacitors. This layout applies similarly when using CL. Consequently, the V_{OUT} net isn't a single connection point in simulation, but a distributed network where phase currents are injected at varying distances. The capacitors are also distributed along the row of V_{OUT} inductor leads, with associated parasitics within and between them. The distributed network of parasitics in layout and output capacitors effectively filters waveforms from distant phases more rapidly. As a result, individual capacitors conduct more current ripple from nearby V_{OUT} inductor pins than from those further away. Since ceramic capacitors typically have minimum impedance above 1 MHz to 2 MHz, current ripple with the main F_s < 1 MHz harmonic (DL, Figure 3a) may be attenuated less compared to waveforms with multiple current peaks per the switching period (for example, CL; Figure 4b). Additionally, considering the poles created by ESL and ESR of the output capacitors, along with layout parasitics, a larger attenuation of the waveform with higher frequency content is also expected.

Another factor is that even though the total output current ripple of CL could be mathematically larger than such from DL: the local phase currents will be comparable, in fact often the CL phase ripple current will have somewhat smaller amplitude. The CL is effectively bringing current ripple cancellation from the output V_{OUT} net (in DL case) up to each switching phase.

Figure 7 shows a typical component placement and layout of the multiphase buck converter, where the output voltage rail is provided to some CPU or GPU load (socket area is shown by the large rectangular outline). The output capacitor array is located under the specified load area.

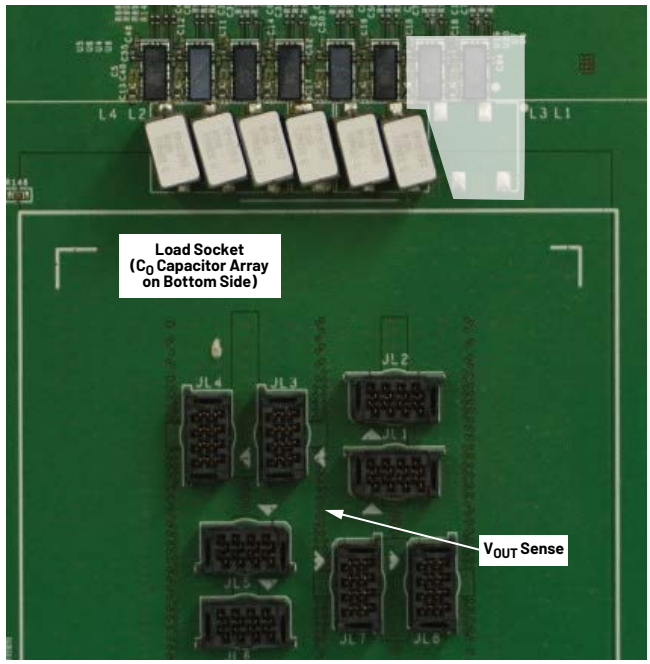

Figure 7. Board layout with multiphase buck. Six discrete inductors are loaded.

Figure 8 shows the V_{OUT} voltage ripple at the voltage sense point in the middle of the load socket in Figure 7 in the following conditions: V_{IN} = 12 V, V_{OUT} = 1 V, F_s = 600 kHz. Initially, DL = 100 nH is loaded into six phases of the voltage regulator, resulting in a maximum voltage ripple of 10.11 mV (Figure 8a). Placing CL = 6× 100 nH results in a slightly improved measurement of 10.05 mV max (Figure 8b). Then loading CL = 6× 50 nH into the inductor footprint for a better transient shows only a slightly increased ripple of 14.91 mV (Figure 8c). This is a negligible increase, especially considering that the typical limiting factor for the minimum output capacitance is the fast transient conditions, not the V_{OUT} ripple.

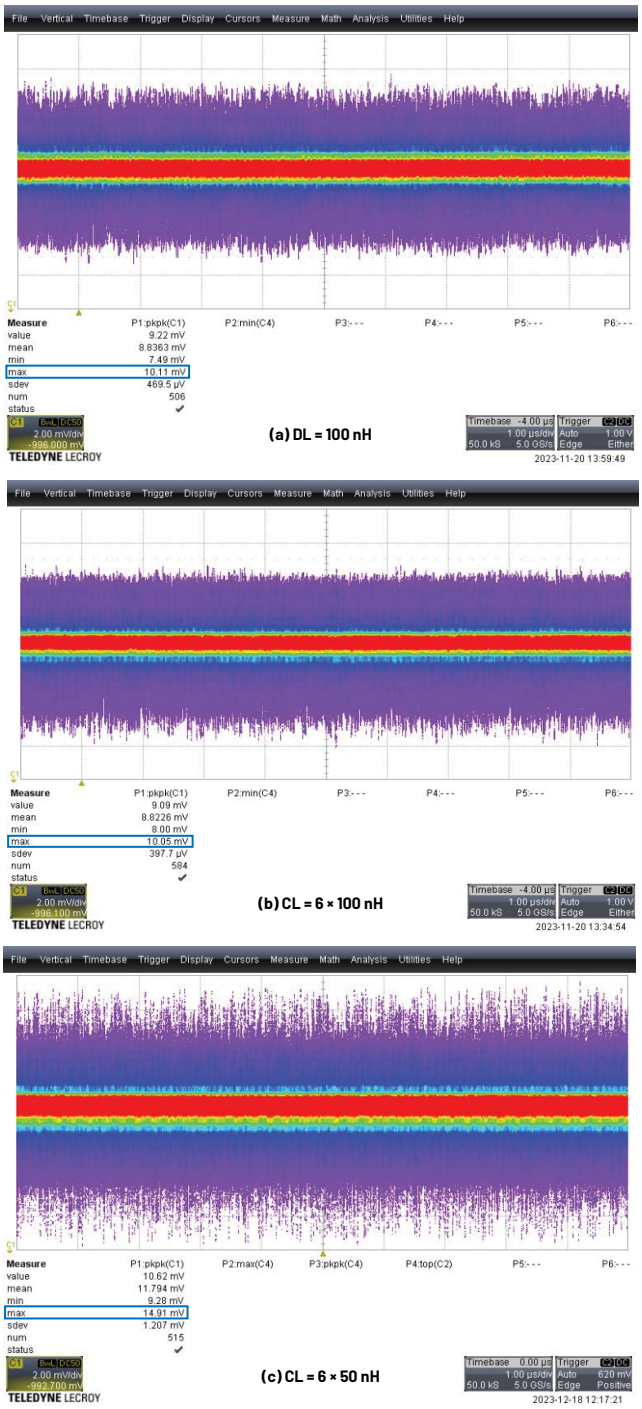

Figure 8. V_{OUT} ripple with 6-phase buck (12 V to 1 V, 600 kHz) at V_{OUT} sense in the CPU socket: (a) DL = 100 nH, 10.11 mV MAX, (b) CL = 6× 100 nH, 10.05 mV MAX, (c) CL = 6× 50 nH, 14.91 mV MAX.

The phase current ripple of CL = 6× 50 nH is only 7.7 A as shown in Figure 4b or Figure 6. Reducing the high current ripple of 30.6 A for DL = 50 nH by increasing the value to DL = 100 nH results in a proportional decrease to 15.3 A, which is an improvement (though at the cost of transient response). However, it remains twice as large as the ripple in CL = 6× 50 nH. Therefore, choosing DL = 100 nH will still impact efficiency.

Transient Performance

As the 6-phase CL = 6× 50 nH would have a big advantage in current ripple over the DL = 50 nH with a similar transient performance, the value of the discrete inductor is increased to DL = 100 nH to decrease the ripple difference at least partially with CL = 6× 50 nH. The resulting transient is compared in Figure 9.

Measurements were done with the same conditions of V_{IN} = 12 V, V_{OUT} = 1 V, F_s = 600 kHz. In order to showcase undershoot and overshoot of the output voltage, the loadline setting was changed for a smaller droop of 0.132 mΩ. The approach to showcase the voltage overshot is easier than that of removing some output capacitors. As expected with low V_{OUT} (for example, $V_{OUT} < V_{IN}/2$), the overshoot dominates the peak-to-peak transient performance of the output voltage.

For the load step of 240 A (40 A per phase), the output voltage peak-to-peak is dV_{OUT} = 81.2 mV for CL = 6× 50 nH (Figure 9a), and dV_{OUT} = 153.3 mV for DL = 100 nH (Figure 9b). Notice the PWM signals on top of the waveforms in Figure 9: even though the feedback loop is never instantaneous, the overshoot corresponds to the complete absence of the PWM pulses. This means that all phases are pulled down without any switching events and the transient performance is limited only by the current slew rate in the inductors themselves. This explains a roughly 2× measured difference in output voltage peak-to-peak between CL = 6× 50 nH and DL = 100 nH.

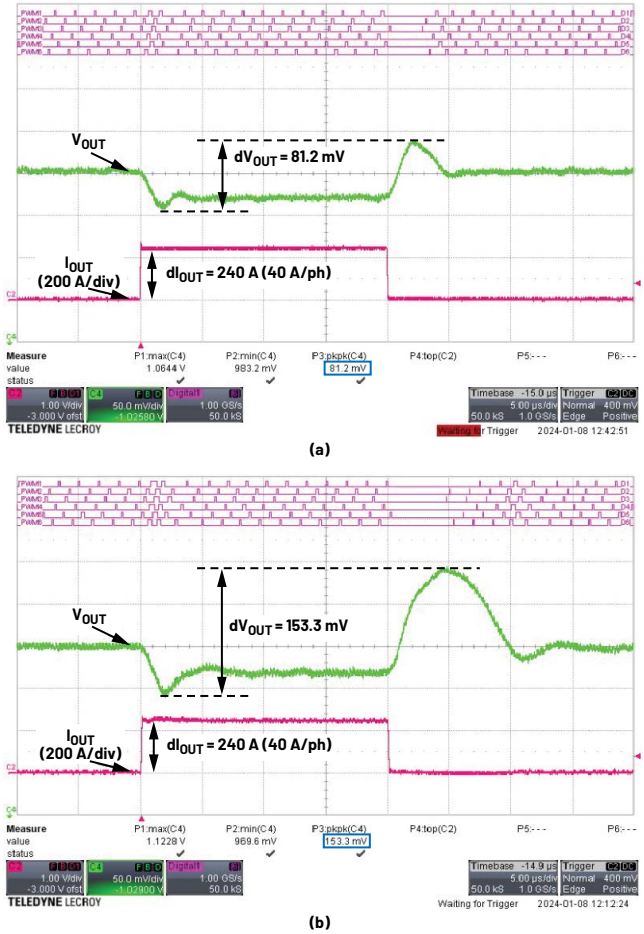

Figure 9. Transient performance for 6-phase buck where V_{IN} = 12 V, V_{OUT} = 1 V, F_s = 600 kHz, and 240 A load step: (a) CL = 6× 50 nH, (b) DL = 100 nH. The same board, same output capacitance and same lowered loadline setting of 0.132 mΩ.

Looking at the Figure 9 waveforms, the V_{OUT} ripple is not a concern as the aggressive transient excursions dominate the output voltage peak-to-peak. The minimum output capacitance will be defined by the transient specs, not the V_{OUT} ripple.

In a real application, the slower DL = 100 nH would require close to 2× more output capacitance to satisfy the same V_{OUT} peak-to-peak transient specifications as compared to CL = 6× 50 nH. At the same time, the DL = 100 nH would still have 2× larger current ripple if the same switching frequency is used. This could affect efficiency for two reasons: either due to large current ripple causing increased rms in current waveforms across the circuit and higher AC losses in DL, or due to higher switching frequency needed to reduce ripple, leading to proportionally higher switching losses.

Conclusion

Coupled inductor technology enables a variety of system benefits compared to the conventional approach, and these advantages can be optimized for many different priorities and applications.[8-10] However, an intriguing and counterintuitive fact is that the total current ripple of a multiphase buck converter remains the same for discrete and coupled inductors with identical inductance values. Leveraging the benefits of CL often results in an increase in the total output current ripple, despite typically reducing the current ripple in each phase. However, this potential drawback is generally mitigated by CL effectively pulling the phase interleaving from the output of the converter upstream into each phase, as well as by the filtering properties of the distributed Co tank. In other words, even if the total output current ripple of the solution with CL is purposely increased, it is better mixed among the physically separated V_{OUT} leads of the different phases, compared to DL. Also, the individual phase currents of CL typically have a higher frequency content and lower peak-to-peak, so they are often filtered better in the distributed network of the output capacitors and layout parasitics. This typically results in a very minor increase of V_{OUT} ripple when the CL advantage is utilized for a better transient or efficiency.

In many multiphase applications, the minimum amount of the output capacitance is often defined by the large and fast transient step specifications rather than considerations for the V_{OUT} ripple. This makes the total current ripple considerations even less important. As the number of phases (N_{ph}) increases for larger load current specifications, there's a general trend to note: the transient steps are expected to grow proportionally with N_{ph}, leading to a proportional increase in the minimum required output capacitance. However, the total current ripple at the output decreases significantly with the increase of interleaved phases in parallel. This holds true for both DL and CL and generally reduces the significance of output voltage ripple considerations. As a CL solution is typically associated with a faster transient and/or higher efficiency, a potential increase of the total output current ripple is typically not a significant design factor. However, it is good practice to check the V_{OUT} ripple performance in applications with slow transient and low N_{ph}, where V_{OUT} ripple rather than transient response might be a dominating factor dictating the minimum required output capacitance.

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Alexandr Ikriannikov is a fellow for the Communications and Cloud Power Team at Analog Devices. He received his Ph.D. degree in electrical engineering from the California Institute of Technology in 2000, where he studied power electronics from Dr. Slobodan Ćuk. His graduate school projects ranged from power factor correction for AC-to-DC applications to 15 V to 400 V DC-to-DC for Mars rovers. After graduate school he joined Power Ten to redesign and optimize multi-kW AC-to-DC power supplies, then in 2001 joined Volterra Semiconductor, concentrating on low voltage high current applications and coupled inductors. Volterra was acquired by Maxim Integrated in 2013, which is now part of Analog Devices. Currently, Alexandr is a senior member of IEEE. He holds more than 70 issued U.S. patents plus more pending and has authored multiple publications in the field of power electronics.