ADF4193 PLL Loop Filter Design Using ADI SimPLL

Technical Note

ADF4193-TN-001

GENERAL DESCRIPTION

This Technical Note shows how ADI SimPLL can be used to design the loop filter for a PLL using the ADF4193.

This is illustrated using a worked example of a GSM/DCS-1800 TX synthesizer. The SimPLL file used in this example may be downloaded from the ADF4193 Product Page on the web.

Following the recommendations in the Applications section of the ADF4193 datasheet, a 13MHz PFD frequency with a 60kHz final loop bandwidth is chosen for the GSM TX synthesizer.

LOOP FILTER DESIGN STEPS

1. Use SimPLL to design the filter for desired loop BW (60kHz in this example) with a 45° phase margin.
2. Adjust the value of R2 from the default 1k to 1.8k so that value of L1 is approx 2.2mH. The 2.2mH inductor is recommended as the value of R3 becomes too small with the next available inductor value of 1.5mH and is thus dominated by the SW3 Ron.
3. Select Tools-> Build This results in the loop filter component values of Figure 1.

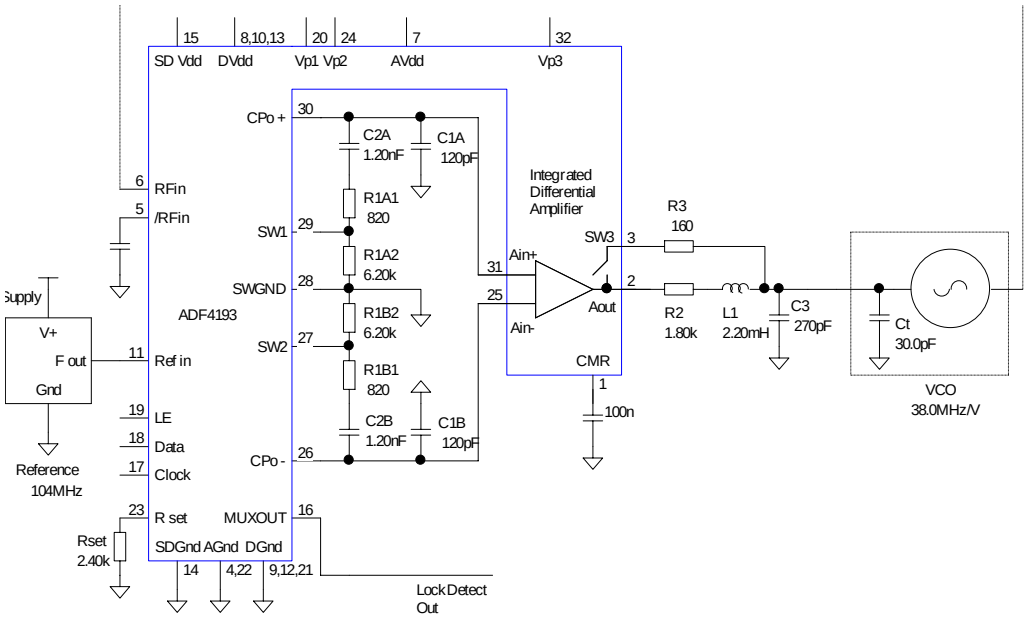

Figure 1. Initial Loop filter Design

In this example the input reference noise is set at -130dBc/Hz by selecting Reference-> Phase Noise -> Point/Floor.

VCO noise is also added by selecting VCO -> Phase Noise -> Point/Floor. The phase noise at 100kHz is set to -105dBc/Hz, which results in a phase noise of -145dBc/Hz two decades up at 1MHz offset. This results in the SSB Phase Noise shown in Figure 2. Also the VCO input capacitance is set to 30pF.

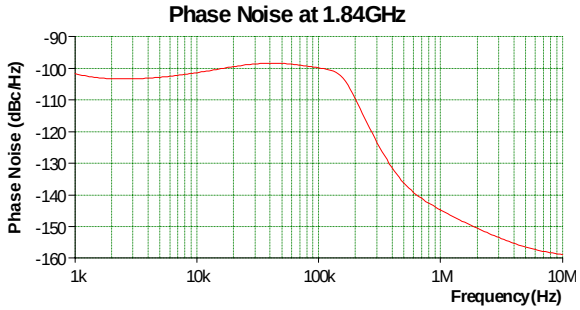

Figure 2. Phase Noise Profile in Initial Design

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The fast lock timers can be updated in ADI SimPLL by selecting Chip -> Speedup Mode -> SW R1 8xBW. Following the recommendations in the ADF4193 datasheet for a GSM TX synthesizer, the ICP timeout is set to 28 (~8.6us with a 13MHz PFD frequency) and the SW timeout is set to 35 (~10.8us). With these timer values the charge pump current is reduced from 64 × 104 uA to 1 × 104 uA, in 6 binary steps after ~8.6us. ADI SimPLL shows this in the Phase Detector Output plot.

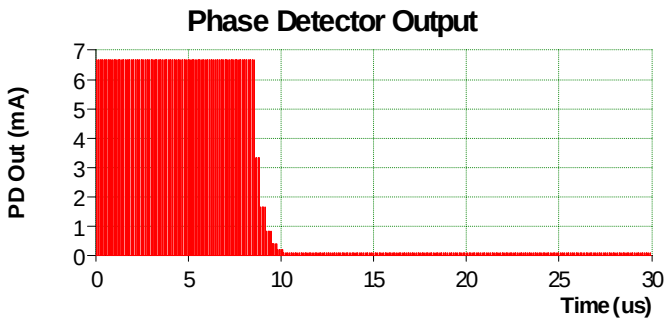

Figure 3. Phase Detector Output plot from ADI SimPLL

The frequency and phase settling plots from ADI SimPLL with these timer values are as follows:

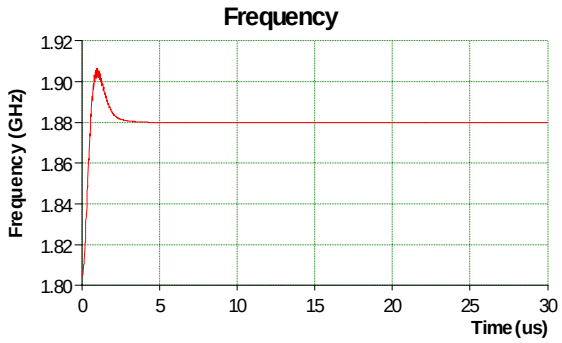

Figure 4. Frequency Settling Transient for a 75MHz Jump across the DSC-1800 TX Band

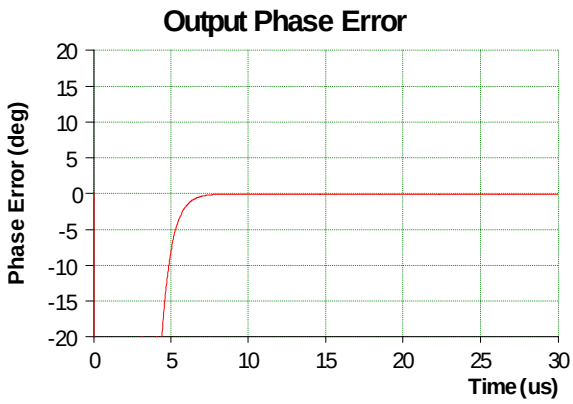

Figure 5. Phase Settling Transient for a 75MHz Jump across the DCS-1800 TX Band

IMPROVED SPUR SUPPRESSION

The differential amplifier and loop filter switches provided on the ADF4193 provide an additional degree of freedom in the loop filter design that can be taken advantage of for increased suppression of out-of-band spurs and noise from the PLL.

Since the optimum 45° phase margin for fast settling is only needed in wide BW mode, extra spur and noise attenuation can be achieved in narrow BW mode by increasing C3. E.g. from 270pF to 470pF. The will change the wide BW phase margin slightly so R3 should be reduced to restore it to 45°. E.g. from 180 to 62 ohms. The phase margin in wide BW mode can be observed by selecting Chip->Mode-> FL always and placing the marker where the wide BW open loop gain is at 0dB, as shown in Figure 6.

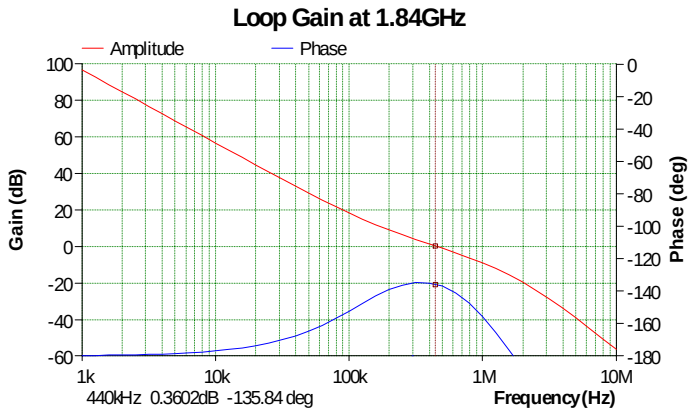

Figure 6. Loop Gain and Phase in Wide BW Mode

Phase Margin = 180° - 135.8° = 44.2°

The improved attenuation of out-of-band noise from the PLL and spurs at offsets >100kHz can be seen in the blue trace of Figure 7. The phase noise eventually becomes dominated by VCO noise at offset frequencies >400kHz, however the improvement in spur attenuation extends beyond this, up to the self resonant frequency of the 2.2mH inductor (~2MHz). The VCO noise contribution can be easily turned off in the simulator by selecting Tools -> Individual Noise Control.

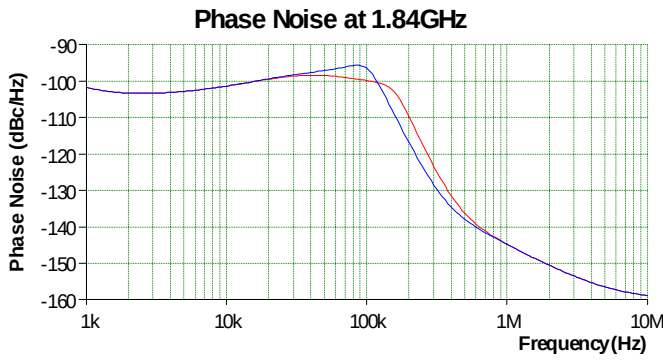

Figure 7. SSB Phase Noise Plots

The improvement in far out attenuation is achieved with no significant degradation to the lock time performance (see below plots). This is because the phase margin in wide BW mode is still at the optimum value of 45 degrees. The narrow BW phase margin can be reduced down to 30° without any noticeable impact on settling time. Going lower than this may give rise to a slight ripple in the settled phase when the BW is reduced.

The final loop filter values for 60kHz/26MHz PFD are shown in Figure 11. Figures 8 to 10 show the new frequency and phase settling transients in blue overlaid on the original transients in red.

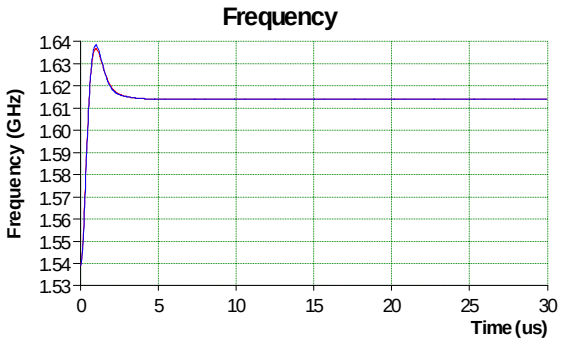

Figure 9. Frequency Settling Transients

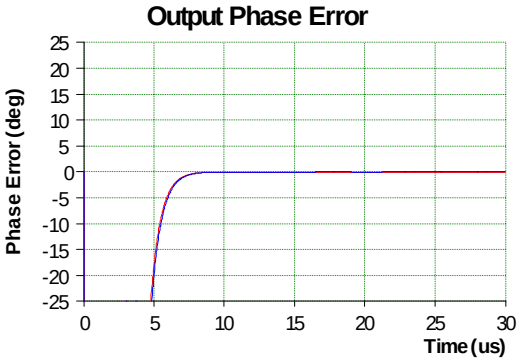

Figure 8. Phase Settling Transients

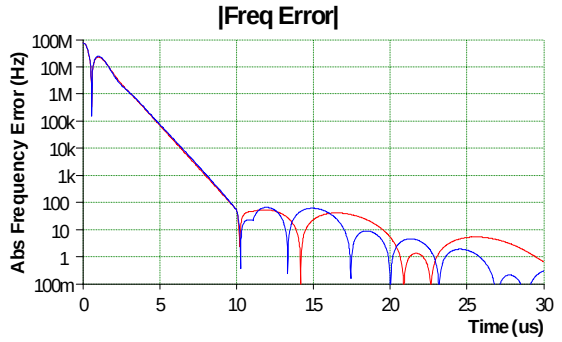

Figure 10. Frequency Error Plots

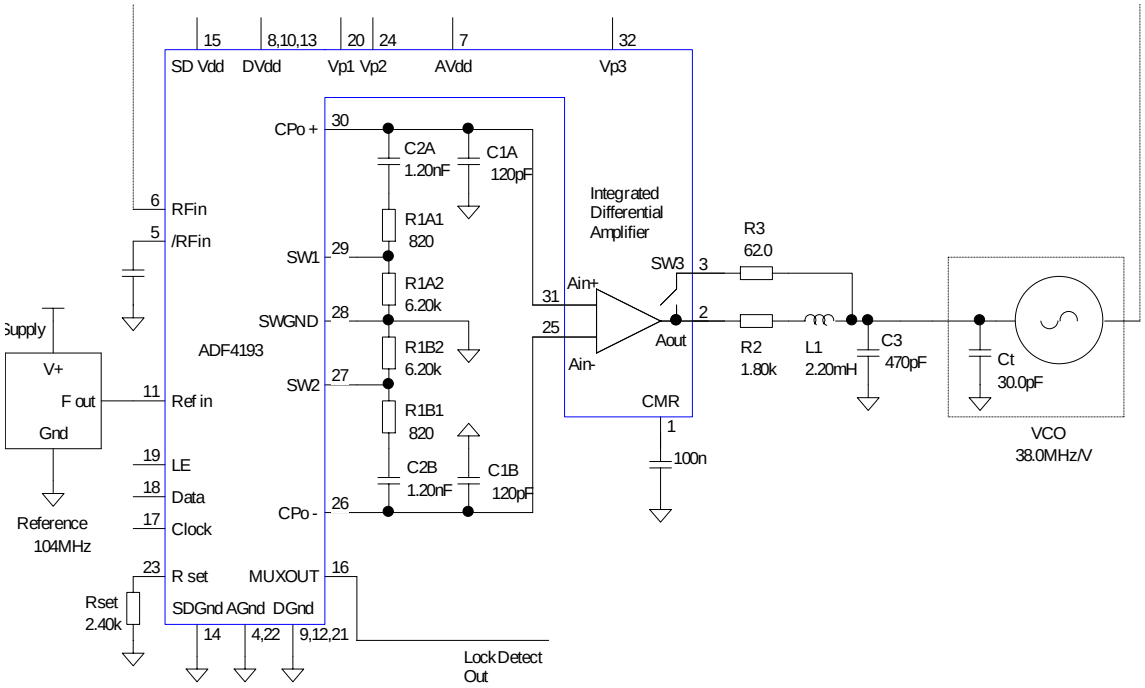

Figure 11. Loop Filter Components for a DCS1800 TX Synthesizer