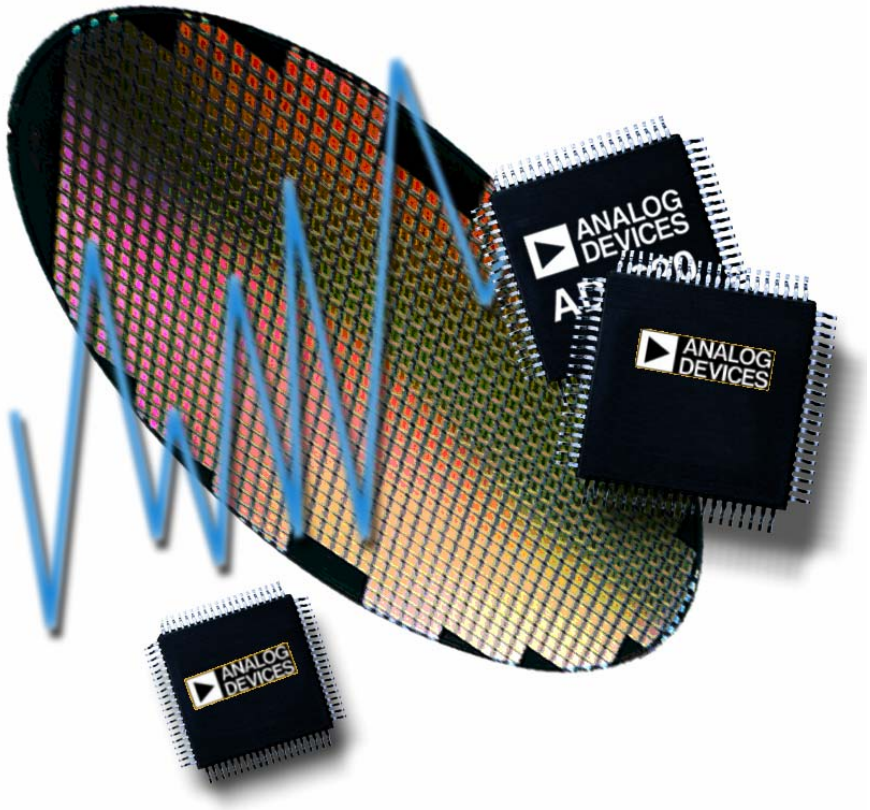

Reliability Report

Report Title: 8inch ADLK 3um 30V SPSM BiCMOS Q Process Qualification Report

Report Number: 4731

Date: 3 Nov 2008

Analog Devices Reliability. Raheen Industrial Park . Limerick, Ireland
Tel: 353.61.229011 Fax: 353.61.303891 www.analog.com

Introduction

This report covers the qualification of the 8inch ADLK 3um 30V SPSM BiCMOS Q process, transferred from the equivalent 6inch process technology. The products used to release this process are AD7243/33, ADG201HS and AD7839. Additional ESD classification was performed on ADM3222 AD5521, AD7572 and ADM206E. The ESD classification of these seven generics covered the full spectrum of product designs (ADC, DAC, Switch and Interface) from this process. The AD7839 is detailed in RQR02375.

The following products have been released from the 8inch ADLK 3um 30V SPSM BiCMOS Q process based on data substitution, AD7226, AD7225, PM7226, ADM1385, PM7528, AD7528, AD7538, ADG408/9, ADM242/222, ADM2209E, AD7534, AD7237/A, ADG409, AD7849, AD7846, ADM3222, ADM206E, ADM206, AD7841, AD5521, AD7533, AD7834, ADG411/431/511/661, ADG412/432/512/662, ADG413/433/513/663, ADG221/222, ADG201A, ADG212/202A., ADG419, ADG417, AD7247/A, AD7228/A, ADG451/2/3, ADG211A, AD7541A, AD7533, AD11/2009, AD7841, AD7835, AD7537, AD5532, AD5532HS, AD7543, ADG428, AD7549, AD7224, AD7524, AD7837, AD7847, ADM233L, AD5532ABC-3, AD5532ABC-2, AD5532ABC-5, AD5532HS, AD5532ABC-1, AD5533ABC-1, AD5516-2, AD5516-1, AD7845, AD7835, ADG509A, ADG508A, AD7537, AD7547, AD7836, AD5520, AD5570, AD7542, AD7548, AD7628, AD7245, AD2S99, AD79021, ADP667, ADM5170, AD7249, AD79012, AD7548MIL ADG509AMIL, AD79019, AD7543MIL and the AD79011.

Product Description

The AD7243 is a complete 12-bit, voltage output, digital-to-analog converter with output amplifier and Zener voltage reference on a monolithic CMOS chip. No external trims are required to achieve full specified performance.
The output amplifier is capable of developing +10V across a 2k(Ohm) load. The output voltage ranges with single supply operation are 0 to +5 V or 0 to +10V, while an additional bipolar ±5 V output range is available with dual supplies. The ranges are selected using the internal gain resistor.

The ADG201HS is a monolithic CMOS device comprising four independently selectable switches. They are designed on an enhanced LC^2MOS process, which gives an increased signal handling capability of ±15 V. These switches also feature high switching speeds and low RON.
The ADG201HS switches are turned on with a logic low on the appropriate control input. Each switch conducts equally well in both directions when ON and each has an input signal range that extends to the supplies. All switches exhibit break-before-make switching action for use in multiplexer applications. Inherent in the design is low charge injection for minimum transients when switching the digital inputs.

Device Characteristics

Part Number	AD7243
Die Size (mm)	2.60 x 4.30
Wafer Fabrication Site	ADI-Limerick
Wafer Fabrication Process	Q3 SPSM
Transistor Count	1300
Maximum Power Dissipation (W)	0.140
Worst Case Metal Line Current (mA/µm)	0.35e5 A/cm sq
Passivation Layer	Undoped-oxide/SiN
Bond Pad Metal Composition	AlCu

Part Number	ADG201HS
Die Size (mm)	1.8 x 1.9
Wafer Fabrication Site	ADI-Limerick
Wafer Fabrication Process	Q3 SPSM
Transistor Count	100
Maximum Power Dissipation (W)	0.00001
Passivation Layer	Undoped-oxide/SiN
Bond Pad Metal Composition	AlCu

Package/Assembly Characteristics

Available Packages	16-SOICWB	16-PDIP
Assembly Location	Carsem-S	Carsem-M
Package Die Attach	Ablestik 84-1LMIS R4	Ablestik 84-1LMIS R4
Leadframe Material	Copper	Copper
Package Bond Wire	Gold	Gold
Bond Wire Dia. (mils)	1.30	1.30
Package Molding Compound	Sumitomo 6600H	Sumitomo 6300H
Package Lead Finish	Tin / Lead Solder Plate	Tin / Lead Solder Plate

Description/Results of Tests Performed

Table 1 provides a description of the qualification tests conducted and the associated test results. Tests and sample sizes for the qualification of the 8inch ADLK 3um 30V SPSM BiCMOS Q process are based on the ADI specification ADI0012, "Procedure for the Qualification of New or Revised Processes or Packages." All qualification devices were chosen from standard material manufactured through normal production processes and were electrically tested at room temperature following each endpoint. Any device that did not meet all electrical data sheet limits following stressing would be considered a failure. As Table 1 indicates no failures occurred during qualification of the 8inch ADLK 3um 30V SPSM BiCMOS Q process.

Table 1. 8inch ADLK 3um 30V SPSM BiCMOS Q Qualification Results

Test Name	Conditions	Duration	Package Type	Lot #	Sample Size	Qty. Rejects
Autoclave* ADG201HS	121C 100%RH 2atm	168hrs	16-PDIP	M61836.1	45	0
				M61837.1	45	0
				M61838.1	45	0
Autoclave* AD7243	121C 100%RH 2atm	168hrs	16-SOICWB	M61852.1	45	0
				M61853.1	45	0
				M61854.1	45	0
Early Life Failure ADG201HS	TJ = NAC	168hrs	16-PDIP	M61638.1	300	0
				M61836.1	300	0
				M61837.1	300	0
Early Life Failure AD7243	TJ = NAC	168hrs	16-SOICWB	M64173.1	300	0
				M64175.1	300	0
				M64174.1	300	0
Early Life Failure AD7572	TJ = 125	168hrs	24-PDIP	N92056.1	100	0
				N92057.1	100	0
				N92058.1	100	0
High Temperature AD7572	TJ = 125	1000hrs	24-PDIP	N92056.1	45	0
				N92057.1	45	0
				N92058.1	45	0
High Temperature Operating Life ADG201HS	TJ = NAC	500hrs	16-PDIP	M61802.1	45	0
				M61803.1	45	0
				M61801.1	45	0
High Temperature Operating Life AD7243	TJ = NAC	1000hrs	16-SOICWB	M64176.1	45	0
				M64177.1	45	0
				M64178.1	45	0
High Temperature Storage ADG201HS	150C	1000hrs	16-PDIP	M66440.1	45	0
				M66441.1	45	0
				M66439.1	45	0
High Temperature Storage AD7243	150C	1000hrs	16-SOICWB	M66443.1	45	0
				M66444.1	45	0
				M66442.1	45	0

Highly Accelerated Stress Test* ADG201HS	130C 85%RH 2atm, Biased	96hrs	16-SOICnb	M72809.1	45	0
				M72808.1	45	0
				M72810.1	45	0
Temperature Cycle* ADG201HS	-65C/+150C	500cycles	16-PDIP	M61842.1	45	0
				M61843.1	45	0
				M61844.1	45	0
Temperature Cycle* AD7243	-65C/+150C	500cycles	16-SOICWB	M61859.1	45	0
				M61860.1	45	0
				M61858.1	45	0
Unbiased Highly Accelerated Stress Test* AD7243	130C 85%RH 2atm	96hrs	16-SOIC	M61856.1	45	0
				M61857.1	45	0
				M61855.1	45	0

Noted samples (*) were subjected to preconditioning (per J-STD-020B Level 3) prior to the start of the stress test. Level 3 preconditioning consists of the following:

- Bake: 24 hrs @ 125°C
- Unbiased Soak: 192 hrs @ 30°C, 60%RH
- Reflow: 3 passes through a convection/IR oven with a peak temperature of 240 +0/-5°C for a minimum of 10 seconds.

ESD Testing Results

The results of ESD testing are summarized in Table 3. As accept/reject criteria, all samples were electrically tested to data sheet limits before and after ESD stressing.

Human Body Model (HBM) ESD Sensitivity Classification testing was conducted on the AD7243, ADG201HS, ADM3222, ADM206E, AD7572 and AD5521 using a KeyTek Verifier V3 Test System. During HBM testing of a given sample, one positive and one negative discharge was applied to each of the following pin combinations:

(1) Every individual pin to each power supply
(2) Every individual pin to each ground
(3) Every individual I/O pin to the group of all other I/O pins.

Field-Induced (Robotic) Charged Device Model (FICDM) ESD Sensitivity Classification testing was conducted using a Verifier Robotic CDM Test System. During FICDM testing of a given sample, the device package was charged via a field plate and a discharge pin made contact with each individual device pin to discharge it through a 1Ω resistor to ground. Three positive and three negative discharges were applied to every pin.

The ADM206E was tested to IEC 1000-4-2 standards. During testing all I/O pins are tested to ground. The intention is to test the transmitter and receiver to IEC 1000-4-2, using a Key Tek tester.

Table 3. ESD Characterization Results*

ESD Model	Package	ESD Test Spec	RC Network	Highest Pass Level	First Fail Level	Class
FICDM ADG201HS	16-PDIP	ESD Assoc. STM5.3.1-1999	1Ω, Cpkg	1500V	-----	C6
FICDM AD7243	16-SOICWB	ESD Assoc. STM5.3.1-1999	1Ω, Cpkg	500V	1000V	C4
FICDM ADM3222	20-SSOP	ESD Assoc. STM5.3.1-1999	1Ω, Cpkg	1500V	-----	C6
FICDM ADM206E	24-SOIC	ESD Assoc. STM5.3.1-1999	1Ω, Cpkg	1500V	-----	C6
FICDM AD7572	24-PDIP	ESD Assoc. STM5.3.1-1999	1Ω, Cpkg	1500V	-----	C6
FICDM AD5521	80-TQFP	ESD Assoc. STM5.3.1-1999	1Ω, Cpkg	1500V	-----	C6
HBM AD7243	16-SOICWB	ESD Assoc. STM5.1-1998	1.5kΩ, 100pF	2500V	3000V	2
HBM ADG201HS	16-PDIP	ESD Assoc. STM5.1-1998	1.5kΩ, 100pF	4000V	----	3A
HBM ADM3222	20-SSOP	ESD Assoc. STM5.1-1998	1.5kΩ, 100pF	4000V	----	3A
HBM ADM206E	24-SOIC	ESD Assoc. STM5.1-1998	1.5kΩ, 100pF	4000V	----	3A
HBM AD7572	24-PDIP	ESD Assoc. STM5.1-1998	1.5kΩ, 100pF	1000V	1500V	1
HBM AD5521	80-TQFP	ESD Assoc. STM5.1-1998	1.5kΩ, 100pF	4000V	----	3A
IEC ADM206E Contact	24-SOIC	IEC 1000-4-2	330Ω, 150pF	+/-8,000	------	4

Discharge						
IEC ADM206E Air Discharge	24-SOIC	IEC 1000-4-2	330Ω, 150pF	+/-15,000	------	4

*ADI measures ESD results using stringent test procedures based on the specifications listed in the above table. Any comparison with another supplier's results should ensure that the same ESD test procedures have been used. For further details, please see the EOS/ESD chapter of the ADI Reliability Handbook at http://www.analog.com/corporate/quality/manuals/.

Latch-Up and Electrical Overstress Testing Results

The AD7243, ADG201HS, AD7572 and AD5521 was tested for Class I static latch-up conditions using the test method outlined in JEDEC Standard Number 78. The result summary is shown below:

- No latch-up occurred during testing of each individual input and output pin in which both positive and negative current pulses (50µs risetime, 5ms duration) were applied up to Inorm +115mA / -105mA for AD7243, Inorm +121mA / -101mA for ADG201HS, Inorm +121mA / -111mA for AD7572 and Inorm +151mA / -121mA for AD5521. This input and output latch-up testing was conducted initially with all input pins at Vin minimum levels, and subsequently with all input pins at Vin maximum levels.
- No latch-up occurred during testing of the supply pin groups in which voltage pulses (50µs risetime, 5ms duration) were applied up to 24.8V for AD7243 and ADG201HS, up to 24V for AD7572 and AD5521. This over voltage latch-up testing was conducted initially with all input pins at Vin minimum levels, and subsequently with all input pins at Vin maximum levels.

The devices that were subjected to the latch-up test criteria all passed post-latch-up electrical testing.

Additional Qualification Data

Reliability qualification testing has been conducted on other products manufactured on the same technologies as the 8inch ADLK 3um 30V SPSM BiCMOS Q process.

Samples of some of the many device types manufactured with these technologies are continuously undergoing reliability evaluation as part of the ADI Reliability Monitor Program. This additional qualification data, as well as FIT data, is available on Analog Devices' web site at http://www.analog.com/corporate/quality/read/1stpage.html.

Conclusion

The qualification of the 8inch ADLK 3um 30V SPSM BiCMOS Q process has successfully completed and is released for production.

The following products have been released based on qualification data or data substitution, AD7234/33, ADG201HS, AD7839, AD7226, AD7225, PM7226, ADM1385, PM7528, AD7528, AD7538, ADG408/9, ADM242/222, ADM2209E, AD7534, AD7237/A, ADG409, AD7849, AD7846, ADM3222, ADM206E, ADM206, AD7841, AD5521, AD7533, AD7834, ADG411/431/511/661, ADG412/432/512/662, ADG413/433/513/663, ADG221/222, ADG201A, ADG212/202A., ADG419, ADG417, AD7247/A, AD7228/A, ADG451/2/3, ADG211A, AD7541A, AD7533, AD11/2009, AD7841, AD7835, AD7537, AD5532, AD5532HS, AD7543, ADG428, AD7549, AD7224, AD7524, AD7837, AD7847, ADM233L, AD5532ABC-3AD5532ABC-2, AD5532ABC-5, AD5532HS, AD5532ABC-1, AD5533ABC-1, AD5516-2, AD5516-1, AD7845, AD7835, ADG509A, ADG508A, AD7537, AD7547, AD7836, AD5520, AD5570, AD7542, AD7548, AD7628, AD7245, AD2S99, AD79021, ADP667, ADM5170, AD7249, AD79012, AD7548MIL ADG509AMIL, AD79019, AD7543MIL and the AD79011.

Approvals

Reliability Engineer: James Molyneaux
This report has been approved by electronic means (1.8).

Additional Information

Data sheets and other additional information are available on Analog Devices' web site at the addresses shown below.

Home Page:	http://www.analog.com
Sales Info:	http://www.analog.com/world/corp_fin/sales_directory/distrib.html
Reliability Data:	http://www.analog.com/corporate/quality/read/1stpage.html
Reliability Handbook:	http://www.analog.com/corporate/quality/manuals/