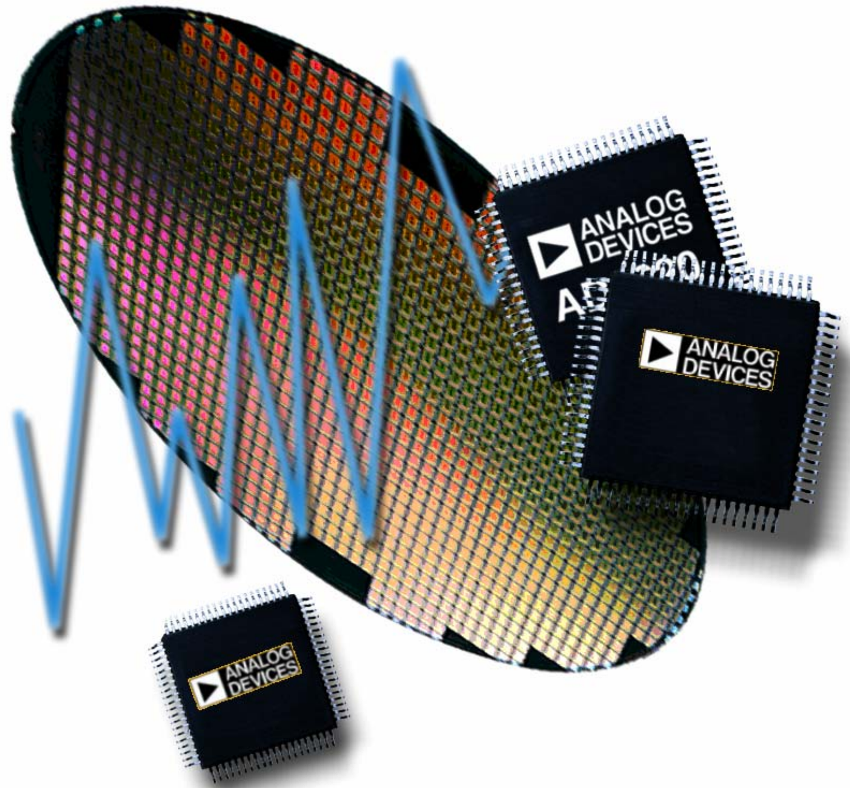
ANALOG DEVICES



Reliability Report

Report Title: ADLK 8V2DPDMR (HVBP2) Process Qualification

Report Number: 5998

Date: 19 September 2007

Analog Devices Reliability . Gateway Business Park, Special Economic Park, Javelera, Gen. Trias . Cavite, Philippines
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Summary

This report documents the successful qualification requirements for release of the ADLK 8V2DPDMR (HVBP2) process. The generics used for the qualification are the AD8675, ADA4004-4, and ADR127 products in a 6-TSOT, 8-SOICnb, and 14-SOICnb package.

This report details qualification results for both the product level qualifications and device level qualifications.

Section A: Covers the Product Level Qualification.

Section B: Covers the Device Level Qualification.

Section A: Product Level Qualification Data

The AD8677 qualification in 8-SOICnb is also covered in this report. The qualification plan for the AD8677 is RQR04075A (#6417). The AD8677 is the fourth product to be qualified for the Limerick 8V2DPDMR process release and results are also shown below.

The AD8675 precision amplifier has ultra-low offset, drift and voltage noise combined with very low input bias currents over the full operating temperature range. The AD8675 is a precision, wide bandwidth amplifier featuring rail-to-rail output swings and very low noise. Operation is fully specified from ±5V to ±15 volts.

The ADA4004-4 is a 1.8 nV/√Hz precision quad amplifier featuring 40 µV offset, 0.7 µV/ºC drift, 12 MHz bandwidth, and low 1.7 mA/amplifier supply current.

Analog Devices' new ADR127 is a 1.25 V reference providing high precision, low power, and low voltage. A perfect companion chip for high accuracy data converters in power constraint applications, the ADR127 offers the lowest temperature drift performance over the extended industrial temperature range of -40ºC to +125ºC while only consuming 85 µA. Its low input and output voltage capability ensures that it's the ideal solution for our latest generation of high performance CMOS converters in handheld portable instrumentations. The combination of precision, power, and low voltages makes the ADR127 ideally suited for battery operated instrumentations equipments.

The AD8677 is the next generation of precision, ultra-low offset amplifiers. Operation is fully specified from ±5 V to ±15 V supply.

Table 1. ADR127 Product Characteristics

Device

Maximum Power Dissipation (W)	0.001
Device / Die ID	2512Z
Die Size (mm)	.76 x 1.20
Wafer Fabrication Site	ADI-Limerick
Wafer Fabrication Process	8V2DPDMR
Passivation Layer	undoped-oxide/SiN
Bond Pad Metal Composition	AlCu

Package/Assembly

Available Package(s)	6-TSOT
Body Size (mm)	1.60 x 2.90 x .87
Assembly Location	Carsem-M
Die Attach	Ablestik 84-1LMIS R4
Lead Frame Material	Copper
Bond Wire Type	Gold Tanaka GLD
Bond Wire Dia. (mils)	0.80
Mold Compound	NITTO MP 8000CSM
Lead Finish	Tin Plate
Moisture Sensitivity Level	1
Maximum Peak Reflow (°C)	260C +0/-5C

Table 2. ADA4004-4 Product Characteristics

Device

Maximum Power Dissipation (W)	0.204
Device / Die ID	2510/Y
Die Size (mm)	1.73 x 1.70
Wafer Fabrication Site	ADI-Limerick
Wafer Fabrication Process	8V2DPDMR
Passivation Layer	undoped-oxide/SiN
Bond Pad Metal Composition	AlCu
Package/Assembly	
Available Package(s)	14-SOICnb
Body Size (mm)	4.00 x 8.75 x 1.50
Assembly Location	Amkor-P
Die Attach	Ablestik 8340

Lead Frame Material	Copper
Bond Wire Type	Gold
Bond Wire Dia. (mils)	1.20
Mold Compound	Sumitomo 6730B
Lead Finish	Tin Plate
Moisture Sensitivity Level	1
Maximum Peak Reflow (°C)	260C +0/-5C

Table 3. AD8675 Product Characteristics

Device	
Maximum Power Dissipation (W)	0.135
Device / Die ID	2503X
Die Size (mm)	1.32 x 1.32
Wafer Fabrication Site	ADI-Limerick
Wafer Fabrication Process	8V2DPDMR
Passivation Layer	undoped-oxide/SiN
Bond Pad Metal Composition	AlCu
Package/Assembly	
Available Package(s)	8-SOICnb
Body Size (mm)	4.00 x 5.00 x 1.50
Assembly Location	Amkor-P
Die Attach	Ablestik 8340
Lead Frame Material	Copper
Bond Wire Type	Gold
Bond Wire Dia. (mils)	1.20
Mold Compound	Sumitomo 6730
Lead Finish	Tin Plate
Moisture Sensitivity Level	1
Maximum Peak Reflow (°C)	260C +0/-5C

Table 4. AD8677 Product Characteristics

Device	
Maximum Power Dissipation (W)	0.135
Device / Die ID	2509X
Die Size (mm)	0.95 x 0.95
Wafer Fabrication Site	ADI-Limerick
Wafer Fabrication Process	8V2DPDMR
Passivation Layer	undoped-oxide/SiN
Bond Pad Metal Composition	AlCu

Package/Assembly	
Available Package(s)	8-SOICnb
Body Size (mm)	4.00 x 5.00 x 1.50
Assembly Location	Amkor-P
Die Attach	Ablestik 8340
Lead Frame Material	Copper
Bond Wire Type	Gold
Bond Wire Dia. (mils)	1.20
Mold Compound	Sumitomo 6730
Lead Finish	Tin Plate
Moisture Sensitivity Level	1
Maximum Peak Reflow (°C)	260C +0/-5C

Description/Results of Tests Performed

Table 4 provides a description of the qualification tests conducted and the associated test results on the AD8677, AD8675, ADA4004-4, and ADR127 and other products manufactured on the same technologies as described in the product characteristics tables.

Table 5: Package Qualification Test Results

Test Name	Conditions	Specification	Device	Package	Lot Num	Sample Size	Qty. Rejects
Autoclave [1]	121C 100%RH 2atm 168hrs	JEDEC-STD-22, Method A102	AD8675	8-SOICnb	f159516.7	79	0
				8-SOICnb	f159575.7	77	0
					F159642.7	70	0
			ADA4004-4	14-SOICnb	f159494.7	79	0
	121C 100%RH 2atm 96hrs	JEDEC-STD-22, Method A102	ADA4004-4		f159654.7	74	0
			ADR127	6-TSOT	AA40332.1	77	0
					AA40333.1	77	0
					AA71757.1	77	0
HTS	150C 1000hrs	JEDEC-STD-22, Method A103	AD8675	8-SOICnb	f159516.4	79	0
					f159575.4	79	0
					F159642.4	77	0
			ADA4004-4	14-SOICnb	f159494.4	80	0
					f159551.4	80	0
					f159654.5	80	0
			ADR127	6-TSOT	AA40336.1	77	0
					AA40337.1	77	0
					AA71759.1	77	0
SHR [1]	See Below	ADI-0049	AD8675	8-SOICnb	f159516.5	25	0
			ADA4004-4	14-SOICnb	f159494.5	25	0
			ADR127	6-TSOT	aa40338.1	20	0

					Lot Num	Sample Size	Qty. Rejects
					aa40338.1	20	0
Temp Cycle [1]	-65C/+150C 500cycles	JEDEC-STD-22, Method A104	AD8675	8-SOICnb	f159516.8	80	0
					f159575.8	79	0
					F159642.8	68	0
			ADA4004-4	14-SOICnb	f159494.8	79	0
					f159551.8	49	0
					f159654.8	79	0
Temp Cycle	-65C/+150C 500cycles	JEDEC-STD-22, Method A104	ADR127	6-TSOT	AA80831.1	77	0
Temp Cycle [1]	-65C/+150C 500cycles	JEDEC-STD-22, Method A104	ADR127	6-TSOT	AA40340.1	77	0
					AA40341.1	77	0
	-65C/+150C reconcycles	JEDEC-STD-22, Method A104	ADR127		AA71760.1	77	0
Unbiased HAST [1]	130C 85%RH 2atm 96hrs	JEDEC-STD-22, Method A118	ADA4004-4	14-SOICnb	f159916.5	79	0
					f160129.7	39	0

Note: Results table below is from RQR04075A (#6417)

Test Name	Conditions	Specification	Device	Package	Lot Num	Sample Size	Qty. Rejects
Autoclave [1]	121C 100%RH 2atm 96hrs	JEDEC-STD-22, Method A102	AD8677	8-SOICnb	AA20705.1	85	0
				8-SOICnb	AA20706.1	80	0
					AA20707.1	85	0
HTS	150C 1000hrs	JEDEC-STD-22, Method A103	AD8677	8-SOICnb	AA18037.1	80	0
					AA18038.1	80	0
					AA18039.1	80	0
SHR [1]	See Below	ADI-0049	AD8677	8-SOICnb	AA20711.1	20	0
Temp Cycle [1]	-65C/+150C 500cycles	JEDEC-STD-22, Method A104	AD8677	8-SOICnb	AA20702.1	80	0
					AA20703.1	80	0
					AA20704.1	80	0

[1]These Samples were subjected to preconditioning (per J-STD-020 Level 1) prior to the start of the stress test. Level 1 preconditioning consists of the following:

- Bake: 24 hrs @ 125°C
- Unbiased Soak: 168 hrs @ 85°C, 85%RH
- Reflow: 3 passes through an oven with a peak temperature of 260+0/-5°C

Samples of the many devices manufactured with this packaging technology are continuously undergoing reliability evaluation as part of the ADI Reliability Monitor Program. Additional qualification data is available on Analog Devices' web site at: http://www.analog.com/world/quality/read/1stpage.html.

Table 6: Process Qualification Test Results

Test Name	Conditions	Specification	Part Number	Lot Number	Sample Size	Qty. Rejects
ELF	125C 48hrs	MIL-STD-883, Method 1015	AD8675	f159516.3	630	0
				f159575.12	416	0
				f159575.3	209	0
				F159642.3	628	0
				f159654.10	59	0
				f159916.2	700	0
				f159928.2/6	700	0
				f160129.5/6	669	0
			ADR127	AA43211.1	500	0
				AA43212.1	499	0
				AA45565.1	165	0
				AA45566.1	165	0
				AA71229.1	170	0
				AA71229.2	447	0
				AA71229.3	53	0
HAST [1]	130C 85%RH 2atm, Biased 96hrs	JEDEC-STD-22, Method A110	AD8675	f159516.6	80	0
				f159575.6	80	0
				F159642.6	80	0
			ADR127	AA40334.1	77	0
				AA40335.1	77	0
				AA71758.1	77	0
Unbiased HAST [1]	130C 85%RH 2atm, Biased 96hrs	JEDEC-STD-22, Method A110	ADA4004-4	f159916.3	80	0
Unbiased HAST [1]	130C 85%RH 2atm, Biased 96hrs	JEDEC-STD-22, Method A110	ADA4004-4	f159928.3	80	0
HTOL	125C<Tj<135C, Biased 1000hrs	JESD22-A108	AD8675	f159516.9	46	0
				f159575.9	76	0
				F159642.5	80	0
			ADR127	AA37664.1	75	0
				AA37665.1	77	0
				AA71230.1	74	0
				F160129.8	80	0
				f160129.9	77	0
				f160129.4	80	0
				f159928.4	100	0

Note: Results table below is from RQR04075A (#6417)

Test Name	Conditions	Specification	Part Number	Lot Number	Sample Size	Qty. Rejects
ELF	125C 48hrs	MIL-STD-883, Method 1015	AD8675	AA13504.1	660	0
			AD8677	AA20920.1	564	0
				AA20920.2	101	0
				AA20921.1	564	0
				AA20921.2	101	0
				R88467.1	610	0
HAST [1]	130C 85%RH 2atm, Biased 96hrs	JEDEC-STD-22, Method A110	AD8677	AA20708.1	80	0
				AA20709.1	80	0
				AA20710.1	80	0
HTOL	125C<Tj<135C, Biased 1000hrs	JESD22-A108	AD8675	AA13505.1	85	0
			AD8677	AA20918.1	89	0
				AA20919.1	90	0
				R88468.1	90	0

[1]These Samples were subjected to preconditioning (per J-STD-020 Level 1) prior to the start of the stress test. Level 1 preconditioning consists of the following:

- Bake: 24 hrs @ 125°C
- Unbiased Soak: 168 hrs @ 85°C, 85%RH
- Reflow: 3 passes through an oven with a peak temperature of 260+0/-5°C

Samples of the many devices manufactured with these process technologies are continuously undergoing reliability evaluation as part of the ADI Reliability Monitor Program. Additional qualification data is available on Analog Devices' web site at: http://www.analog.com/world/quality/read/1stpage.html.

ESD Testing

The results of Human Body Model (HBM) and Field Induced Charge Device Model (FICDM) ESD testing are summarized in Table 7.

ADI measures ESD results using stringent test procedures based on the specifications listed in the above table. Any comparison with another supplier's results should ensure that the same ESD test procedures have been used. For further details, please see the EOS/ESD chapter of the ADI Reliability Handbook at http://www.analog.com/world/quality/manuals/.

Table 7. AD8675, ADA4004-4, ADR127, AD8677 ESD Test Results

ESD Model	Package	ESD Test Spec	RC Network	Generic	Highest Pass Level	First Fail Level	Class
FICDM	8-SOICnb	ESD Assoc. STM5.3.1-1999	1Ω, Cpkg	AD8677	1.5kv	-	c6
FICDM	8-SOICnb	ESD Assoc. STM5.3.1-1999	1Ω, Cpkg	AD8675	1.5kv	-	c6
FICDM	6-TSOT	ESD Assoc. STM5.3.1-1999	1Ω, Cpkg	ADR127	0.5kv	-	c4
FICDM	14-SOICnb	ESD Assoc. STM5.3.1-1999	1Ω, Cpkg	ADA4004	1.5kv	-	c6
HBM	6-TSOT	ESD Assoc. STM5.1-2001	1.5kΩ, 100pF	ADR127	0.8kv	-	1b
HBM	14-SOICnb	ESD Assoc. STM5.1-2001	1.5kΩ, 100pF	ADA4004	1.5kv	-	1c
HBM	8-SOICnb	ESD Assoc. STM5.1-2001	1.5kΩ, 100pF	AD8675	2.5kv	-	c2
HBM	8-SOICnb	ESD Assoc. STM5.1-2001	1.5kΩ, 100pF	AD8677	3.5kv	-	c2

Approvals

Reliability Engineer: Edward Mullen
This report has been approved by electronic means (3.5).

Additional Information

Data sheets and other additional information are available on Analog Devices' web site at the addresses shown below.

Home Page: http://www.analog.com
Sales Info: http://www.analog.com/world/corp_fin/sales_directory/distrib.html
Reliability Data: http://www.analog.com/world/quality/read/1stpage.html

Reliability Handbook: **http://www.analog.com/corporate/quality/manuals/**

Section B: Device Level Qualification Data

Purpose

The purpose of this document is to report the device level qualification of HVBP2 Process at ADLK. The qualification tests are determined by ADI0012, “Procedure for the Qualification of New or Revised Processes or Packages”. The devices used for this qualification were fabricated on the HVBP2, Double Poly, Double Metal, CMOS Process, at ADLK 8” Fab.

Scope

This document describes test methods and the conclusion of testing.

Sample Sizes

In general, data should come from three separate wafer fab lots. Specific sample sizes are documented with each individual test.

Use of Packages

DIP-18 Side Brazed Ceramic Package with Aluminium Wire Bond is used for all tests.

Reference Documents

ADI0012: Procedure for the Qualification of New or Revised Processes or Packages
ADI Reliability Handbook: http://www.analog.com/corporate/quality/manuals/

<table>
<tr><th colspan="5">Electromigration</th></tr>
<tr><td colspan="5">Electromigration should be done on each via level and metal layer with any differences in design rules or process parameters, including metal process and the inter/intra level dielectric. Worst case stacked via or each permutation of stacked vias should be tested separately. Via tests should exercise electron flow both up and down the via, thus stressing the via-to-metal interfaces.</td></tr>
<tr><td>Reference Documents</td><td colspan="4">JESD61, JESD87, JESD33A, JESD37, JESD63.</td></tr>
<tr><td rowspan="18">Test Structure</td><td colspan="4">Test structures designed as per JESD87</td></tr>
<tr><td>Pattern</td><td>w/t</td><td>Length</td><td>Comment</td></tr>
<tr><td>Metal 1</td><td>2um</td><td>1500um</td><td>Long flat</td></tr>
<tr><td>Metal 1</td><td>2um</td><td>1500um</td><td>Long topo</td></tr>
<tr><td>Metal 1</td><td>4um</td><td>900um</td><td>Long flat</td></tr>
<tr><td>Metal 1</td><td>4um</td><td>900um</td><td>Long topo</td></tr>
<tr><td>Metal 1</td><td>3um</td><td>800um</td><td>Long snake</td></tr>
<tr><td>Metal 1</td><td>10um</td><td>500um</td><td>Long topo</td></tr>
<tr><td>Metal 1</td><td>10um</td><td>500um</td><td>Long flat</td></tr>
<tr><td>Metal 2</td><td>2um</td><td>1500um</td><td>Long flat</td></tr>
<tr><td>Metal 2</td><td>2um</td><td>1500um</td><td>Long topo</td></tr>
<tr><td>Metal 2</td><td>4um</td><td>900um</td><td>Long flat</td></tr>
<tr><td>Metal 2</td><td>4um</td><td>900um</td><td>Long topo</td></tr>
<tr><td>Metal 2</td><td>3um</td><td>800um</td><td>Long flat</td></tr>
<tr><td>Metal 2</td><td>10um</td><td>500um</td><td>Long topo</td></tr>
<tr><td>Metal 2</td><td>10um</td><td>500um</td><td>Long flat</td></tr>
<tr><td colspan="3">Contact</td><td>Nsd Contact 2x2um</td></tr>
<tr><td colspan="3">Via 1</td><td>6 2x2um2 vias M1 wide</td></tr>
<tr><td></td><td colspan="3">Via 2</td><td>6 2x2um2 vias M2 wide</td></tr>
<tr><td>Vehicle</td><td colspan="4">Package (ceramic) level test</td></tr>
<tr><td>Method</td><td colspan="4">Constant Current stressing @225C</td></tr>
<tr><td>Sample Size</td><td colspan="4">10 - 16</td></tr>
<tr><td>Fail Criteria</td><td colspan="4">Percent Resistance change e.g. 20% or short circuit to extrusion monitor.
End of experiment determined by 100% of samples failed.</td></tr>
</table>

Model	Black's Model: $t_{50} = AJ^{-n}\exp(E_A/kT)$ Current density exponent, n=2. Activation energy, E_A=0.7.
Merit Number	Calculate $t_{0.1}$ at max current density and max operating junction temp: $t_{0.1} = t_{50}\exp[-3.09s]$ … s=sigma
	Calculate max current density (s=sigma): $J_{MAX}=J_{STRESS}\{[\ t_{50}\exp[-3.09s + (^1/T_{USE}-^1/T_{STRESS})^{E_A}/_k\ ]]/100{,}000\}^{1/n}$
Metal Scheme	Metal 1/2: 4KA AlCu / 1.65KA TiN

Table 1 Bamboo Data

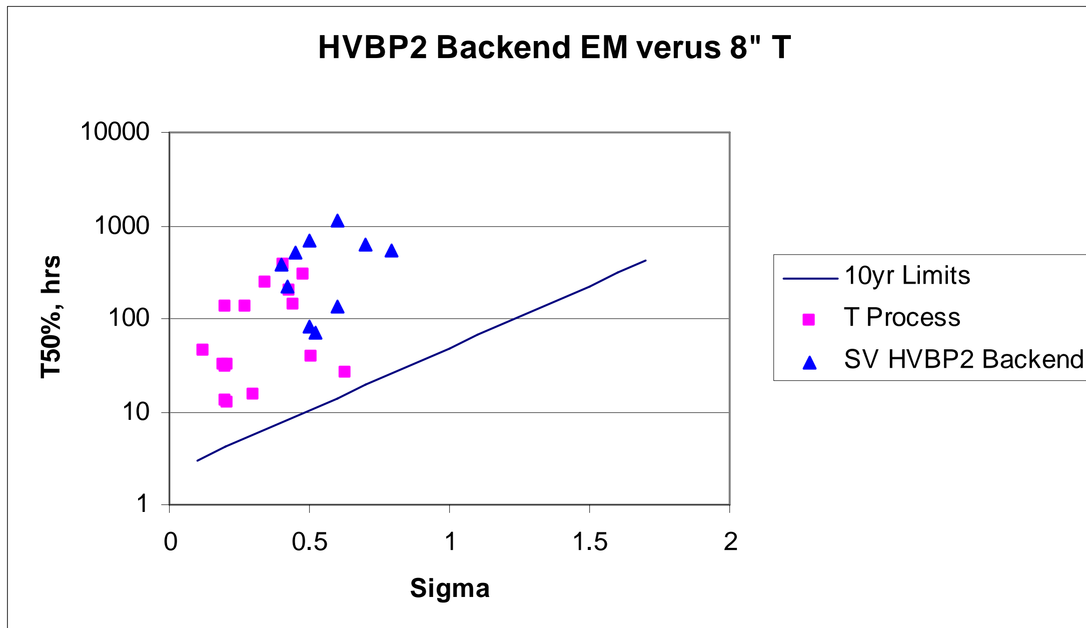
Wafer i.d.	**Structure**	**T50%,hrs(225deg C, 52mA/um²)**	**Sigma**

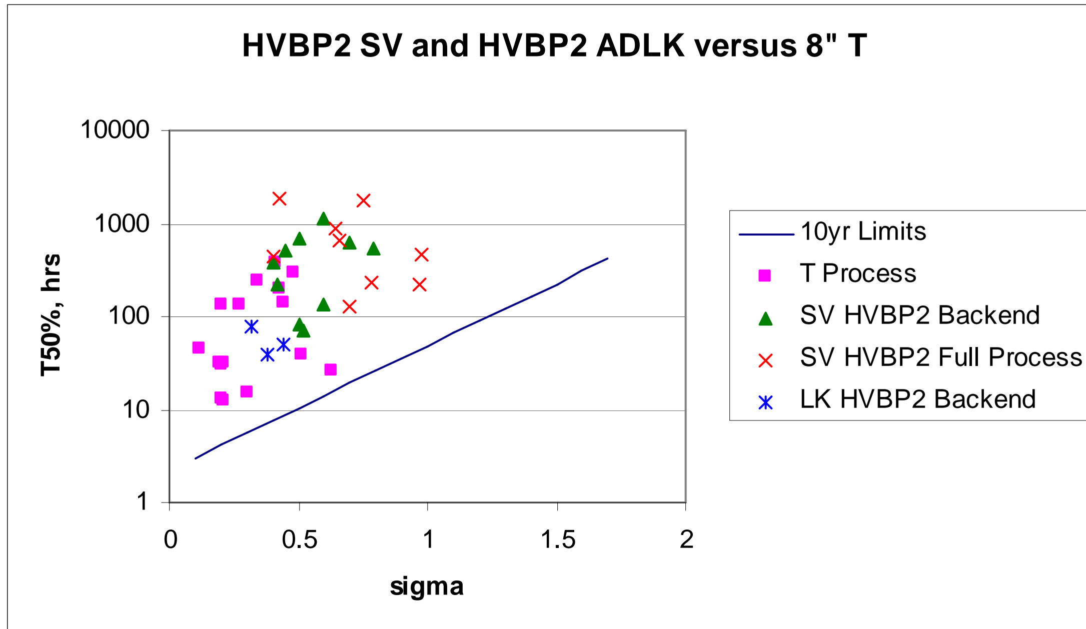
Table 2 Multigrain Data

Wafer i.d.	**Structure**	**T50%,hrs(225deg C, mA/um²)**	**Sigma**
D26764wf3	Metal 1 10*500um long topo	3.37	0.19
	Metal 1 10*500um long flat	4.8	0.23
	Metal 2 4*900um long topo	3.899	0.23
	Metal 2 4*900um long flat	4.83	0.36
D15964wf9	Metal 1 2*1500um long flat	16.72	0.18
	Metal 1 2*1500um long topo	8.23	0.22
	Metal 1 4*900um long flat	8.61	0.32
	Metal 1 4*900um long topo	5.74	0.23
	Metal 1 10*500um long topo	6.09	0.13
	Metal 2 2*1500um long flat	12.56	0.18
	Metal 2 2*1500um long topo	9.09	0.43
	Metal 2 4*900um long flat	5.32	0.32
	Metal 2 4*900um long topo	3.31	0.2
	Metal 2 10*500um long flat	3.81	0.22
	Metal 2 10*500um long topo	2.32	0.26
D17180wf3	Metal 1 10*500um long topo	1.636	0.24
	Metal 1 4*900um long flat	10.45	0.22
	Metal 2 2*1500um long topo	8.8	0.58
	Metal 2 2*1500um long flat	13.644	0.62

Table 3 Contact/Via Data

Wafer i.d.	Structure	T50%,hrs (225deg C, mA)	Sigma
D17180wf3	6 2x2um2 vias M2 wide	12.07	0.398
D15964wf9	Nsd Contact 2x2um	2.18	0.35
	6 2x2um2 vias M1 wide	91.05	0.13
	6 2x2um2 vias M2 wide	10.19	0.52
D26764wf3	6 2x2um2 vias M1 wide	139.112	0.22
	6 2x2um2 vias M2 wide	104.36	0.41





Conclusions

The EM data for the HVBP2 process satisfies reliability requirements for 10yr lifetimes at 70deg C for 0.1% of the population. It also matches well with both Sunny Vale data.

Hot Carrier Injection (HCI): Bipolar Device	
Hot Carrier Testing is performed on the minimum geometry device.	
Reference Documents	JESD28, JESD60
Test Structure	Single transistor device, with all terminals of the device contacted. W/L = 6x6um
Vehicle	Package (ceramic) level test
Method	Stress at room temperature, 25C. Stress method for NPN: Ic vs Hfe • Vbe 0 – 3V in 0.5V steps • Vce fixed at 10V A reverse emitter current of: 1e10^-7 mA, 3e10^-7 mA and 5e10^-7 mA Inspect conditions: Vce = 5V, Ib = .001mA Stress method of PNP: Ic vs Hfe • Vbe 0 – 3V in 0.5V steps • Vce fixed at 10V Inspect conditions: Vce = 5V, Ib = .001mA A reverse emitter current of: 7.9e10^-8 mA, 1.1e10^-7 mA and 2.5e10^-7 mA
Sample Size	24 DUTs
Fail Criteria	The failure point is determined to be where the gain has degraded by 10% from T0 value.

Model	For Bipolar HCI, the % degradation in Gain is plotted versus stress time for each device. The failure point is determined to be where the gain has degraded by 10% from T0 value. The lognormal distributions for each of the three reverse Ie stress currents is plotted and T0.1% hrs and Sigma is noted. The required lifetime is > 10yrs for 0.1% cumulative fail time. The T0.1% is plotted versus stress current and a power series fit is used to fit a trendline. The relevant power series equation is used to calculate the maximum operating current for ADBV required 10yrs lifetime. Iebo-vs-Vebo is measured on a number of time zero devices. This plot allows the maximum operating reverse current to maximum allowed operating reverse Vbe.

Lot Details	**Wafer #**	**Device**	**Reverse Ie (mA)**	**T0.1% [hrs]**	**Sigma**	**Max Reverse Ie (10yrs)**	**Max Reverse Vbe (10yrs)**
D15964.1	12	NPN	1e10^-7 3e10^-7 5e10^-7	NA	NA	NA	Pass
D15964.1	12	PNP	7.9e10^-8 1.1e10^-7 2.5e10^-7	NA	NA	NA	Pass

CONCLUSIONS:

The conclusion is that after >100 hours stress there was < 1% degradation In Hfe (Ic/Ib). The data indicates that Hot-carriers is not a concern for Bipolar devices on HVBP2.

Time Dependent Dielectric Breakdown		
TDDB test is used to model the intrinsic behavior in the technology being qualified using both temperature and voltage acceleration. Time to failure scales inversely with voltage, temperature and area of the oxides in test.		
Reference Documents	EIAJ-988	
Test Structure	Ply 1 – Nitride – Ply 2 Capacitor	
	Tox	Details
	900 Ang.	The strucutures have Cap Area 1 = 76x40 um, Area 2 = 966x40 um, Area 3 = 3616x40um. (See Graph 4 for Area Dependency)
Vehicle	Package (ceramic) level test	
Method	Constant voltage stress at various stress voltages ($V_G > V_{DDMAX}$) at a temperature of 225C Ply1-Nitride-Ply2 capacitors stress = +/-65V stress	
Sample Size	16	
Fail Criteria	Stress until 100% of the samples have failed. For thick oxides, increase in current to >0.0001A is a typical fail criteria.	
Model	E Model: $TFu = \exp E_A/K(1/Tt-1/Tu)*\exp G(Vt-Vu)*TFt$ E-Field Activation Energy, Gamma or G. (See Table 2 & Graph 2) Temperature Activation Energy, E_A. (See Table 2 & Graph 3)	
Merit Number	Calculate lifetime at use conditions: T50test = exp(3.08*sigma) * 10yrs/AT*AE AT & AE are the temperature and voltage acceleration factors from test to use conditions. The T50% control lines in graphs 1 to 5 below are the minimum time for 50% of the test samples to fail and the corresponding sigma value required to ensure <0.1% cumulative failures in 10 yrs at 70C from the TDDB test conditions. (See Graph 1 for results)	

Tables 1 and 2 summaries the qualification lots and the characterization matrix for the HVBP2 process qualification. Table 3 shows the calculated activation energies for both voltage and temperature.

Table 1: Lot Allocation

Lots used during qualification
G31663.1
D12702.1
D12942.1

Table 2: Characterisation matrix

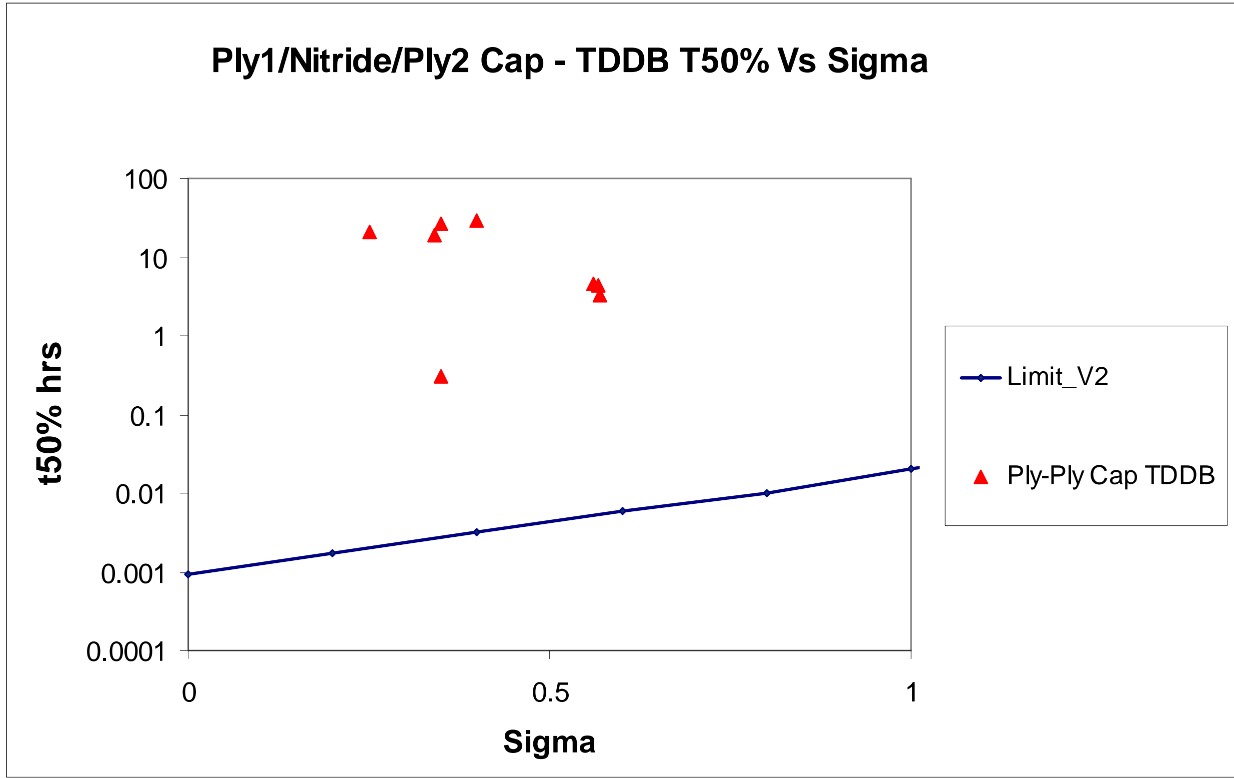
	Voltages for 30V Ply Cap	+/-65V	+/-70V	+/-75V	+/-80V
Temperature					
175C		x	x	x	x
200C		x	x	x	x
225C		x	x	x	x

Table 3: Activation Energies

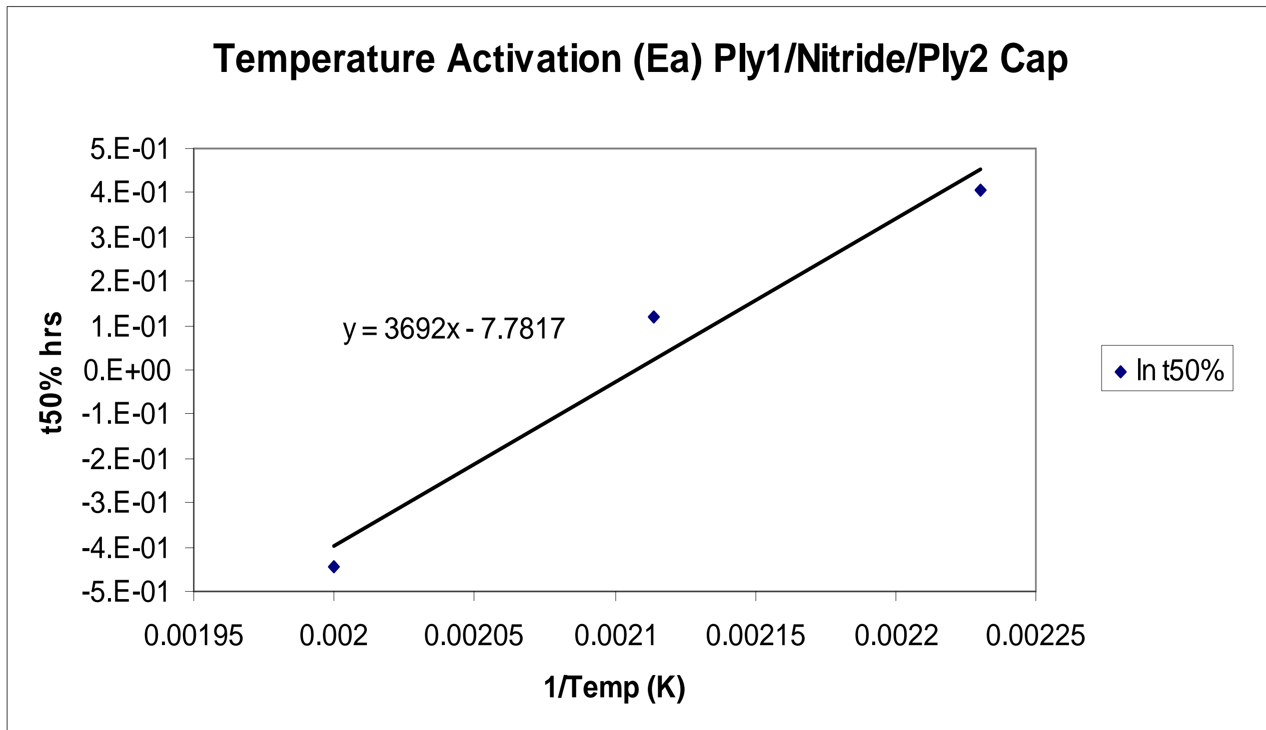
Activation Energies		
Devices	**Gamma**	**Ea**
Ply1-Nitride-Ply2 Cap	3.5	0.32

Graphical representation of results.

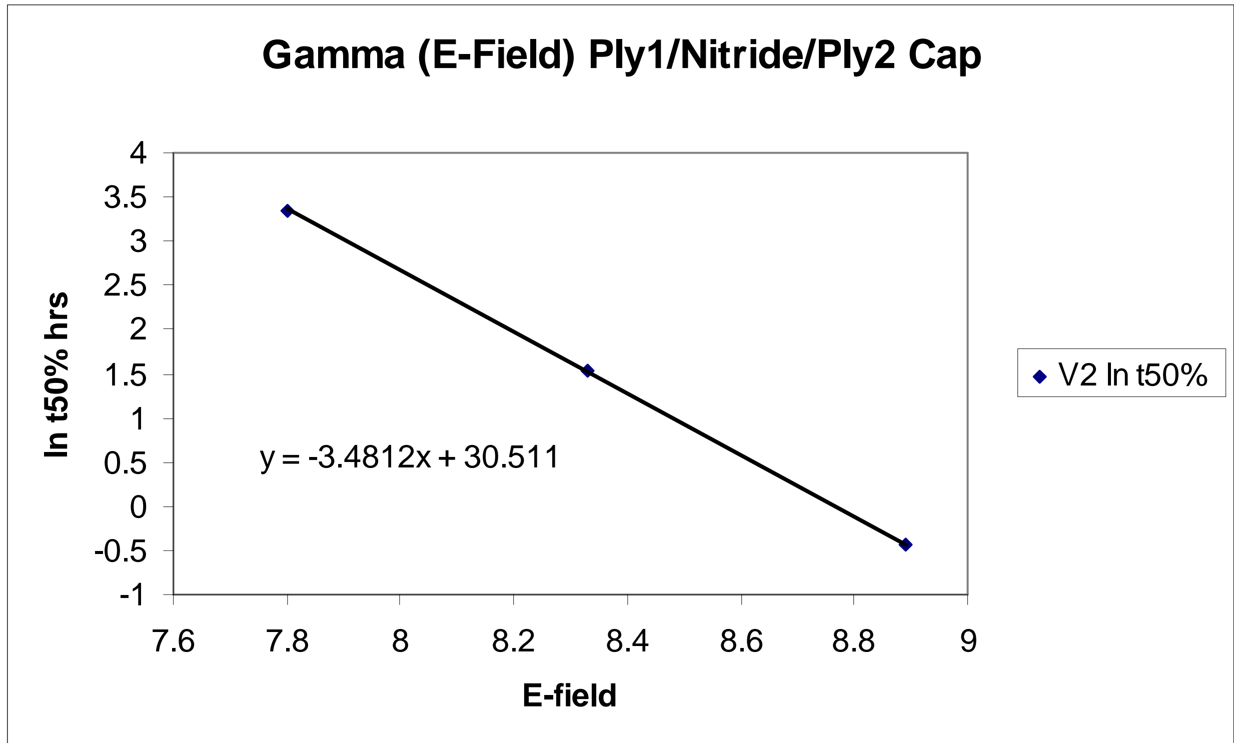
Graph 1: Ply-Nitride-Ply Capacitor 900A Oxide



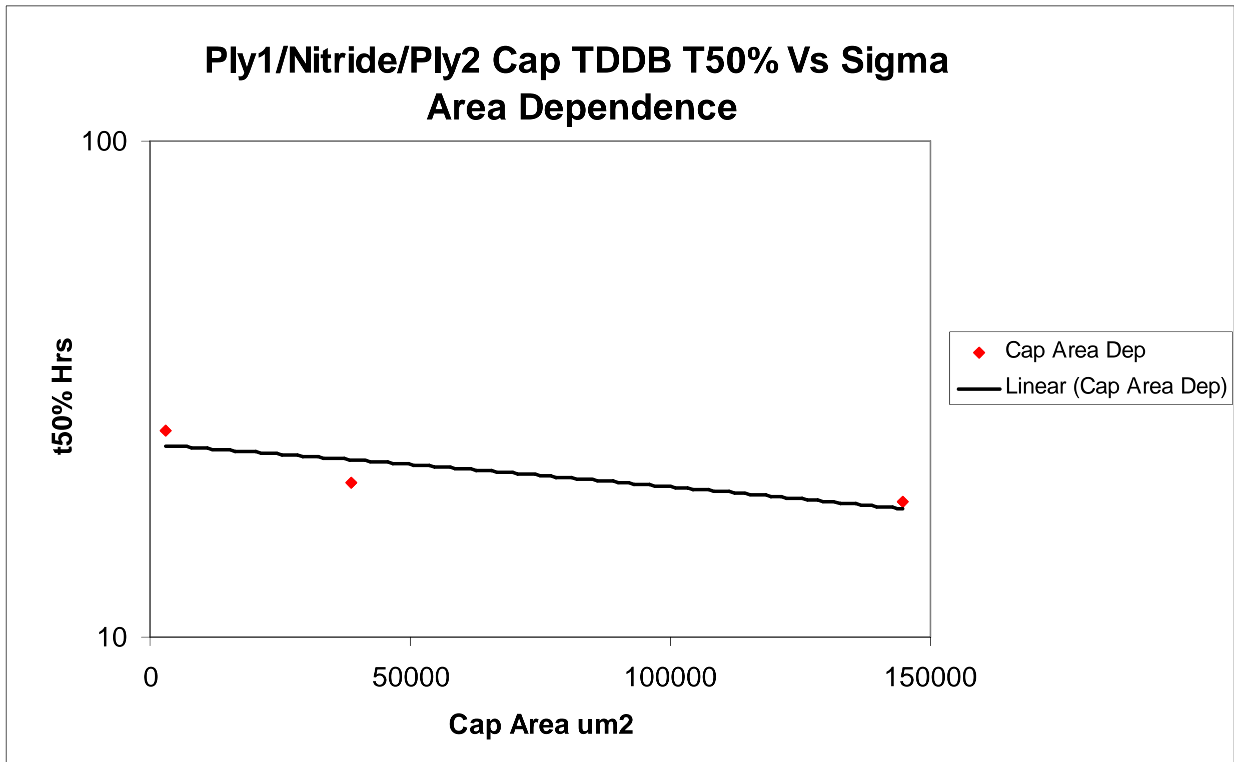
Graph 2: Thermal Activation Energy (Ea)



Graph 3: E-Field Acceleration Factor (Gamma)



Graph 4: Ply-Nitride-Ply Capacitor: Area Dependency



TDDB Summary

The TDDB data for the HVBP2 process satisfies reliability requirements for 10yr lifetimes at 70deg C for 0.1% of the population.

Conclusion

The device level qualification of the ADLK 8" HVBP2 Process has successfully completed for production release.

Approvals

Reliability Engineer: Edward Mullen
This report has been approved by electronic means (3.5).

Additional Information

Data sheets and other additional information are available on Analog Devices' web site at the addresses shown below.

Home Page: http://www.analog.com
Sales Info: http://www.analog.com/world/corp_fin/sales_directory/distrib.html
Reliability Data: http://www.analog.com/world/quality/read/1stpage.html
Reliability Handbook: http://www.analog.com/corporate/quality/manuals/