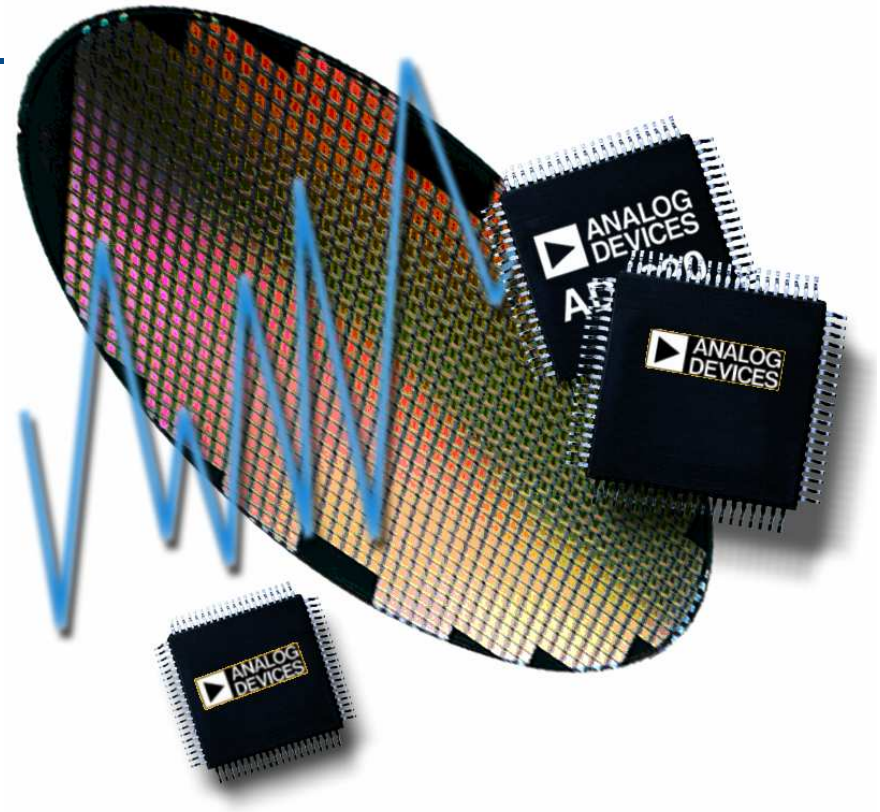

Reliability Report

Report Title: ADT7461 Transfer to TSMC Fab09

Report Number: 6130

Date: 1 November 2006

Analog Devices Reliability . Raheen Industrial Park . Limerick, Ireland
Tel: 353.61.229011 Fax: 353.61.303891 www.analog.com

Summary

This report documents the successful completion of the reliability qualification requirements for release and of the ADT7461 Family Transfer to TSMC Fab09. The ADT7461 is packaged in a 8-SOICnb package.

The ADT7461 is an enhanced digital temperature sensor. The temp sensor can monitor a wide temperature range, and automatically cancels temperature errors due to resistance in series with the remote sensor.

Table 1. Product Characteristics

Part Number	ADT7461
Device / Die Rev	P461
Die Size (mm)	1.31 x 1.74
Wafer Fabrication Site	TSMC Fab - 09
Wafer Fabrication Process	0.5um DPTM CMOS
Passivation Layer	undoped-oxide/SiN
Bond Pad Metal Composition	AlCu
Available Package(s)	8-SOICnb
Body Size (mm)	4.00 x 5.00 x 1.50
Assembly Location	Amkor-P
Die Attach	Ablestik 8340
Lead Frame Material	Copper
Bond Wire Type	Gold
Bond Wire Dia. (mils)	1.00
Mold Compound	Sumitomo 6730
Lead Frame Finish	Tin Plate
Moisture Sensitivity Level	1
Maximum Peak Reflow	260C +0/-5C

Description/Results of Tests Performed

Table 2 provides a description of the qualification tests conducted and the associated test results on the ADT7461 and other products manufactured on the same technologies as described in the product characteristics table.

Table 2. 8-SOICnb Qualification Test Results

Test Name	Conditions	Specification	Device	Lot Num	Sample Size	Qty. Rejects
Autoclave [1]	121C 100%RH 2atm 168hrs	JEDEC-STD-22, Method A102	AD5543	3279	77	0

Autoclave [2]	121C 100%RH 2atm 168hrs	JEDEC-STD-22, Method A102	AD8210	Q4960.4	77	0
				Q4960.5	77	0
				Q4960.6	77	0
Autoclave [3]	121C 100%RH 2atm 168hrs	JEDEC-STD-22, Method A102	AD8675	G25146.1	45	0
				G26148.1	45	0
				G27193.1	45	0
Autoclave [2]	121C 100%RH 2atm 168hrs	JEDEC-STD-22, Method A102	AD8675	G27196.8W#14	45	0
				G27466.1W#13	45	0
				G28425.1w#12	45	0
			ADR127	G26154	45	0
				G28430	45	0
				G28431	45	0
HTS	150C 1000hrs	JEDEC-STD-22, Method A103	AD5543	3279	77	0
			AD8210	Q4960.13	77	0
			AD8675	G21845.1	77	0
			ADR127	G26154	77	0
				G28430	77	0
				G28431	77	0
	150C 240hrs	JEDEC-STD-22, Method A103	AD8675	G25146.1	77	0
SHR [1]	See Below	ADI-0049	AD5543	3279	20	0
SHR [2]	See Below	ADI-0049	AD8210	Q4960.14	10	0
Temp Cycle [2]	-65C/+150C 1000cycles	JEDEC-STD-22, Method A104	AD8210	Q4960.10	77	0
				Q4960.11	77	0
				Q4960.12	77	0
Temp Cycle [1]	-65C/+150C 500cycles	JEDEC-STD-22, Method A104	AD5543	3279	45	0
					77	0
Temp Cycle [3]	-65C/+150C 500cycles	JEDEC-STD-22, Method A104	AD8675	G25146.1	0	0
				G26148.1	0	0
				G27193.1	0	0
				G27196.8W#14	77	0
				G27466.1W#13	77	0
				G28425.1W#12	77	0
Thermal Shock	-65C/+150C 500cycles	JEDEC-STD-22, Method A106	AD5543	3279	77	0
Thermal Shock [2]	-65C/+150C 500cycles	JEDEC-STD-22, Method A106	ADR127	G26154	77	0
				G28430	77	0
				G28431	77	0

[1] These Samples were subjected to preconditioning (per J-STD-020 Level 1) prior to the start of the stress test. Level 1 preconditioning consists of the following:
Bake: 24 hrs @ 125C
Unbiased Soak: 168 hrs @ 85C, 85%RH
Reflow: 3 passes through an oven with a peak temperature of 240+0/-5C for a minimum of 10 seconds.

[2] These Samples were subjected to preconditioning (per J-STD-020 Level 1) prior to the start of the stress test. Level 1 preconditioning consists of the following:
Bake: 24 hrs @ 125C
Unbiased Soak: 168 hrs @ 85C, 85%RH
Reflow: 3 passes through an oven with a peak temperature of 260+0/-5C for a minimum of 10 seconds.

[3] These Samples were subjected to preconditioning (per J-STD-020 Level 1) prior to the start of the stress test. Level 1 preconditioning consists of the following:
Bake: 24 hrs @ 125C
Unbiased Soak: 168 hrs @ 85C, 85%RH
Reflow: 3 passes through an oven with a peak temperature of 255+0/-5C for a minimum of 10 seconds.

Samples of the many devices manufactured with these packaging technologies are continuously undergoing reliability evaluation as part of the ADI Reliability Monitor Program. This additional qualification data, as well as FIT data, is available on Analog Devices' web site at: http://www.analog.com/corporate/quality/read/1stpage.html.

Table 3. Process Qualification Test Results

Test Name	Conditions	Specification	Part Number	Fab Process	Lot Number	Sample Size	Qty. Rejects
HAST [1]	130C 85%RH 2atm, Biased 96hrs	JEDEC-STD-22, Method A110	AD7685	0.5um DPTM CMOS	Q4883.14	79	0
				0.5um DPTM CMOS	Q4883.5	82	0
					Q4883.6	80	0
					Q4883.7	82	0
					Q5827.4	77	0
					Q5827.5	76	0
					Q5827.6	77	0
HTOL	125C<Tj<135C, Biased 1000hrs	JESD22-A108	AD8652	0.5um DPTM CMOS	475973.1	50	0
					475974.1	50	0
					475977.1	50	0
					475978.1	50	0
					475979.1	50	0
			ADP3190	0.5um DPTM CMOS	V62033.1	45	0
					V62044.12	45	0
					V62044.2	45	0
HTOL	150C<Tj<175C, Biased 500hrs	JESD22-A108	ADM1032	0.5um DPTM CMOS	F137216.9	45	0
HTOL	150C<Tj<175C, Biased 500hrs	JESD22-A108	ADM1032	0.5um DPTM CMOS	F137214.7	45	0
HTOL	150C<Tj<175C, Biased 500hrs	JESD22-A108	ADM1032	0.5um DPTM CMOS	F137219.7	45	0
HTOL	150C<Tj<175C, Biased 500hrs	JESD22-A108	ADM1032	0.5um DPTM CMOS	F137220.8	45	0
Temp Cycle [1]	-65C/+150C 500cycles	JEDEC-STD-22, Method A104	ADM1032	0.5um DPTM CMOS	F149882.7	77	0
Temp Cycle [1]	-65C/+150C 500cycles	JEDEC-STD-22, Method A104	ADM1032	0.5um DPTM CMOS	F149606.12	77	0
Temp Cycle [1]	-65C/+150C 500cycles	JEDEC-STD-22, Method A104	ADM1032	0.5um DPTM CMOS	F148970.8	77	0

ELF	125C, 48hrs	MIL-STD-883	ADM1032	0.5um DPTM CMOS	O38084.2	400	0
ELF	125C, 48hrs	MIL-STD-883	ADM1032	0.5um DPTM CMOS	O38084.3	200	0
ELF	125C, 48hrs	MIL-STD-883	ADM1032	0.5um DPTM CMOS	O38084.1	200	0
ELF	125C, 48hrs	MIL-STD-883	ADM1032	0.5um DPTM CMOS	O99006.4	202	0
ELF	125C, 48hrs	MIL-STD-883	ADM1032	0.5um DPTM CMOS	O99006.3	202	0
ELF	125C, 48hrs	MIL-STD-883	ADM1032	0.5um DPTM CMOS	O99006.2	202	0
Autoclave [1]	121C 100%RH 2atm 168hrs	JEDEC-STD-22, Method A102	ADM1032	0.5um DPTM CMOS	F148970.11	77	0
Autoclave [1]	121C 100%RH 2atm 168hrs	JEDEC-STD-22, Method A102	ADM1032	0.5um DPTM CMOS	F149882.9	77	0
Autoclave [1]	121C 100%RH 2atm 168hrs	JEDEC-STD-22, Method A102	ADM1032	0.5um DPTM CMOS	F149606.14	77	0
Autoclave [1]	121C 100%RH 2atm 168hrs	JEDEC-STD-22, Method A102	ADM1032	0.5um DPTM CMOS	L89799.1	45	0
Autoclave [1]	121C 100%RH 2atm 168hrs	JEDEC-STD-22, Method A102	ADM1032	0.5um DPTM CMOS	L20713.1	45	0
Autoclave [1]	121C 100%RH 2atm 168hrs	JEDEC-STD-22, Method A102	AD1958	0.5um DPTM CMOS	V23533.4	77	0

[1] These Samples were subjected to preconditioning (per J-STD-020 Level 1) prior to the start of the stress test.
Level 1 preconditioning consists of the following:
Bake: 24 hrs @ 125C
Unbiased Soak: 168 hrs @ 85C, 85%RH
Reflow: 3 passes through an oven with a peak temperature of 260+0/-5C for a minimum of 10 seconds.

Samples of the many devices manufactured with these packaging technologies are continuously undergoing reliability evaluation as part of the ADI Reliability Monitor Program. This additional qualification data, as well as FIT data, is available on Analog Devices' web site at: http://www.analog.com/corporate/quality/read/1stpage.html

ESD Testing

The results of Human Body Model (HBM) and Field Induced Charge Device Model (FICDM) ESD testing are summarized in Table 2.

ADI measures ESD results using stringent test procedures based on the specifications listed in the above table. Any comparison with another supplier's results should ensure that the same ESD test procedures have been used. For further details, please see the EOS/ESD chapter of the ADI Reliability Handbook at http://www.analog.com/corporate/quality/manuals/.

Table 2. ADT7461 ESD Test Results

ESD Model	Package	ESD Test Spec	RC Network	Highest Pass Level	First Fail Level	Class
FICDM	8-SOICnb	ESD Assoc. STM5.3.1-1999	1ohm, Cpkg	1.5kv	2kv	C6
HBM	8-SOICnb	ESD Assoc. STM5.1-2001	1.5kohm, 100pF	3kv	3.5kv	2

Latch-Up and Electrical Overstress Testing Results

The ADT7461 was tested for latch-up conditions using the test method outlined in JEDEC Standard Number 78. The result summary is shown below:

No latch-up occurred during testing of each individual input and output pin in which both positive and negative current pulses (50us risetime, 5ms duration) were applied up to 100mA. This input and output latch-up testing was conducted initially with all input pins at Vin minimum levels, and subsequently with all input pins at Vin maximum levels.

No latch-up occurred during testing of the supply pin groups in which voltage pulses (50us risetime, 5ms duration) were applied up to VDDmax. This overvoltage latch-up testing was conducted initially with all input pins at Vin minimum levels, and subsequently with all input pins at Vin maximum levels.

The six devices that were subjected to the latch-up test criteria all passed post-latch-up electrical testing.

Approvals

Reliability Engineer: Edward Mullen
This report has been approved by electronic means (2.0).

Additional Information

Data sheets and other additional information are available on Analog Devices' web site at the addresses shown below.

Home Page:	http://www.analog.com
Sales Info:	http://www.analog.com/world/corp_fin/sales_directory/distrib.html
Reliability Data:	http://www.analog.com/corporate/quality/read/1stpage.html
Reliability Handbook:	http://www.analog.com/corporate/quality/manuals/