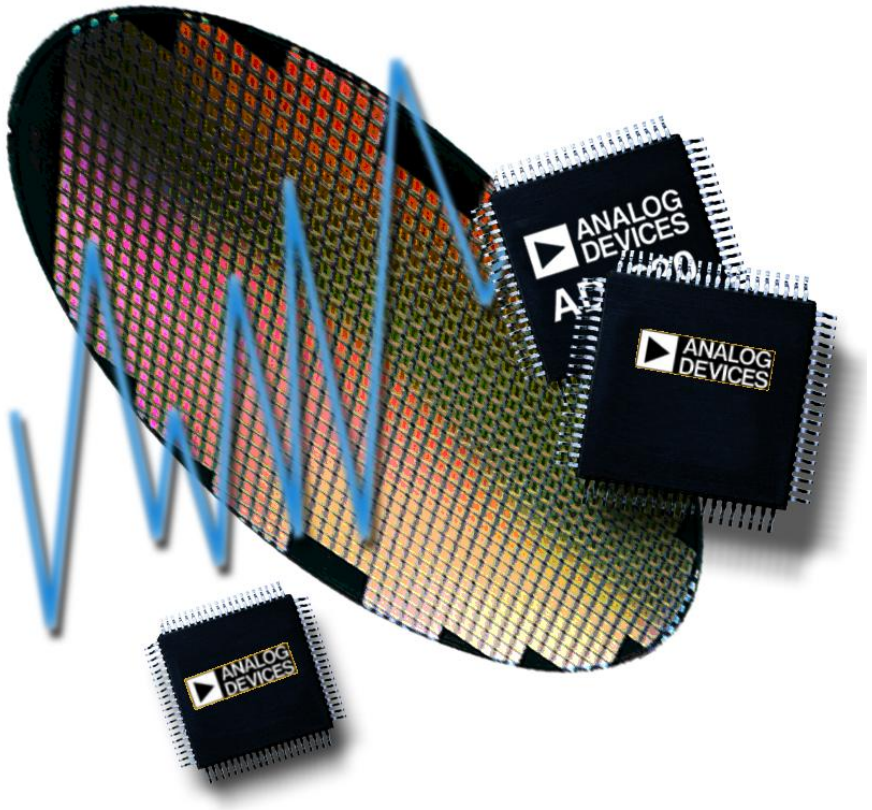

Reliability Report

Report Title: REF01, REF02, and REF03 Product Revision

Report Number: 7271

Revision: A

Date: 17 November 2008

Summary

This report documents the successful completion of the reliability qualification requirements for release of the REF01, REF02, and REF03 product in an 8-CERDIP, 8-PDIP, 8-SOICnb and 8-TO99 package. The REF01, REF02, and REF03 are precision 10.0 V, 5.0 V, and 2.5V band gap voltage references with minimal change for variations in supply voltage, ambient temperature, or loading conditions.

The REF02 was used as the qualification vehicle for the REF0x family. The product revision was due to design improvement to ensure proper start up sequence over all process variance at operating temperature below 0°C.

Table 1: REF01/2/3 Product Characteristics

Device

Die ID	1716Ya
Die Size (mm)	0.8 x 0.85
Wafer Fabrication Site	ADI-Wilmington
Wafer Fabrication Process	2um HVBP1 DM
Transistor Count	32
Passivation Layer	doped-oxide/SiN
Bond Pad Metal Composition	AlCu
Maximum Power Dissipation (W)	0.040

Package/Assembly

Available Package(s)	8-CERDIP	8-PDIP	8-SOICnb	8-TO99
Body Size (mm)	7.87 x 10.29 x 1.00	1.60 x 2.90 x 0.87	4.00 x 5.00 x 1.50	7.45 x 4.19 x 1.25
Assembly Location	ADPI	Carsem-S	Amkor-P	ADPI
Die Attach	SFG (QMI2419MA)	Ablestik 84-1LMIS R4	Ablestik 84-1LMIS R4	JM-7000
Lead Frame Material	Alloy 42	Copper	Copper	Kovar
Bond Wire Type	Aluminum	Gold Tanaka M3	Gold	Aluminum
Bond Wire Dia. (mils)	1.25	1.30	1.00	1.25
Mold Compound	NA	Sumitomo G600C	Sumitomo 6600H	NA
Lead Finish	Tin/Lead Solder Plate	Tin Plate	Tin Plate	Sn63/Pb37
Die Coat	NA	Polyimide	Polyimide	NA
Moisture Sensitivity Level	1			
Maximum Peak Reflow (°C)	240	260	260	240

Description/Results of Tests Performed

Tables 2, 3, 4, 5 and 6 provide a description of the qualification tests conducted and the associated test results for the REF02. All devices were electrically tested before and after each stress. Any device that did not meet all electrical data sheet limits following stressing would be considered a valid (stress-attributable) failure unless there was conclusive evidence to indicate otherwise.

Table 2: SOICnb Package Qualification Test Results

Test Name	Specification	Conditions	Device	Lot Num	Sample Size	Qty. Rejects
Autoclave (AC) [1]	JEDEC-STD-22, Method A102	121C 100%RH 2atm 96hrs	ADR02	Q6969.2	77	0
				Q6969.12	77	0
				Q6969.13	77	0
		121C 100%RH 2atm 168hrs	AD8202	Q5481.1	77	0
				Q5481.9	77	0
				Q5481.8	77	0
			AD8671	R61632.1	77	0
				R69851.1	77	0
				R69850.1	77	0
Solder Heat Resistance (SHR) [1]	ADI-0049	See Below	REF02	Q6969.10	30	0
Temperature Cycle (TC)[1]	JEDEC-STD-22, Method A104	-65C/+150C 500cycles	AD8202	Q5481.4	77	0
				Q5481.16	77	0
				Q5481.17	77	0
			ADR02	Q6969.11	77	0
				Q6969.18	77	0
				Q6969.19	77	0
			AD621	O91670.1	45	0

[1] These Samples were subjected to preconditioning (per J-STD-020 Level 1) prior to the start of the stress test. Level 1 preconditioning consists of the following:

- Bake: 24 hrs @ 125°C
- Unbiased Soak: 168 hrs @ 85°C, 85%RH
- Reflow: 3 passes through an oven with a peak temperature of 260°C

Table 3: CERDIP Package Qualification Test Results

Test Name	Specification	Conditions	Device	Lot Num	Sample Size	Qty. Rejects
Autoclave (AC)	JEDEC-STD-22, Method A102	121C 100%RH 2atm 168hrs	AD684	R4125.5	20	0
			AD734	R4041.4	22	0
High Temperature Storage Life (HTSL)	JEDEC-STD-22, Method A103	150C, 1000hrs	DAC08	E47236.1	16	0
Solderability	MIL-STD-883, Method 2003	Soldering temperature of 245C	OP77	E54663.7	5	0
				E39044.7	5	0
				E29051.8	5	0
				D26808.6	5	0
			ADG201	R38194.3	5	0
Temperature Cycle (TC)	JEDEC-STD-22, Method A104	-65C/+150C 500cycles	OP77	E65097.1	45	0
				D46974.4	45	0
			AD846	pb28259.9	15	0
			AD713	E81895.1	45	0
			ADG201	R86295.1	45	0
			DAC08	E47237.1	77	0

Table 4: PDIP Qualification Test Results

Test Name	Specification	Conditions	Device	Lot Num	Sample Size	Qty. Rejects
Autoclave (AC)	JEDEC-STD-22, Method A102	121C 100%RH 2atm 96hrs	AD80001	AB19566.1	77	0
				AB19567.1	77	0
				AB19568.1	77	0
			OP11	E110557.1	77	0
				E110558.1	77	0
				E110556.1	77	0
			AD845	AB19563.1	77	0
				AB19564.1	77	0
				AB19561.1	77	0
High Temperature Storage Life (HTSL)	JEDEC-STD-22, Method A103	150C, 1000hrs	OP11	E111739.1	77	0
				E111737.1	77	0
				E111738.1	77	0
			AD845	AB19598.1	77	0
Temperature Cycle (TC)	JEDEC-STD-22, Method A104	-65C/+150C 500cycles	AD8001	AB30764.1	77	0
				AB30762.1	77	0
				AB30763.1	77	0
			AD823	AB76223.1	77	0
				AB76222.1	77	0
				AB76221.1	77	0
			AD845	AB27861.1	77	0
				AB27858.1	77	0
				AB27859.1	77	0

Table 5: TO99 Qualification Test Results

Test Name	Specification	Conditions	Device	Lot Num	Sample Size	Qty. Rejects
Solderability	MIL-STD-883, Method 2003	Soldering temperature of 245C	REF02	E69116.8	5	0
				E51203.6	5	0
Temperature Cycle (TC)	JEDEC-STD-22, Method A104	-65C/+150C 500cycles	REF02	E72744.1	45	0
				E60128.1	45	0

Table 6: Process Qualification Test Results

Test Name	Conditions	Specification	Part Number	Lot Number	Sample Size	Qty. Rejects
Early Life Failure Rate (ELFR)	125C 48hrs	MIL-STD-883, Method 1015	AD8512	AA20923.1	800	0
				AA20924.1	800	0
				AA20925.1	800	0
Highly Accelerated Stress Test (HAST)[1]	130C 85%RH 2atm, Biased 96hrs	JEDEC-STD-22, Method A110	AD8512	R70109.1	77	0
				R70110.1	77	0
				R70111.1	77	0
			AD8671	R61633.1	77	0
				R69852.1	77	0
				R69853.1	77	0
			ADR02	Q6969.6	77	0
				Q6969.14	77	0
				Q6969.15	77	0
High Temperature Operational Life (HTOL)	150C<Tj<175C, Biased 500hrs	JESD22-A108	AD8512	AA19526.1	77	0
				AA19527.1	77	0
				AA19528.1	77	0
			ADR02	Q6969.7	77	0
				Q6969.16	77	0
				Q6969.17	77	0
			AD8671	R85521.1	77	0
				R85522.1	77	0
				R85523.1	77	0

[1] These Samples were subjected to preconditioning (per J-STD-020 Level 1) prior to the start of the stress test. Level 1 preconditioning consists of the following:

- Bake: 24 hrs @ 125°C
- Unbiased Soak: 168 hrs @ 85°C, 85%RH
- Reflow: 3 passes through an oven with a peak temperature of 260°C

Samples of the many devices manufactured with these process technologies are continuously undergoing reliability evaluation as part of the ADI Reliability Monitor Program. Additional qualification data is available on Analog Devices' web site at: http://www.analog.com/world/quality/read/1stpage.html.

ESD Testing

The results of Human Body Model (HBM) and Field Induced Charge Device Model (FICDM) ESD testing are summarized in Table 7.

Table 7: REF02 ESD Test Results

ESD Model	Package	ESD Test Spec	RC Network	Highest Pass Level	First Fail Level	Class
FICDM	8-CERDIP	ESD Assoc. STM5.3.1-1999	1Ω, Cpkg	1500V	NA	C6
FICDM	8-PDIP	ESD Assoc. STM5.3.1-1999	1Ω, Cpkg	1500V	NA	C6
FICDM	8-SOICnb	ESD Assoc. STM5.3.1-1999	1Ω, Cpkg	1500V	NA	C6
FICDM	8-TO99	ESD Assoc. STM5.3.1-1999	1Ω, Cpkg	1500V	NA	C6
HBM	8-SOICnb	ESD Assoc. STM5.1-2007	1.5kΩ, 100pF	4000V	NA	3A

ADI measures ESD results using stringent test procedures based on the specifications listed in the above table. Any comparison with another supplier's results should ensure that the same ESD test procedures have been used. For further details, please see the EOS/ESD chapter of the ADI Reliability Handbook at http://www.analog.com/en/corporate/quality-and-reliability/reliability-handbook/content/index.html.

Latch-up Testing

Six samples of the REF02 were submitted for latch-up testing at Ta=25°C per JEDEC Standard JESD78, Class I. Summary of results are shown in the table below.

Table 8: REF02 Latch-up Test Results

Tested Pins	Positive trigger Polarity (mA)	Negative trigger Polarity (mA)	V_{supply} Over voltage (V)	Level
Output	+100	-70	NA	B
Input	+100	-100	NA	A
Power	NA	NA	54	NA

*Results taken from report#7177

Approvals

Reliability Engineer: Robert Yhap

Additional Information

Data sheets and other additional information are available on Analog Devices' web site at the addresses shown below.

Home Page: http://www.analog.com
Customer Service: http://www.analog.com/en/content/contact_customer_service/fca.html
Reliability Handbook: http://www.analog.com/corporate/quality/manuals/