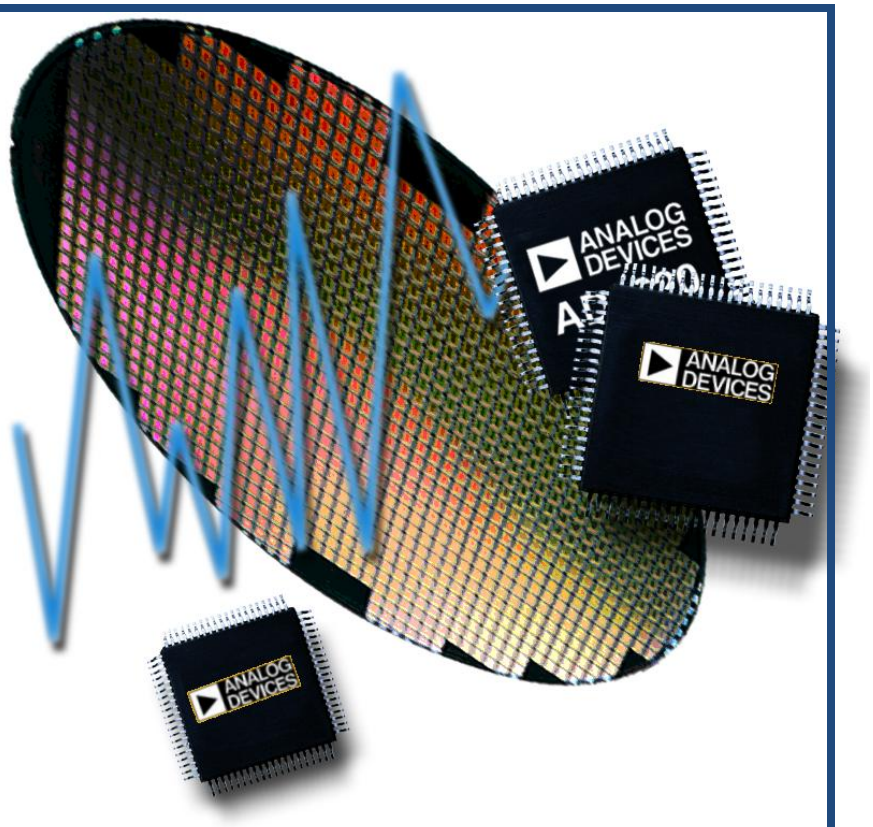

Reliability Report

Report Title: AD8628 Die Revision (X) Automotive Qualification

Report Number: 8202

Revision: A

Date: 18 January 2010

Summary

This report documents the successful completion of the reliability automotive qualification requirements for release of the AD8628 product in a 5-SOT_23, a 5-TSOT, and an 8-SOIC_N package. The AD8628 is a zero-drift, single-supply, rail-to-rail input/output operational amplifier.

Table 1: AD8628 Product Characteristics

Die/Fab

Die ID	6438x
Die Size (mm)	0.78 x 1.30
Wafer Fabrication Site	TSMC Fab 9
Wafer Fabrication Process	0.6um CMOS
Transistor Count	Eight hundred
Passivation Layer	undoped-oxide/SiN
Bond Pad Metal Composition	AlSiCu

Package/Assembly

Available Package	5-SOT_23	8-SOIC_N	5-TSOT
Body Size (mm)	2.90 x 1.60 x 1.15	5.00 x 4.00 x 1.75	2.90 x 1.60 x 0.90
Operating Temperature Range	-40°C ≤ TA ≤ +125°C	-40°C ≤ TA ≤ +125°C	-40°C ≤ TA ≤ +125°C
Assembly Location	Carsem-M	Amkor-P	Carsem-M
Molding Compound	NITTO MP 8000C	Sumitomo 6600H	NITTO MP 8000CSM
Wire Type	Gold Tanaka FA	Gold	Gold Tanaka GLD
Wire Diameter (mils)	1.00	1.00	0.80
Die Attach	Ablestik 84-1LMIS R4	Ablestik 84-1LMIS R4	Ablestik 84-1LMIS R4
Lead Frame Material	Copper	Copper	Copper
Lead Finish	Tin Plate	Tin Plate	Tin Plate
Moisture Sensitivity Level	1	1	1
Maximum Peak Reflow Temperature (°C)	260	260	260

Description / Results of Tests Performed

Tables 2 and 3 provide a description of the qualification tests conducted and the associated test results for products manufactured on the same technologies as described in Table 1. All devices were electrically tested before and after each stress. Any device that did not meet all electrical data sheet limits following stressing would be considered a valid (stress-attributable) failure unless there was conclusive evidence to indicate otherwise.

Table 2: Package Qualification Test Results

Test Name	Specification	Conditions	Device	Package	Lot #	Sample Size	Qty. Failures
Autoclave (AC)[1,3]	JESD22-A102	121°C 100%RH 2atm 168 hours	AD8512	Amkor-P 8-SOIC_N	R70106.1	77	0
					R70107.1	77	0
					R70108.1	77	0
		121°C 100%RH 2atm 96 hours	ADR02	Amkor-P 8-SOIC_N	Q6969.12	77	0
					Q6969.13	77	0
					Q6969.2	77	0
			AD8630	Amkor-P 14-SOIC_N	Q7954.5	77	0
					Q7954.6	77	0
					Q7954.7	77	0
			AD8601	Carsem-M 5-SOT_23	Q6729.2	77	0
					Q6729.3	77	0
					Q6729.4	77	0
			AD8628	Carsem-M 5-SOT_23	Q8202.7	77	0
				Carsem-M 5-TSOT	Q8202.6	77	0
			ADR366	Carsem-M 5-TSOT	Q6658.11	77	0
					Q6658.12	77	0
					Q6658.13	77	0
			ADR392		Q7853.1	77	0
Biased HAST (HAST)[1,2]	JESD22-A110	130°C 85%RH 2atm, Biased 96 hours	AD8629	Amkor-P 8-SOIC_N	Q7100.14	77	0
					Q7100.15	77	0
					Q7100.16	77	0
			ADR02		Q6969.6	77	0
					Q6969.14	77	0
					Q6969.15	77	0
			AD8601	Carsem-M 5-SOT_23	Q6729.10	77	0
					Q6729.11	77	0
					Q6729.21	77	0
			ADR366	Carsem-M 5-TSOT	Q6658.7	76	0
					Q6658.8	77	0
					Q6658.9	76	0
			ADR392		Q7853.6	77	0
High Temperature Storage Life (HTSL)[2]	JESD22-A103	150°C 1,000 hours	AD8630	Amkor-P 14-SOIC_N	Q7954.8	45	0
			AD8629	Amkor-P 8-SOIC_N	Q7892.3	45	0
			AD8601	Carsem-M 5-SOT_23	Q6729.13	45	0
			ADR366	Carsem-M 5-TSOT	Q6658.10	45	0

Test Name	Specification	Conditions	Device	Package	Lot #	Sample Size	Qty. Failures
High Temperature Storage Life (HTSL)[2]	JESD22-A103	150°C 1,000 hours	AD8202	Amkor-P 8-SOIC_N	Q5481.12	77	0
					Q5481.13	77	0
					Q5481.2	77	0
			AD8512		R66760.1	77	0
			AD8671		R66900.1	77	0
					R66901.1	77	0
			ADR02		Q6969.8	45	0
Temperature Cycling (TC)[1,2]	JESD22-A104	-65°C / +150°C 500 cycles	AD8630	Amkor-P 14-SOIC_N	Q7954.10	77	0
					Q7954.11	77	0
					Q7954.12	77	0
			AD8628	Carsem-M 5-SOT_23	Q8202.11	77[4]	0
				Carsem-M 5-TSOT	Q8202.10	77[5]	0
			ADR392		Q7853.2	77	0
			AD8629	Amkor-P 8-SOIC_N	Q7892.5	77[6]	0
			ADR02		Q6969.18	77	0
					Q6969.11	77	0
					Q6969.19	77	0
			AD8601	Carsem-M 5-SOT_23	Q6729.18	77	0
					Q6729.19	77	0
					Q6729.20	77	0
			ADR366	Carsem-M 5-TSOT	Q6658.14	77	0
					Q6658.15	77	0
					Q6658.16	77	0
			AD8671	Amkor-P 8-SOIC_N	R61634.1	77	0
			AD8202	Amkor-P 8-SOIC_N	Q5481.4	77	0

[1] These samples were subjected to preconditioning (per J-STD-020 Level 1) prior to the start of the stress test. Level 1 preconditioning consists of the following:

- Bake: 24 hrs @ 125ºC,
- Soak: Unbiased Soak: 168 hrs @ 85ºC, 85%RH,
- Reflow: 3 passes through an oven with a peak temperature of 260ºC.

[2] Pre- and post-stress electrical test was performed at ambient and hot temperatures.

[3] Pre- and post-stress electrical test was performed at ambient temperature.

[4] Post-TC wire bond pull testing was performed per AEC-Q100 on five devices from TC lot# Q8202.11. Minimum bond pull recorded was 5.00grams force. Complete data for the five units are presented in Appendix A of this report.

[5] Post-TC wire bond pull testing was performed per AEC-Q100 on five devices from TC lot# Q8202.10. Minimum bond pull recorded was 7.70grams force. Complete data for the five units are presented in Appendix A of this report.

[6] Post-TC wire bond pull testing was performed per AEC-Q100 on five devices from TC lot# Q7892.5. Minimum bond pull recorded was 4.90grams force. Complete data for the five units are presented in Appendix A of this report.

Table 3: Process Qualification Test Results

Test Name	Specification	Conditions	Device	Fab Process	Lot #	Sample Size	Qty. Failures
Early Life Failure Rate (ELFR)[3]	MIL-STD-883, Method 1015	125°C, Biased 48 hours	ADW84402	TSMC Fab 9 0.6um CMOS	Q6248.20	800	0
					Q6248.21	800	0
					Q6248.24	800	0
High Temperature Operating Life (HTOL)[2]	JESD22-A108	125°C ‹ Tj ‹ 135°C, Biased 1,000 hours	ADUM1402W		Q7170.11	45	0
					Q7170.12	45	0
					Q7170.13	45	0
		150°C ‹ Tj ‹ 175°C, Biased 500 hours	ADW84402		Q6248.10	45	0
					Q6248.11	45	0
					Q6248.12	45	0
			AD8601		Q7507.3	77[1]	0
			AD8692		Q7248.11	77[1]	0

[1] These Samples were subjected to preconditioning (per J-STD-020 Level 1) prior to the start of the stress test. Level 1 preconditioning consists of the following:

- Bake: 24 hrs @ 125ºC,
- Soak: Unbiased Soak: 168 hrs @ 85ºC, 85%RH,
- Reflow: 3 passes through an oven with a peak temperature of 260ºC.

[2] Pre- and post-stress electrical test was performed at hot, ambient and cold temperatures.
[3] Pre- and post-stress electrical test was performed at ambient and hot temperatures.

Samples of the many devices manufactured with these package and process technologies are continuously undergoing reliability evaluation as part of the ADI Reliability Monitor Program. Additional qualification data is available on Analog Devices' web site.

ESD Test Results

The results of ESD testing are summarized in the ESD Results Table. All parts were electrically tested at room and hot temperatures pre- and post-stress. ADI measures ESD results using stringent test procedures based on the specifications listed in Table 4. Any comparison with another supplier's results should ensure that the same ESD test procedures have been used. For further details, please see the EOS/ESD chapter of the ADI Reliability Handbook (available via the 'Quality and Reliability' link at http://www.analog.com).

Table 4: ESD Test Results

ESD Model	Package	ESD Test Spec	RC Network	Highest Pass Level	First Fail Level	Class
FICDM	8-SOIC_N	ANSI/ESD STM5.3.1-1999	1Ω, Cpkg	±1500V	NA	C6
FICDM	5-TSOT	ANSI/ESD STM5.3.1-1999	1Ω, Cpkg	±1000V	±1500V	C5
FICDM	5-SOT_23	ANSI/ESD STM5.3.1-1999	1Ω, Cpkg	±1000V	±1500V	C5
HBM	8-SOIC_N	ANSI/ESD STM5.1-2007	1.5kΩ, 100pF	±7000V	±8000V	3A
MM	8-SOIC_N	ANSI/ESD STM5.2-1999	0Ω, 200pF	±200V	±400V	M3

Latch-Up Test Results

Six samples of the AD8628 were Latch-up tested at T_A=125ºC per JEDEC Standard JESD78, Class II, Level A. Pre- and post-stress electrical test was performed at ambient and hot temperatures. All six devices passed.

Approvals

Reliability Engineer: Robert Yhap
This report has been approved by electronic means (4.0)

Additional Information

Data sheets and other additional information are available on Analog Devices' web site: http://www.analog.com

Appendix

Appendix A: Post TC Wire Bond Pull Test Results

Appendix A:
Post-TC Wire Bond Pull Test Results

Qual#8202 **AD8628 8-SOT_23**
Lot#8202.11

	Measurement in grams force				
DUT **BOND**	**1**	**2**	**3**	**4**	**5**
1	6.20	6.30	7.70	7.15	5.65
2	6.10	5.40	7.20	6.90	5.50
3	5.50	5.00	5.55	6.70	7.00
4	6.20	5.85	5.75	6.30	6.60
5	5.80	6.65	5.90	5.90	5.65

min	5.00
avg	6.18
max	7.70
std dev	0.667

Qual#8202 **AD8629 8-TSOT**
Lot#8202.10

	Measurement in grams force				
DUT **BOND**	**1**	**2**	**3**	**4**	**5**
1	11.95	12.05	10.70	10.75	9.85
2	7.70	8.35	9.95	16.35	7.80
3	11.30	12.90	11.60	11.75	11.05
4	10.70	10.00	11.25	9.55	10.20
5	11.45	11.85	10.30	11.50	12.25

min	7.70
avg	10.92
max	16.35
std dev	1.74

Qual#7892 **AD8629 8-SOICnb**
Lot#Q7892.5

	Measurement in grams force				
DUT **BOND**	**1**	**2**	**3**	**4**	**5**
1	6.35	6.25	5.65	7.65	7.75
2	6.25	4.90	6.40	5.05	7.40
3	6.25	6.65	6.45	7.50	5.60
4	7.20	6.50	6.35	7.75	7.25
5	6.20	6.60	5.55	7.10	6.50
6	6.85	5.95	6.65	5.40	6.15
7	6.55	4.95	6.20	5.65	6.15
8	6.85	6.45	6.05	6.20	5.70
9	5.75	5.45	6.00	5.10	7.45
10	6.95	6.35	5.80	7.65	6.85

min	4.90
avg	6.36
max	7.75
std dev	0.747