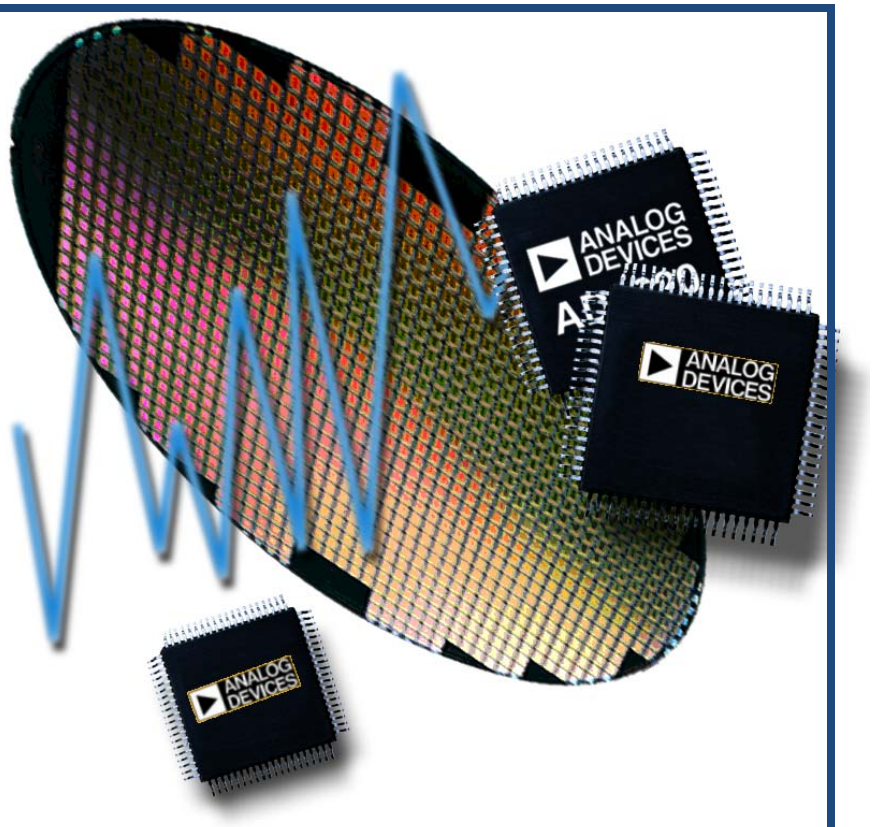

Reliability Report

Report Title: AD7400A (8-PDIP) & AD7400A/AD7401A (16-SOIC_W) Product Qualification

Report Number: 6823

Revision: A

Date: 10 July 2008

Summary

This report documents the successful completion of the reliability qualification requirements for release of the AD7400A in 8-PDIP and AD7400A/AD7401A products in a 16-SOIC_W. The AD7400A and AD7401A are second-order, Σ-Δ modulators that convert an analog input signal into a high speed, 1-bit data stream with on-chip digital isolation based on Analog Devices, Inc., *i*Coupler® technology.

Table 1: AD7400A Product Characteristics

Die/Fab

Maximum Power Dissipation (W)	0.100	
Device / Die ID	N79A	N712B
Die Size (mm)	1.51 x 2.90	1.50 x 2.87
Wafer Fabrication Site	I_LIMK0206	E_TSMC0908
Wafer Fabrication Process	0.50um DPTM CMOS	0.6um DPTM CMOS
Passivation Layer	undoped-oxide/SiN	undoped-oxide/SiN
Bond Pad Metal Composition	AlSiCu	AlCu

Package/Assembly

Available Package	8-PDIP
Body Size (mm)	9.53 x 6.35 x 3.30
Assembly Location	Carsem-S
Molding Compound	Sumitomo G600C
Wire Type	Gold Tanaka M3
Wire Diameter (mils)	1.30
Die Attach	Ablestik 84-3J
Lead Frame Material	Copper
Lead Finish	100Sn
Moisture Sensitivity Level	5
Maximum Peak Reflow Temperature (°C)	260

Table 2: AD7400A Product Characteristics

Die/Fab

Maximum Power Dissipation (W)	0.100	
Device / Die ID	N79A	N712B
Die Size (mm)	1.51 x 2.90	1.50 x 2.87
Wafer Fabrication Site	I_LIMK0206	E_TSMC0908
Wafer Fabrication Process	0.50um DPTM CMOS	0.6um DPTM CMOS
Passivation Layer	undoped-oxide/SiN	undoped-oxide/SiN
Bond Pad Metal Composition	AlSiCu	AlCu

Package/Assembly

Available Package	16-SOIC_W

Body Size (mm)	10.35 x 7.62 x 2.50
Assembly Location	Carsem-S
Molding Compound	Sumitomo 6600H
Wire Type	Gold Tanaka M3
Wire Diameter (mils)	1.30
Die Attach	Ablestik 84-3J
Lead Frame Material	Copper
Lead Finish	100Sn
Moisture Sensitivity Level	1
Maximum Peak Reflow Temperature (°C)	260

Table 3: AD7401A Product Characteristics

Die/Fab

Maximum Power Dissipation (W)	0.100	
Device / Die ID	N79A	N71
Die Size (mm)	1.51 x 2.90	1.50 x 2.87
Wafer Fabrication Site	I_LIMK0206	E_TSMC0908
Wafer Fabrication Process	0.50um DPTM CMOS	0.6um DPTM CMOS
Passivation Layer	undoped-oxide/SiN	undoped-oxide/SiN
Bond Pad Metal Composition	AlSiCu	AlCu

Package/Assembly

Available Package	16-SOIC_W
Body Size (mm)	10.35 x 7.62 x 2.50
Assembly Location	Carsem-S
Molding Compound	Sumitomo 6600H
Wire Type	Gold
Wire Diameter (mils)	1.30
Die Attach	Ablestik 84-3J
Lead Frame Material	Copper
Lead Finish	100Sn
Moisture Sensitivity Level	1
Maximum Peak Reflow Temperature (°C)	260

Description / Results of Tests Performed

Table 4 provides a description of the qualification tests conducted and the associated test results for products manufactured on the same technologies as described in Tables 1, 2, and 3. All devices were electrically tested before and after each stress. Any device that did not meet all electrical data sheet limits following stressing would be considered a valid (stress-attributable) failure unless there was conclusive evidence to indicate otherwise.

Table 4: Package Qualification Test Results

Test Name	Conditions	Specification	Device	Package	Lot Num	Sample Size	Qty. Rejects
Autoclave [1]	121C 100%RH 2atm 96hrs	JEDEC-STD-22, Method A102	AD7400A	8-PDIP-300_MIL	S180568.1	77	0
					S180569.1	77	0
					S180570.1	77	0
SHR [1]	See Below	ADI-0049	AD7400A	8-PDIP-300_MIL	S180568.3	11	0
					S180569.3	11	0
					S180570.3	11	0
Temp Cycle [1]	-65C/+150C 500cycles	JEDEC-STD-22, Method A104	AD7400A	8-PDIP-300_MIL	S180568.2	77	0
					S180569.2	77	0
					S180570.2	77	0

[1] These Samples were subjected to preconditioning (per J-STD-020 Level 5) prior to the start of the stress test. Level 5 preconditioning consists of the following:

- Bake: 24 hrs @ 125°C
- Unbiased Soak: 72 hrs @ 30°C, 60%RH
- Reflow: 3 passes through an oven with a peak temperature of 260+0/-5°C

Samples of the many devices manufactured with these package and process technologies are continuously undergoing reliability evaluation as part of the ADI Reliability Monitor Program. Additional qualification data is available on Analog Devices' web site.

ESD Test Results

The results of ESD testing are summarized in the ESD Results Table. ADI measures ESD results using stringent test procedures based on the specifications listed in Table 5. Any comparison with another supplier's results should ensure that the same ESD test procedures have been used. For further details, please see the EOS/ESD chapter of the ADI Reliability Handbook (available via the 'Quality and Reliability' link at http://www.analog.com).

Table 5: ESD Test Results

ESD Model	Package	ESD Test Spec	RC Network	Highest Pass Level	First Fail Level	Class
FICDM	8-PDIP	ANSI/ESD STM5.3.1-1999	1Ω, Cpkg	1.5kV	±NA	C6
FICDM	16-SOIC_W	ANSI/ESD STM5.3.1-1999	1Ω, Cpkg	1.5kV	±NA	C6
HBM	16-SOIC_W	ESD Assoc. STM5.1-2001	1.5kΩ, 100pF	2.5kV	±NA	C2

Latch-Up Test Results

Six samples of the AD7400A were Latch-up tested at Ta=25ºC per JEDEC Standard JESD78, Class I, Level A. All six devices passed.

Approvals

Reliability Engineer: Colm Heffernan
This report has been approved by electronic means (4.0)

Additional Information

Data sheets and other additional information are available on Analog Devices' web site:
http://www.analog.com